Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 30th January 2004

Birmingham:	**Steve Hillier, Gilles Mahout, Richard Staley, Pete Watkins**
Heidelberg:	**Ralf Achenbach, Florian Föhlisch, Eike-Erik Kluge, Kambiz Mahboubi, Karlheinz Meier, Pavel Meshkov, Frederik Rühr, Vladimir Savinov*, Klaus Schmitt**
Mainz:	**Cano Ay, Stefan Rieke, Uli Schaefer**
RAL:	**Bruce Barnett, Norman Gee, Tony Gillman, Adrian Mirea, Weiming Qian**
Stockholm:	**Christian Bohm, Attila Hidvegi, Sam Silverstein**
	***visiting from Pittsburgh**

1. Birmingham

- Integration tests have been successfully carried out at RAL with three CPMs feeding either RoI or DAQ data to a single ROD.
- With three CPMs in adjacent slots, there is occasional loss of G-link lock during a run, when L1A signals are present. There is also some evidence from scope measurements that the TTC clock jitter increases under these conditions, which may be exacerbating the problem. Further studies will be made, including observing the effect of increasing the TTC traffic.
- New ROC firmware has been written to provide a minimum of three clock ticks between successive DAVs for RoI data, to ensure compliance with the predictions made by Weiming's ROD simulations. These firmware changes will now also be made to the DAQ data path.

2. Heidelberg

- A lot of work has continued with the PPM design, and the last few problems have now all been solved. The pcb is now ready to be submitted for manufacture.
- The reason for the low yield of 30% good MCM substrates from Wurth remains unknown. The 30 good substrates were sent to Hasec for optical inspection and for pull testing to measure bond strengths. Visual inspection revealed that the surface finish of the bond pads is apparently not good, but the results of the pull tests were very encouraging, with a high mean figure of 12-13cN. The batch of 100 substrates from the second-source Swiss company is expected to be delivered in early February.
- Assembly of these 30 new MCMs cannot take place until the new PPrASICs become available (mid March?).
- Vladimir Savinov has been visiting KIP from Pittsburgh to carry out tests of the LAr receiver module. He summarised the results that had been found:
    - Using playback of non-saturated LAr pulse data, the receiver performed perfectly, as expected from the measurements already performed in Pittsburgh and described at length in the FDR documentation.
    - Increasing the gain in the receiver allowed a study of internal saturation effects. The permissible input signal range before saturation sets in is currently asymmetric (–2.5V to +2.1V). It is proposed to increase the positive limit to +2.5V by means of changing some component values, but it is estimated that this will increase the electronic noise figure from 520 microvolts to ~600 microvolts (for the entire signal chain), which still remains well below the FADC quantisation noise. This change will first be modelled in detail, and then tried on an actual receiver channel and the resultant noise measured.

- The worrying result concerns the response of the receiver to input signals that are already saturated in the tower builders, where the 15nsec internal shaping time constant in the receiver introduces considerable distortion into the flat-tops of the pulses and will almost certainly produce incorrect BCID results. Although this needs more study, no solution has yet been proposed.
- Cross-talk measurements have been made, by driving one channel with full-amplitude, but non-saturated, pulses and measuring the coupled signal on a second channel. A cross-talk figure of better than 0.3% was measured, compared to a figure of 0.15% for direct injection at Pittsburgh.
- Finally, summation of signals split between the barrel and end-cap LAr calorimeter regions was successfully tried.

- Florian reported that he has been working on the DAQ software, but has encountered some problems (with partitions?). He and Cano spent some time in Mainz looking at the problem, but it is not yet resolved.

3. Mainz

- The new JEM1 design is now with Rohde & Schwarz for pcb manufacture and assembly. They have reported some problems with the lack of metallisation on the underside of some of the vias, but after some discussions with their assembly experts, they believe that they can proceed to produce at least the four boards for the Slice Tests. For larger-scale production, there may need to be a layout modification to correct this problem and to ensure a good yield.
- The JEM1 firmware designs are now being finalised.
- Electrical-optical and optical-electrical conversion of the DAQ/RoI G-link signals has been tried using "flying-lead" test cards. Differential G-link signals from a JEM feed a Stratos optical transmitter, feeding 10m of optical fibre into a Stratos optical receiver driving single-ended signals to a G-link receiver daughter-card on a DSS. Using fill-frames and PRBS data sequences, the links appear robust, with no evidence of loss of lock. More systematic tests are planned, and the test cards will accompany the JEMs to RAL in February for the next phase of the integration tests.
- The 9U crate is now being used with a VMM and Concurrent processor, although there are some mechanical problems with the VMM which need to be addressed. The VMM itself will be re-designed for the final ATLAS trigger system, with this and other problems fixed.
- TTCrx-derived clock jitter has led to problems where the FPGAs have not configured correctly. The problem disappeared when the optical fibre drive cable was replaced.
- It would be very useful to have an L1A generator in Mainz, but this will depend on the availability of GIO cards.

4. RAL

Tony summarised the status reports received from Viraj and Ian, who were unable to be at the meeting:

- The 9U ROD schematic design is almost complete, and checking has started. In two or three days it will be ready to submit to the Drawing Office for layout.
- There are a few outstanding issues still to be resolved:
  - How should the Crate Geographical addresses be derived?
  - Spare I/O pins must be defined for the FPGAs.
  - If the VME64x backplane is retained (rather than the VME64xP variant), the onboard +5V and +3.3V power supply distribution probably needs some re-partitioning.

- The required Xilinx devices have a long (12 week) delivery lead time, so they should be ordered now.

- All paperwork for the manufacture and assembly of the new CPM PCB is now ready, and the order will be sent today. With Richard's agreement, we decided to request a "standard" 15-day (pcb) + 10-day (assembly) turnaround time, rather than an accelerated 10-day + 7-day programme, which is more expensive and would carry a higher risk.
- CMM-Energy firmware:
  - The source of a bug in the ET memory reported by Murrough and Jurgen was caused by a typo in an unrelated section of firmware, causing data contention on the VME bus. This will be fixed in the next firmware release.
  - VME access to the algorithm block (originally designed by Andrea) is being modified, and it will be homogenised with the rest of the design. Most of the work is complete, and all the changes so far have been transparent to the user, but the firmware won't be released until it is fully finished.
  - To complete the design, the ET-miss LUTs must be mapped directly into the VME address space, rather than have them accessed via a single location and an address counter. This has been discussed but a specification has yet to be agreed. A specification must be available by next Monday to ensure a new version of the CMM-energy code is ready for the next JEM tests.
- CMM firmware (all versions):
  - The 6U ROD design requires a gap in the DAV signal between readout events of some minimum number of bunch crossings. The CMM readout controller code could easily be modified to insert such a gap (if a Change Request were generated). There are no other outstanding Change Requests.
- Bruce reported that the readout system using the HOLA cards is coming together well, and there are a further six new Interposer cards ready in Birmingham.
- Weiming reported that ten new TTCdec cards of the latest design have been assembled and tested, and he already has available nine which are fully working.

5. Stockholm

- Sam is preparing CMM-Jet firmware for the forthcoming RAL integration tests with Ian in early February.
- Attila is also preparing two different versions of new Jet algorithm firmware for the February integration tests at RAL.
- ERNI can supply a three-level mating version of the B19 connectors, which occupy about 65% of each CPM/JEM slot, at a reasonable price. This should reduce the high insertion forces, although not by as much as was hoped. We should probably order the parts soon to ensure availability.
- AMP are being pursued to supply a tool to repair/replace damaged connector pins. The representative from ERNI advised that it would be very difficult to use such a tool in situ without first removing the backplane, but we have at least one example upon which we could practise!

Next Phone Conference – 13th February 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman