Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 30th September 2004

Birmingham: **Gilles Mahout, Richard Staley, Dimitrios Typaldos, Pete Watkins**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Christoph Geweniger, Paul Hanke, Kambiz Mahboubi*, Pavel Meshkov, Klaus Schmitt, Hans-Christian Schultz-Coulon**

QMUL: **Eric Eisenhandler**

RAL: **Bruce Barnett, Norman Gee, Tony Gillman**

Stockholm: **Attila Hidvégi**

***** *at CERN (ATLAS test-beam)*

1. Birmingham

- Gilles reported that he has been examining the CP FPGA firmware to try to discover the cause of the Read-Write errors seen at the test-beam for a particular VME register. He believes that he has fixed a bug in the code, which could have caused the problem. However, he also thinks that the VME-- bus that was damaged with a broken pin during the TCM swap may be causing some problems.
- Richard reported that the LVDS Source Module (LSM) is currently in the Drawing Office. Component placement is finished, and routing is under way.
- The new CPM 1.9 design is also being routed at present.

2. Heidelberg

- Paul reported that the new batch of ASIC wafers will arrive at KIP one week earlier than expected, and tests on them will start at the beginning of November.
- The problems of non-accessibility of the PHOS4 chips on the PPM seen at the test-beam must be studied in the laboratory at KIP – the test-beam environment is not appropriate.
- During the initial MCM tests at KIP, the PHOS4 dies could be accessed via I2C as expected, but these tests had been done on the MCM test rig, and not when the devices were mounted on a PPM board. Therefore it is unlikely to be a fault with the MCM itself.
- Norman asked if this problem could be studied at KIP with the "golden" PPM and the homebrew processor. One difficulty may be to find someone to modify the ReMFPGA firmware in the short term at KIP.
- The PHOS4 reset problem was also discussed. The latest version of the PHOS4 chip is renamed PRODE, and is a rad-hard version of the original design. It is unclear whether it is available in die form.
- There has been an important meeting with the MCM companies Hasec and Würth, where many of the remaining technical issues concerning MCM production were discussed. One of the major issues discussed was the proposal from the manufacturers to change from the silicone gel cavity filling to a 2-step dam and fill glob-top encapsulation technique, which is more straightforward and an industry-standard process. The MCM lid is now only needed to act as an electrical shield.
- The proposal is therefore over the next couple of weeks to assemble two small batches (4-6 devices) of MCMs – one batch using dam and fill and the other with gel fill. Both batches will then undergo thermal and vibration stressing to look at failure rates.

3. QMUL

- Eric noted that the CMM Final Design Review had concluded successfully, with some recommendations regarding further testing, in particular with the inputs populated with as many

source modules as possible to maximise the Backplane background traffic. Ian will update the test plan. One important lesson was that future reviews should not be held until all necessary preparation work had been completed, irrespective of the scheduled review timetable. (Extreme pressures of test-beam work had hindered this in the case of the CMM.)

4. RAL

Viraj had submitted a status report as follows:

- **CPM 1.9:** Most of the components for two CPM 1.9 modules which were used on the previous version are in stock at RAL, except for the Xilinx XCV1000E FPGAs for which a quotation has been requested. New components, such as the optical transceivers, PLLs etc, need to be ordered soon.

  Bruce queried whether the lack of stock XCV1000E devices indicated a looming problem for our forthcoming production, as this is now a rather old Xilinx family.

- **LSM:** Two LSMs will be manufactured by CEMGRAFT on a 'one-stop-shop' basis. The Bill of Materials has been supplied for to obtain a quotation and lead times.
- **CMC-format G-Link Optical Receiver cards**: Four cards have been ordered from CEMGRAFT (PCB manufacture, assembly and component procurement) on 21st September, and delivery is expected on 13th October.
- **TCM-VME64**: Initial schematic modifications have been made, and final design modifications are awaited. The outline of the new board is complete, and component placement is ongoing pending final schematic modifications which should be finalised by next week. The schematics will be posted on the web for review as soon as they have been independently checked.
- **TCM-CP/JEP:** This is not as advanced as the TCM-VME64, but it is expected to be completed by mid-October. The schematics will be posted on the web for review as soon as they have been independently checked.
- **VMM:** The schematics are complete and the layout is in progress. The schematics will be posted on the web for review as soon as they have been independently checked.
- **9UROD:** Following the JTAG tests from a few weeks ago, the Trigger Lab crate will be used for testing the module, once an external 48V supply has been added. Firmware development continues. Dummy loads are available to test System ACE, as soon as the crate is ready.
- **CMM:** At the test-beam, tests were made of the interface between the CMM and the CTP Input Module. The polarity of the LVDS channel pairs is reversed between the two modules, which the CTP group will correct in firmware. The parity bit was suspected to be arriving one clock tick late at the CTP. However, careful timing measurements showed it to be exactly in phase with the data, and Ian's extensive gate-level simulation of the firmware shows that it is sent on the correct clock tick. Ian therefore believes that it is not a CMM problem.

5. Stockholm

Sam had submitted the following status report:

- The 9U Wiener crates have still not arrived from CERN. (Due to some mix-up, they were actually still at CERN, but real shipping is imminent!)
- Sam has sent the Backplane pin replacement tool-kit to CERN for use in emergencies at the test-beam.
- Due to an unfortunate incident during the repair of his laptop computer, Sam is having to reconstitute the tender documents and write the papers for the Backplane Final Design Review from 3-year-old backups that he has found on an old computer. He has no estimate yet on when this will all be completed.

- Ian had expressed concern that the total logic used in the CMM FPGA design for the JEP is slightly less than the equivalent design in the CP system. Having examined the design, Sam had found no problems so far, and believes the probable reason to be that the JEP system only merges data from two crates rather than four, so the big adder tree is reduced significantly. This leaves extra room for FCAL handling and Jet-ET calculations that use several extra memories, but not a large amount of logic. Actual testing of the design should reveal more.

6. Test-Beam

Kambiz summarised the current situation in the test-beam work (much more information can be found in his detailed daily status reports):

- The parity-error problem seen with the JEM LVDS input data is always on the same pair of channels. Swapping MCMs and LCD cards does not cure it. Re-routing these two channels on to alternative LCD pins by firmware is being attempted.
- The second PPM has a problem of often spontaneously powering itself down when operated in the test crate. It also has one bad channel on its LCD card (as well exhibiting the parity-error problem on the same channel-pair as seen in the first PPM).
- Juergen and Murrough have been working on the offline software. The calorimeter trigger system was unfortunately removed from the combined running overnight (29/30 September), but will be included again as soon as possible.

Next Phone Conference – Thursday 14th October 2004 at 10:00 (UK), 11:00 (Germany, Sweden)

Tony Gillman