9U ROD (status 6/02/04)

- **Schematics all most complete**
  - **Assigning pins on J3 user pins**
    - **GA<5> (crate address)**
    - **Power to Rear S-Link cards (3A@ 3v3)**
- **Started to check the schematics**
- **Scheduled to hand over to DO last week**
- **Changes:**
  - **VME buffers (Data and Address)**
  - **VME 64xP -> VME64x**
    - **Re-design power distribution**
- **DO can start work now**
  - **Place 'modules'**
    - **9 x (optical + electrical +)**
    - **5 x (4 x G-link + Input FPGA +)**
- **More checking!**
- **Order FPGAs today!**
- **Panagiotis leaves RAL end of February 2004**

Floor plan (Provisional)