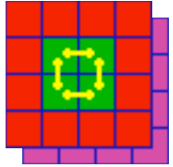


Trigger crate orders for 2004



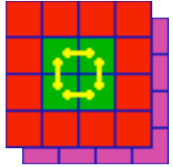
- ATLAS was asked to place all 2004 crate orders in December 2003
 - ▲ For us this is essentially all our crates, including test rigs
- Need 4 different types of 9U crate:
 - ▲ TileCal receivers (*same as LAr, copy their order*)
 - No VME64, custom backplane, rear-transition modules
 - ▲ CP and JEP
 - No VME64, custom backplane
 - ▲ RODs
 - VME64 with J3, rear-transition modules
 - ▲ Preprocessor
 - VME64, custom J3



TileCal receivers



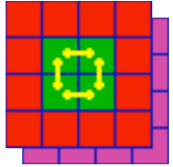
- **Backplane:** Pittsburgh custom (*fitted by Wiener*)
- **Rear-transition modules:** 120mm (*non-standard*)
- **6U slots:** None
- **Power:** 100A @ +5V digital,
100A @ +5V analogue, 100A @ -5V analogue
- **Configuration, cooling:** Above crate, air
- **Test-rig:** *Pittsburgh responsibility*
- **Problems:** None
- **Quantity:** 2 (*Stockholm*)
- **Delivery:** CERN – June



CP and JEP



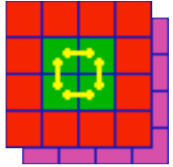
- **Backplane: Stockholm custom**
- **Rear-transition modules: None (*i.e. no runners*)**
- **6U slots: 2**
- **Power: 300A @ +5V, 200A @ +3.3V**
- **Configuration, cooling: Rear door, water**
- **Test-rig: Similar but power above crate, air**
- **Problems: None**
- **Quantities: 7 for system (*4 UK, 3 Stockholm*)
2 for test-rigs (*UK*) (+1 existing)**
- **Delivery: Stockholm – June; test-rig – Nov.**



RODs (1)



- Backplane: **VME64x** (*was VME64xP!*) + J3
- Rear-transition modules: **160mm**
- 6U slots: **2**
- Power: **200A** (*was 300A*) @ +5V, **200A** @ +3.3V, **24A** @ +48V
- Configuration, cooling: **Rear door, water**
- Test-rig: **Similar but power above crate, air**
- Quantities: **3 for system** (*HD, UK, Stockholm*)
1 for test-rig (*UK*) (+1 existing)



RODs (2)



■ Problems:

▲ Is power-pin limit 1.2A or 2.0A/pin? *Disagreement!*
(1.2A is for multiple power pins at 60 °C)

▲ If not 2.0A/pin, wanted to use J0 pins on **VME64xP**

▲ But use of **VME64xP** is not advisable

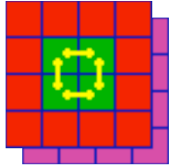
(P. Farthouat and G. Dumont)

- E.g. possible conflict with Concurrent CPU, which might use J0 *if* an optional PMC card is present and CPU has a J0 connector

▲ PROPOSE to use **VME64x** by using 48V pins on J1 and DC–DC converters for some of the power

■ **Delivery:** RAL – June, except 1 crate – Nov.

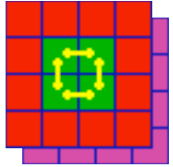
(But order not yet submitted, so possible delay?)



Preprocessor (1)



- Backplane: **VME64x(P?) + HD custom J3**
- Rear-transition modules: **None (*i.e. no runners*)**
- 6U slots: **2**
- Power: **300A @ +5V, 300A @ +3.3V, 40A @ +12V, 40A @ -12V**
(Not yet measured; probably less)
- Configuration, cooling: **Front of rack, air**
- Test rig: **Front of rack, air**
- Quantities: **9 for system (*HD*)**
1 for test rig (*HD*)



Preprocessor (2)



■ Problems:

- ▲ Power requirements cannot be met with 6 ‘bricks’, which is maximum in ATLAS-standard options
- ▲ Power supply location must allow for mass of input and output cables
- ▲ Power-pin limit 1.2A or 2.0A/pin?
 - If not 2.0A, wanted to use J0 pins on VME64xP, but use of VME64xP is not advisable
 - Can avoid possible VME64XP conflict with Concurrent if CPUs *without J0* are *always* used
 - If 2.0A/pin, can use VME64x
- ▲ ATLAS crates not satisfactory; power supplies and power-pins will be discussed directly with Wiener

■ Delivery: ???