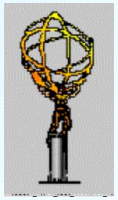
February 2004

CTP, LTP, Rod-Busy Review

See http://agenda.cern.ch/fullAgenda.php?ida=a036454

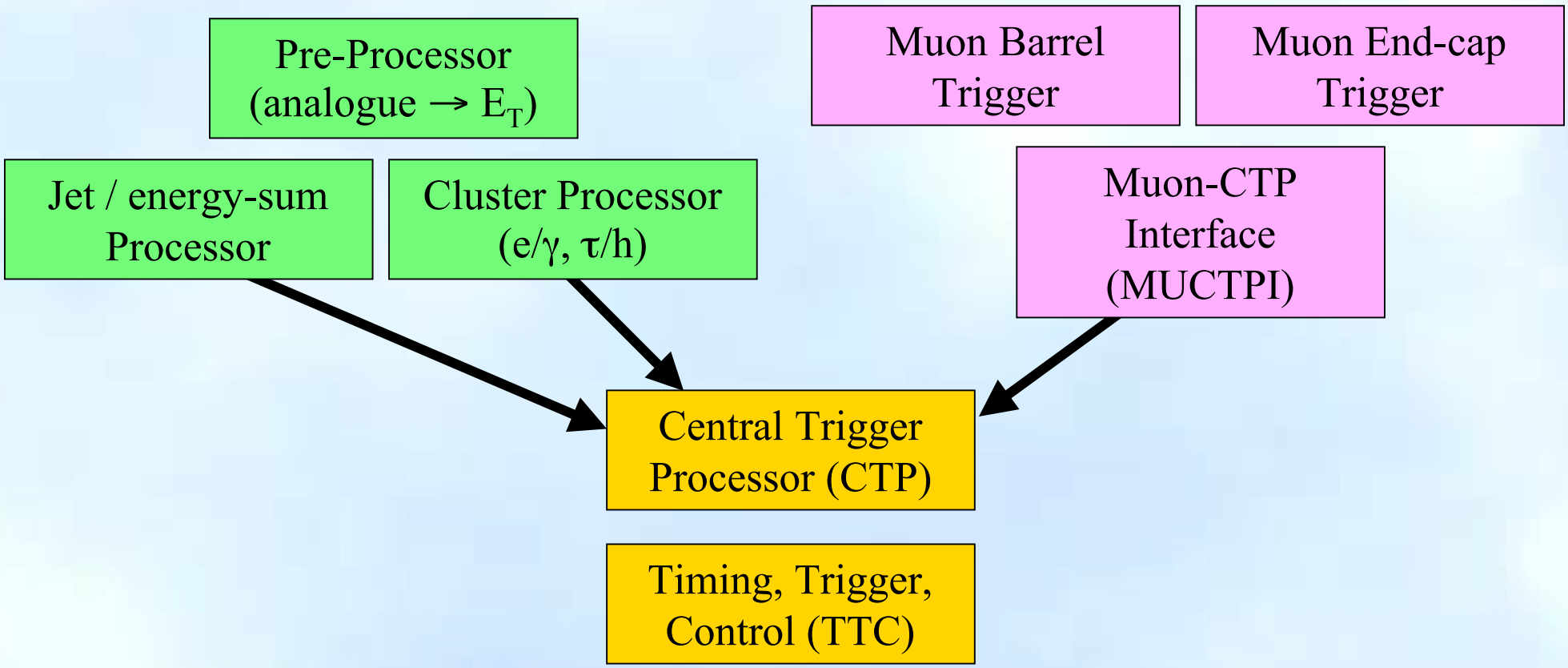
C .N .P .Gee
Rutherford Appleton Laboratory

Level-1 Structure

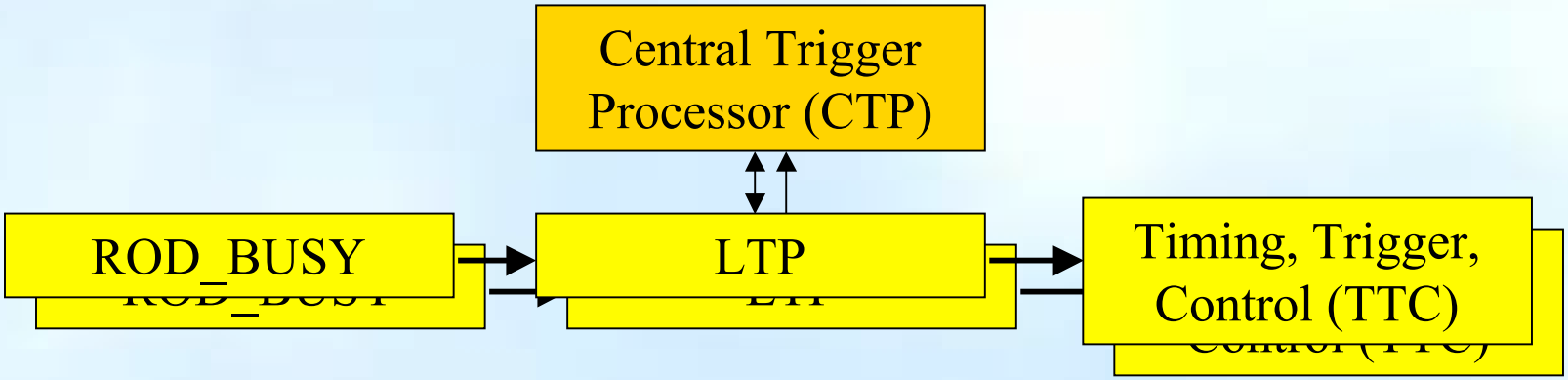


~7000 calorimeter trigger towers

O(1M) RPC/TGC channels



Interface to Detectors



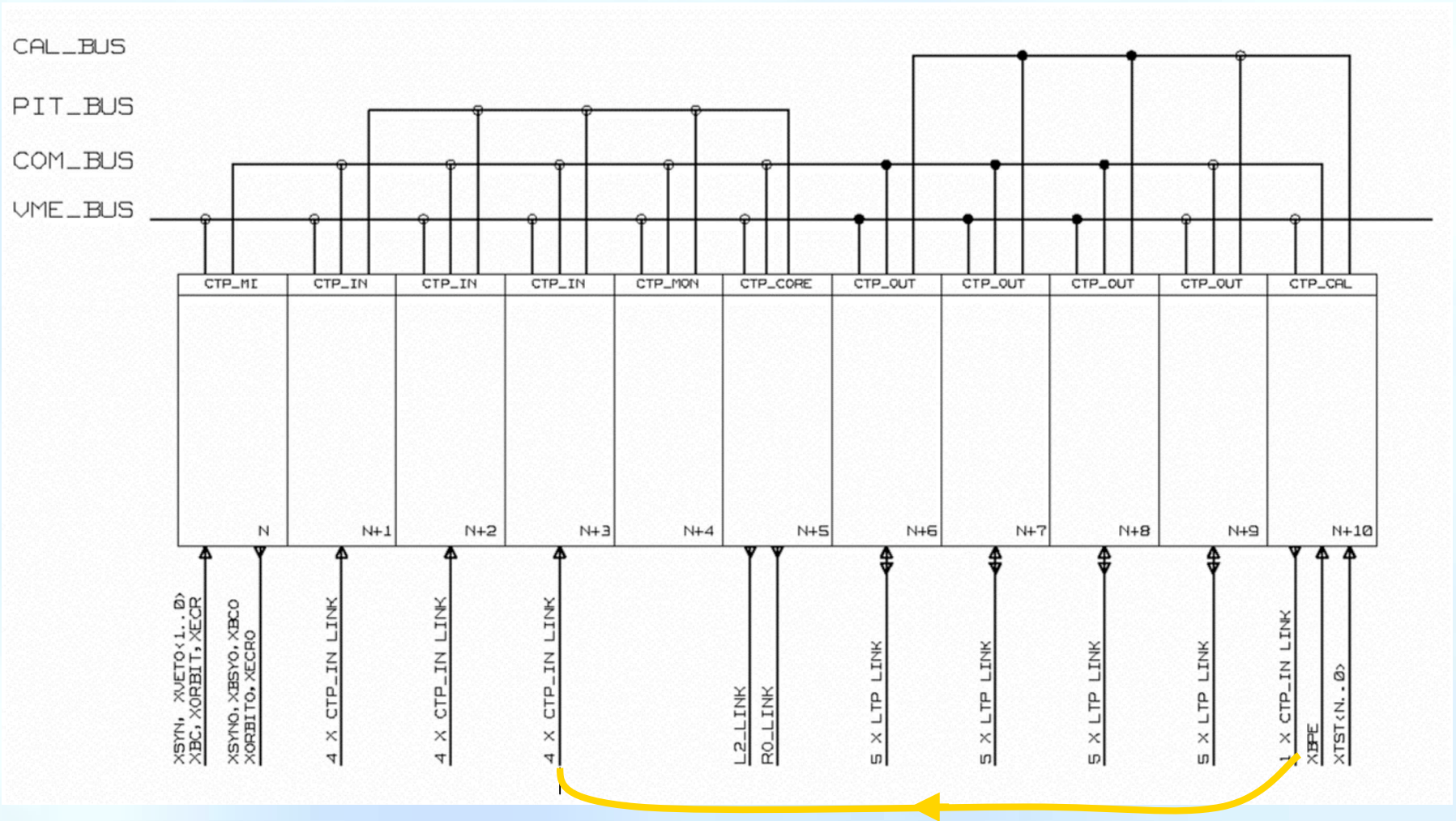
Review Overview

- **Initial plan was for FDR for CTP, LTP and ROD_BUSY**
  - But FDR is strict: requires working modules, performance measurements.
    - ***CTP is not at this stage.***
- **Agree on Interim review for CTP**
  - With FDR after the test beam; will need to be rigorous.
  - Tension between need to complete documentation in detail to ensure robust design, but allow CTP design to proceed quickly.
  - Even so, very large number of comments in detail.
- **PDR for LTP and ROD_BUSY, separately documented**
  - In fact the LTP and ROD_BUSY designs are more advanced and stable. Comments turn out to be relatively minor.

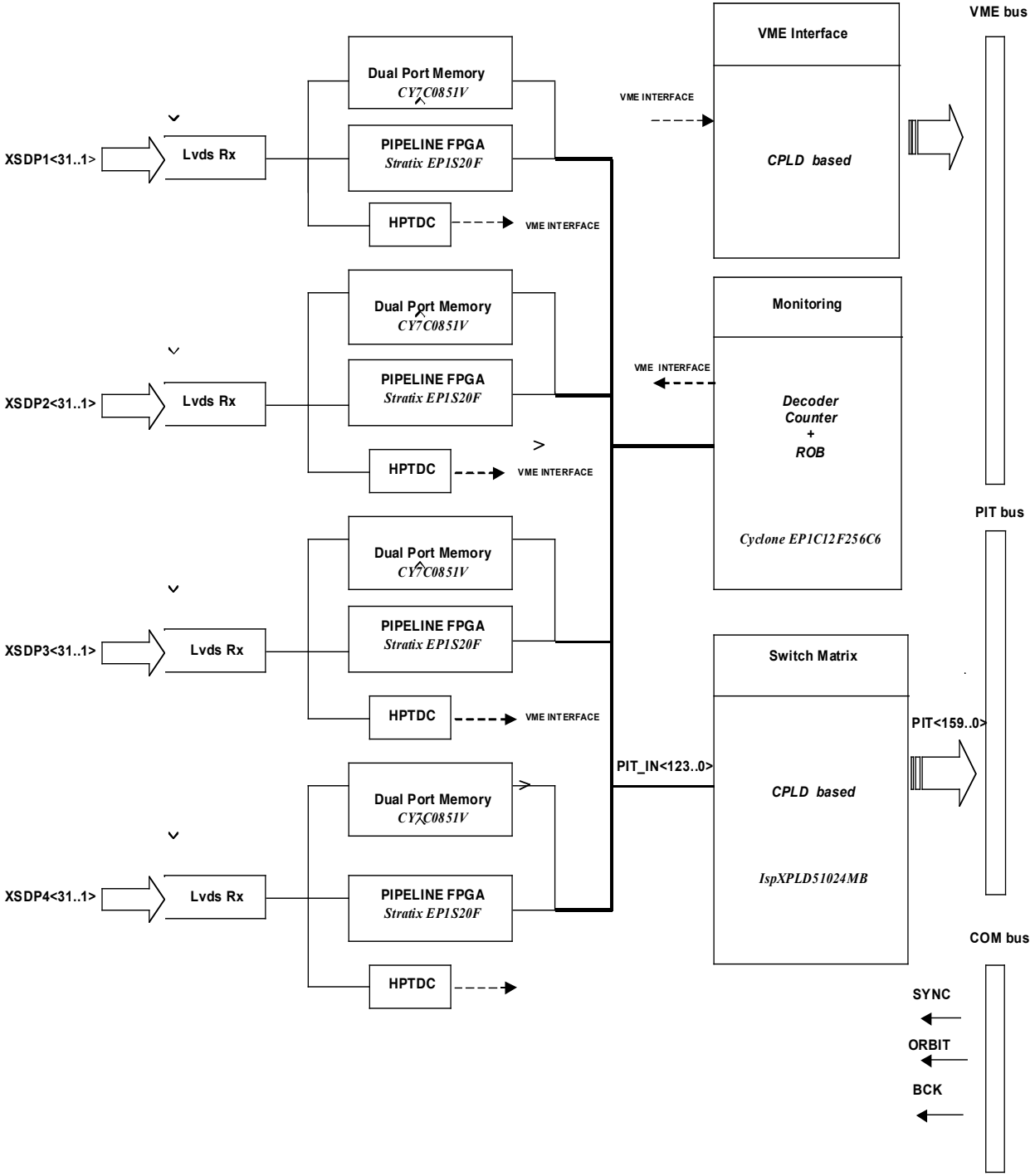
CTP Structure

- **Eleven 9-U modules of 6 separate types. A complex system.**
  - CTP_MI (LHC Machine interface)
  - CTP_IN: 3 modules, total 160 outputs from 3*4*31=372 inputs.
  - CTP_MON: Monitoring by large no of scalers. Prototype exists
  - CTP_CORE: main combinatorial logic module.
  - CTP_OUT: 4 modules, bi-directional links to total of 20 LTPs.
  - CTP_CAL: Calibration pulse generation.
- **Three 40MHz backplanes**
  - PIT_BUS: 160 bits single-ended from 3*INs to CORE and MON
  - COM_BUS: Synchronisation, clocks.
  - CAL_BUS: Calibration request signals.

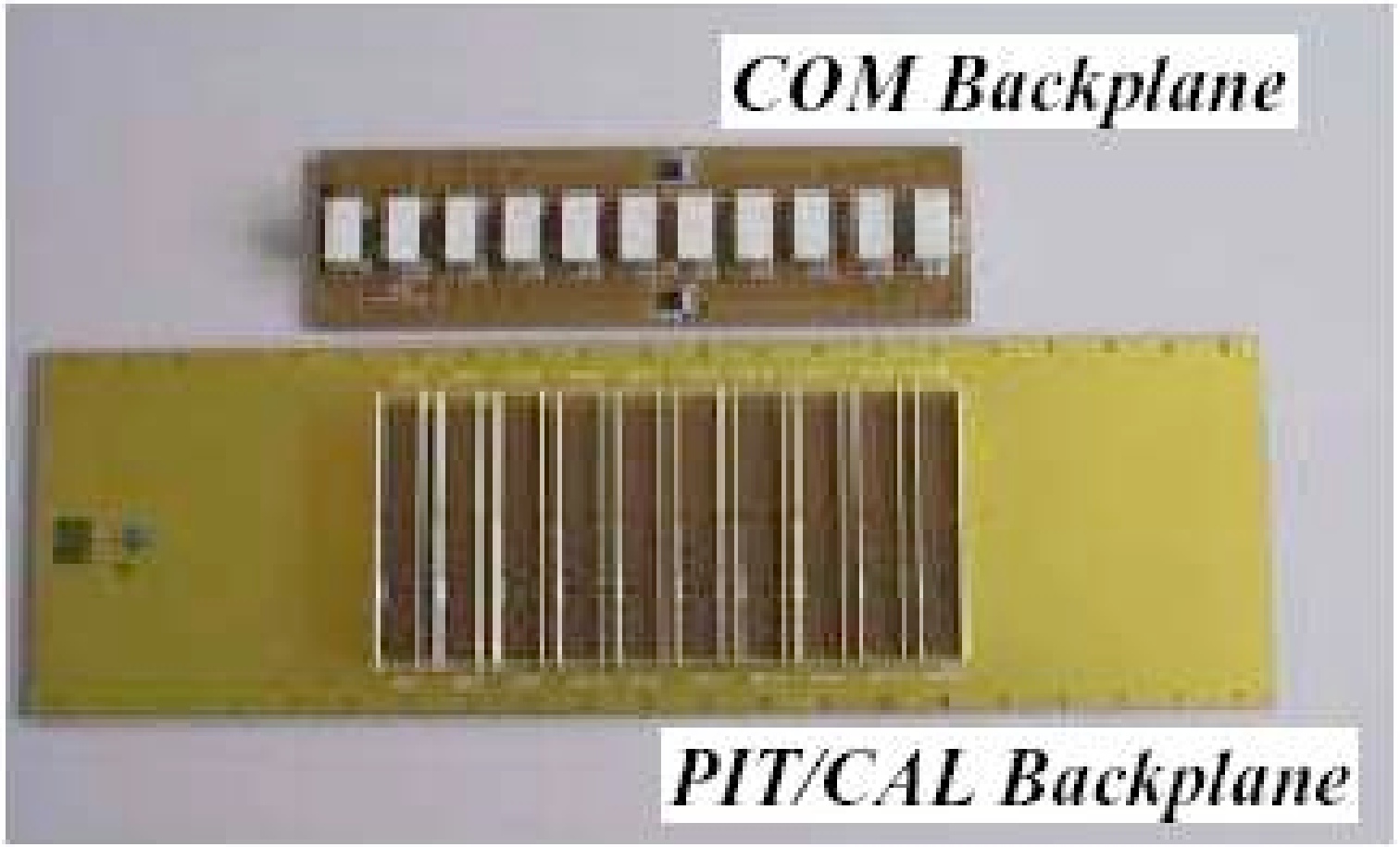
CTP Structure



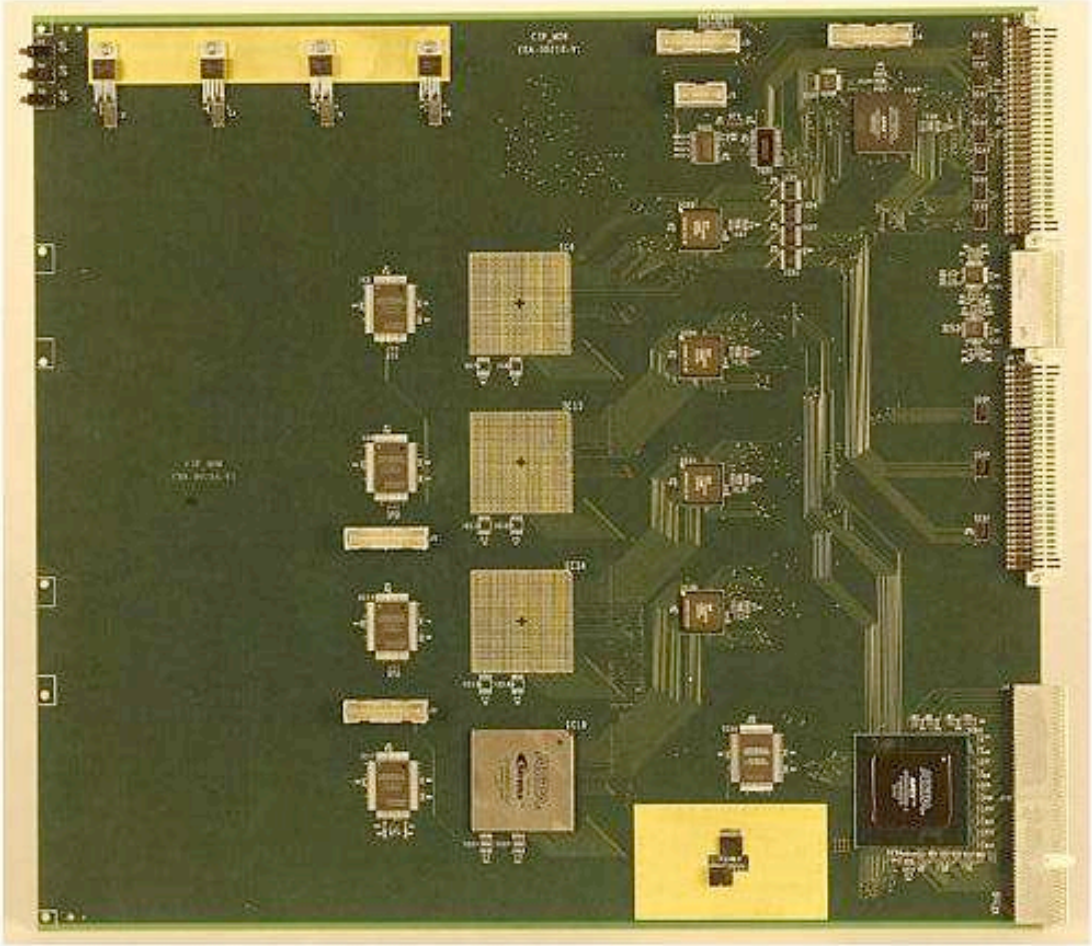
CTP_IN


VME bus
VME Interface
VME INTERFACE
CPLD based
Dual Port Memory
CY7C0851V
PIPELINE FPGA
Stratix EP1S20F
HPTDC
VME INTERFACE
XSDP1<31..1>
Lvds Rx
Monitoring
Decoder
Counter
+
ROB
Cyclone EP1C12F256C6
PIT bus
Switch Matrix
PIT<159..0>
PIT_IN<123..0>
IspXPLD51024MB
COM bus
SYNC
ORBIT
BCK

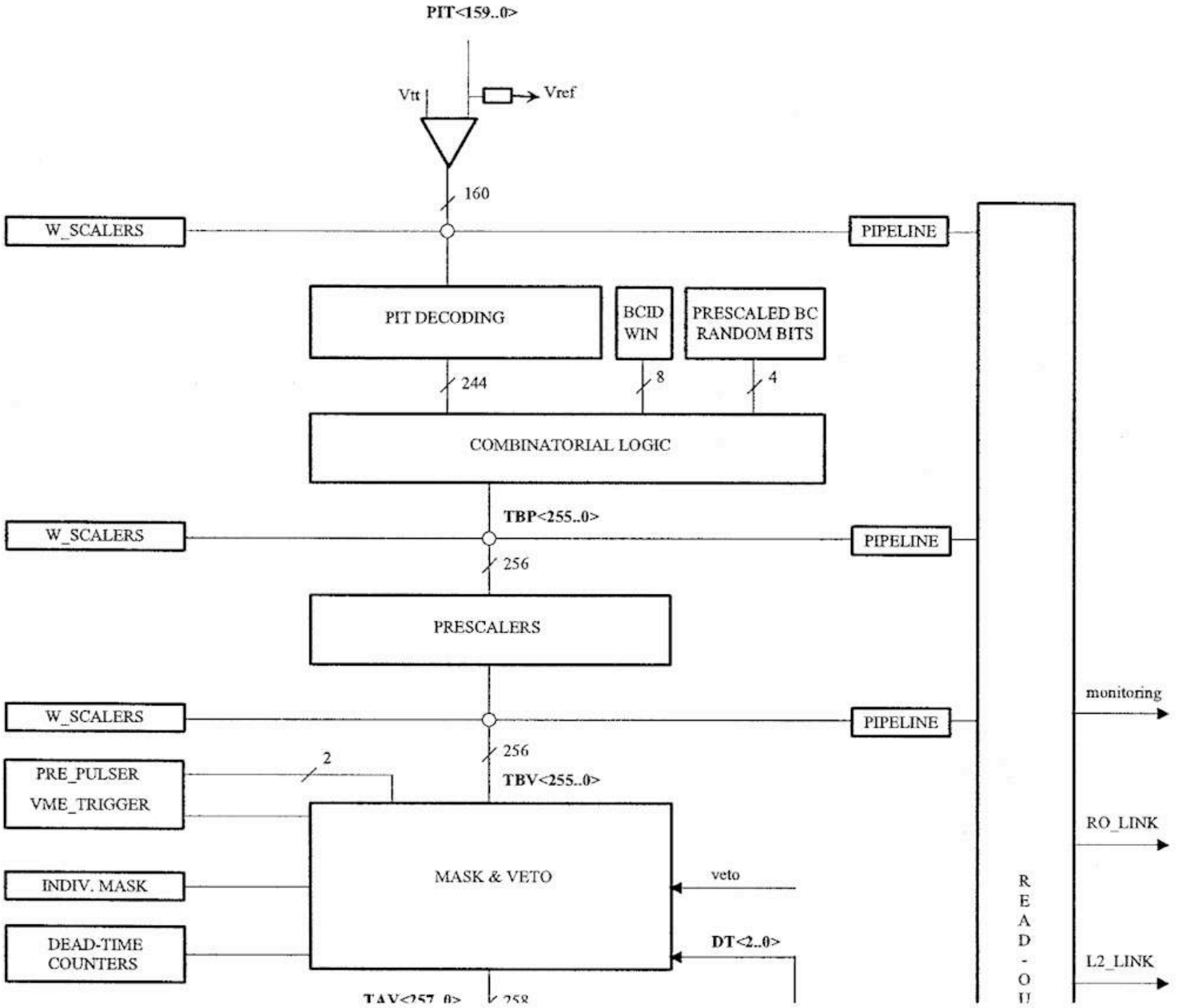
Backplane



CTP_MON



CORE


PIT<159..0>
Vtt
Vref
160
W_SCALERS
PIPELINE
PIT DECODING
BCID WIN
PRESCALED BC RANDOM BITS
244
8
4
COMBINATORIAL LOGIC
TBP<255..0>
W_SCALERS
PIPELINE
256
PRESCALERS
W_SCALERS
PIPELINE
monitoring
256
TBV<255..0>
2
PRE_PULSER
VME_TRIGGER
RO_LINK
MASK & VETO
veto
INDIV. MASK
DEAD-TIME COUNTERS
DT<2..0>
L2_LINK
READ-OUT

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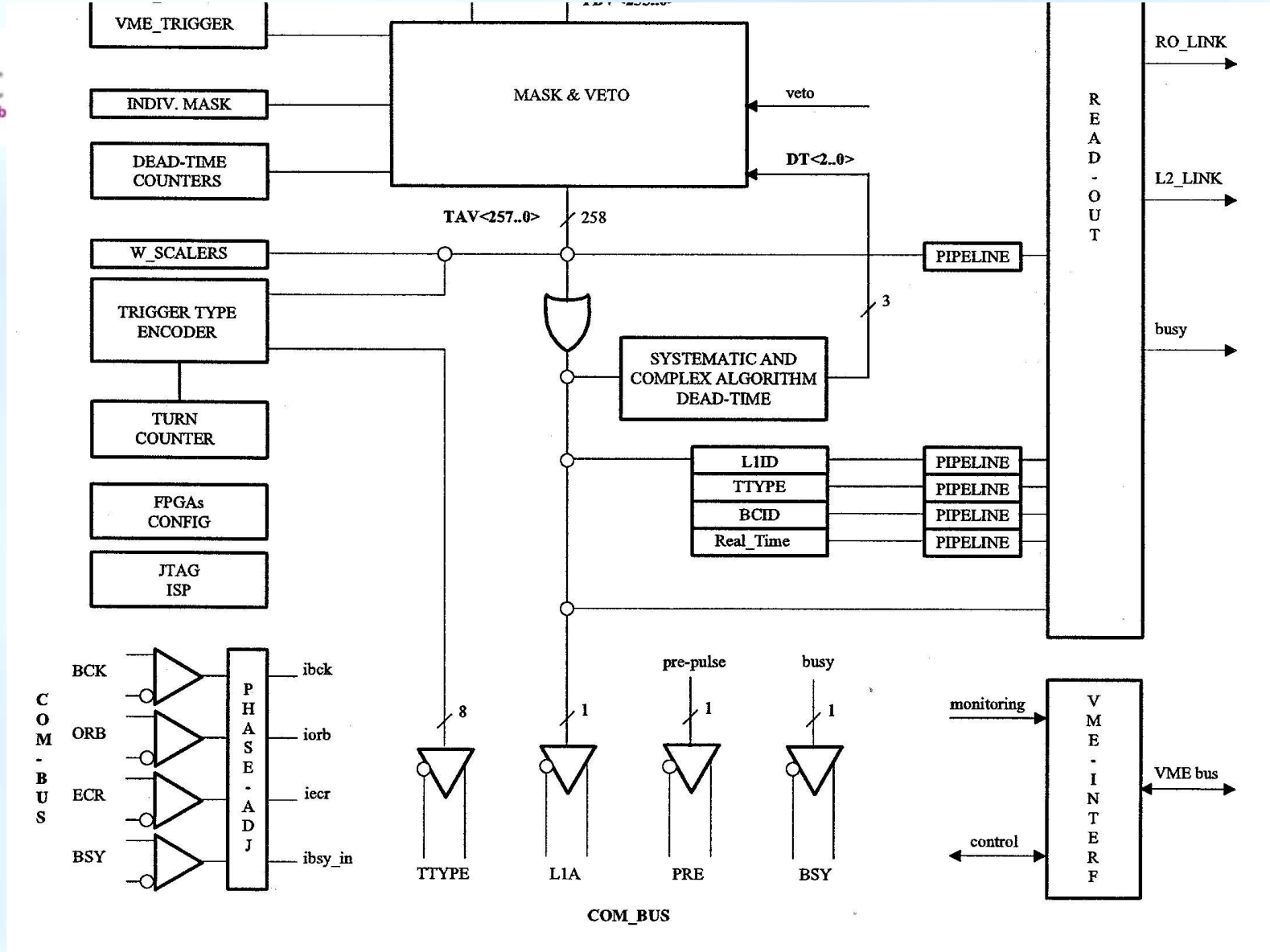
CORE



Status

- **Modules not documented - more information requested:**
  - CTP_MI
  - CTP_OUT:
  - CTP_CAL:
- **Some documentation for**
  - CTP_IN: Detailed design, well thought-out.
  - CTP_MON: No documentation, but prototype exists
  - CTP_CORE: Complex module, tight latency budget, planning reduced version.
- **Three 40MHz backplanes**
  - Prototypes exist, many simulated waveforms.

Status (2)

- **URD: an established document. Still some questions to resolve**
  - Some where ATLAS policy is unclear – e.g. sweeper, trigger types, checkpoint,….
  - Some where detectors need to agree.
  - Some where interface details need to be documented
- **Trigger Menus:**
  - No document, but a series of detailed studies presented. Includes use of unusual triggers – eg cosmic, beam halo. Conclude capacity of design is adequate.
- **Daq & Control.**
  - Good initial document, needs to be correlated with other LVL1 DAQ & Control.

Reviewers Comments

- **Reduced version of CTP_CORE to meet beam timetable.**
- **Adopt Sign-off procedure to ensure detector agreement.**
- **Ask for external documents/decisions on an agreed timescale**

- **Await information on undocumented modules.**

LTP and ROD-BUSY

- **ROD_BUSY is mature, presented many times.**
- **LTP is relatively new, but well documented and clearly well thought out.**
- **Both modules pass PDR with relatively few comments.**
  - Documentation to be updated.
  - Desire for common software support.
- **FDR after use in test beam.**