ATLAS T1

GLINK DAV GAP requirement of ROD f/w

Weiming Qian

UK Meeting, RAL

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3 factors affecting DAV GAP

- GLINK serial data format and SLINK slice data format
- Data FPGA State Machine Design
- Clock domains (GLINK clock .vs. TTC clock40)

GLINK data format and SLINK slice data format

- Header and status words adds to the DAV GAP

	1 GLINK slice data length (serial)	1 SLINK slice data length	Ticks needed to write 1 Slink slice to FIFO
6U ROD CPM DAQ	84	84	84
6U ROD JEM DAQ	89	47	80
9U ROD CPM DAQ	84	85	85
6U ROD Neutral	X	X+1	X+1
9U ROD Neutral	X	X+2	X+2

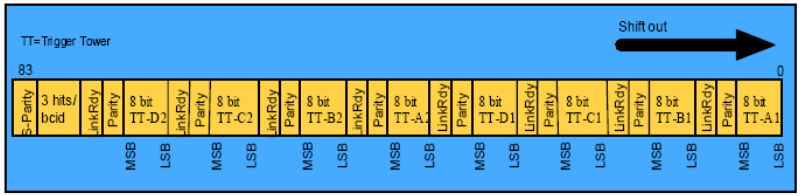


Figure 16: CPM G-Link DAQ data format

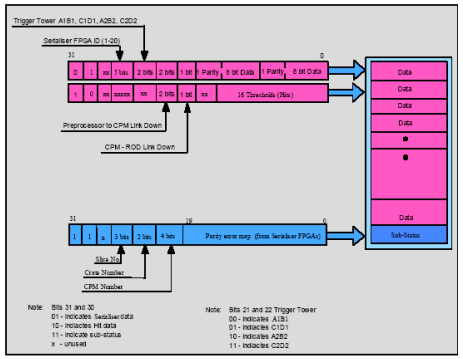
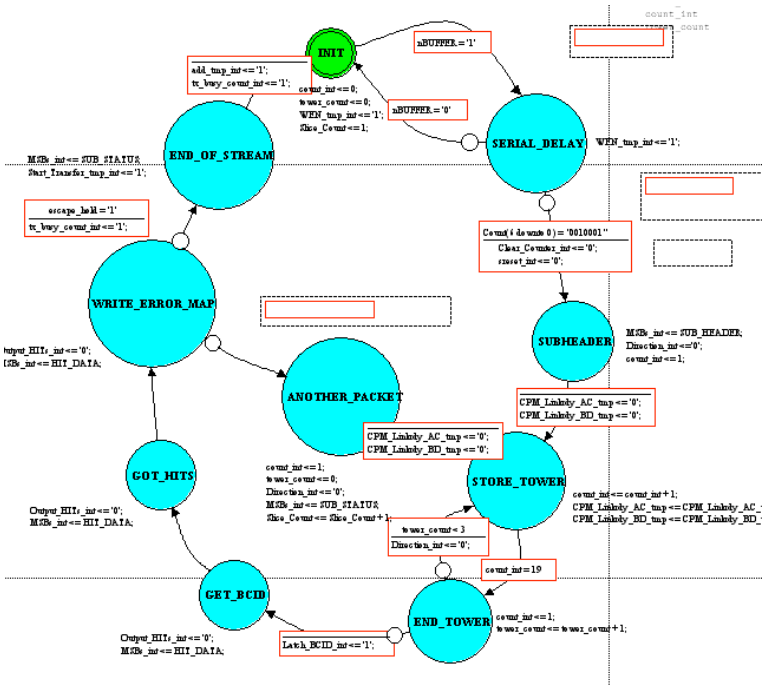


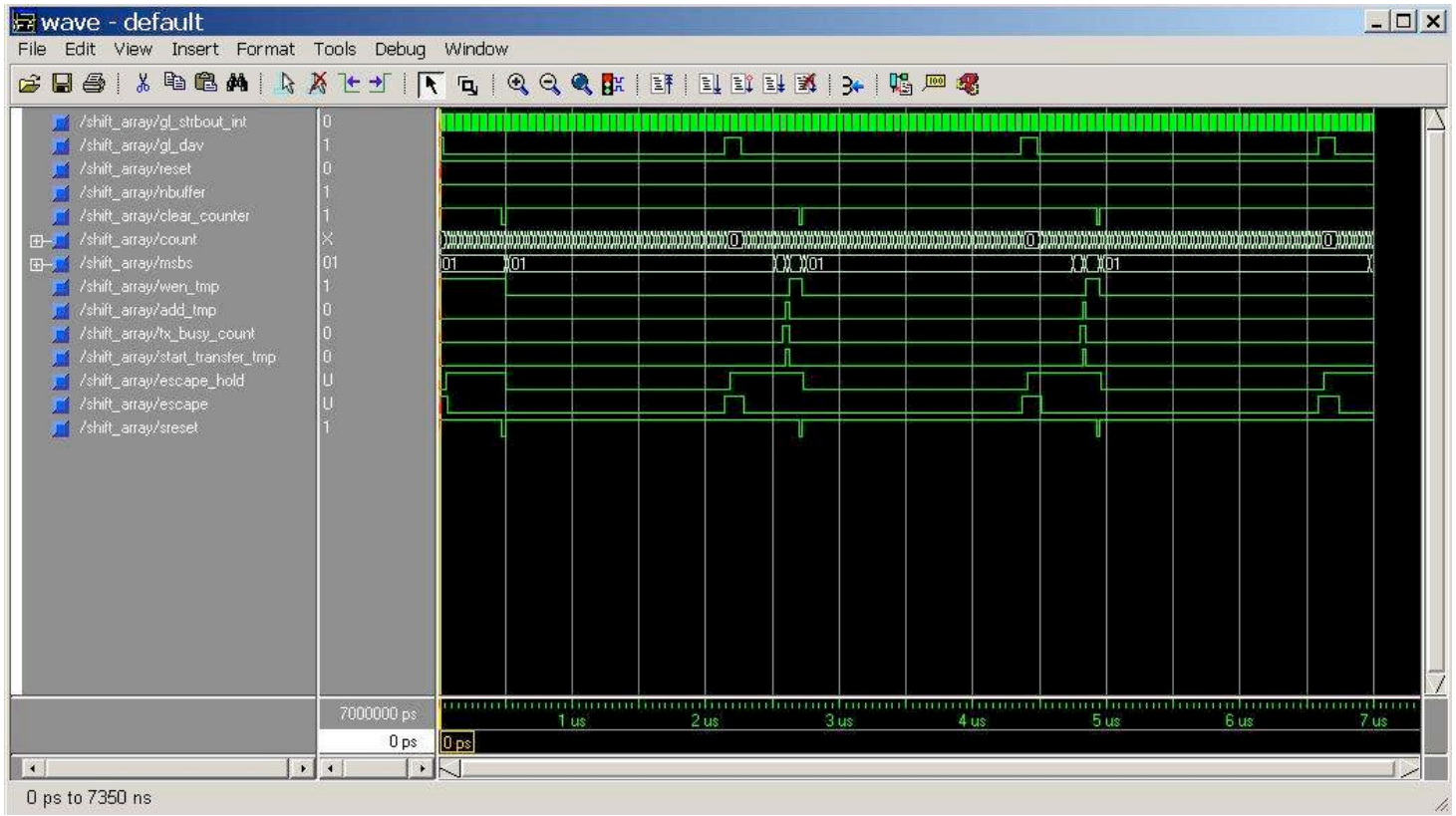
Figure 17: CPM S-Link DAQ data format.

Data FPGA State Machine Design



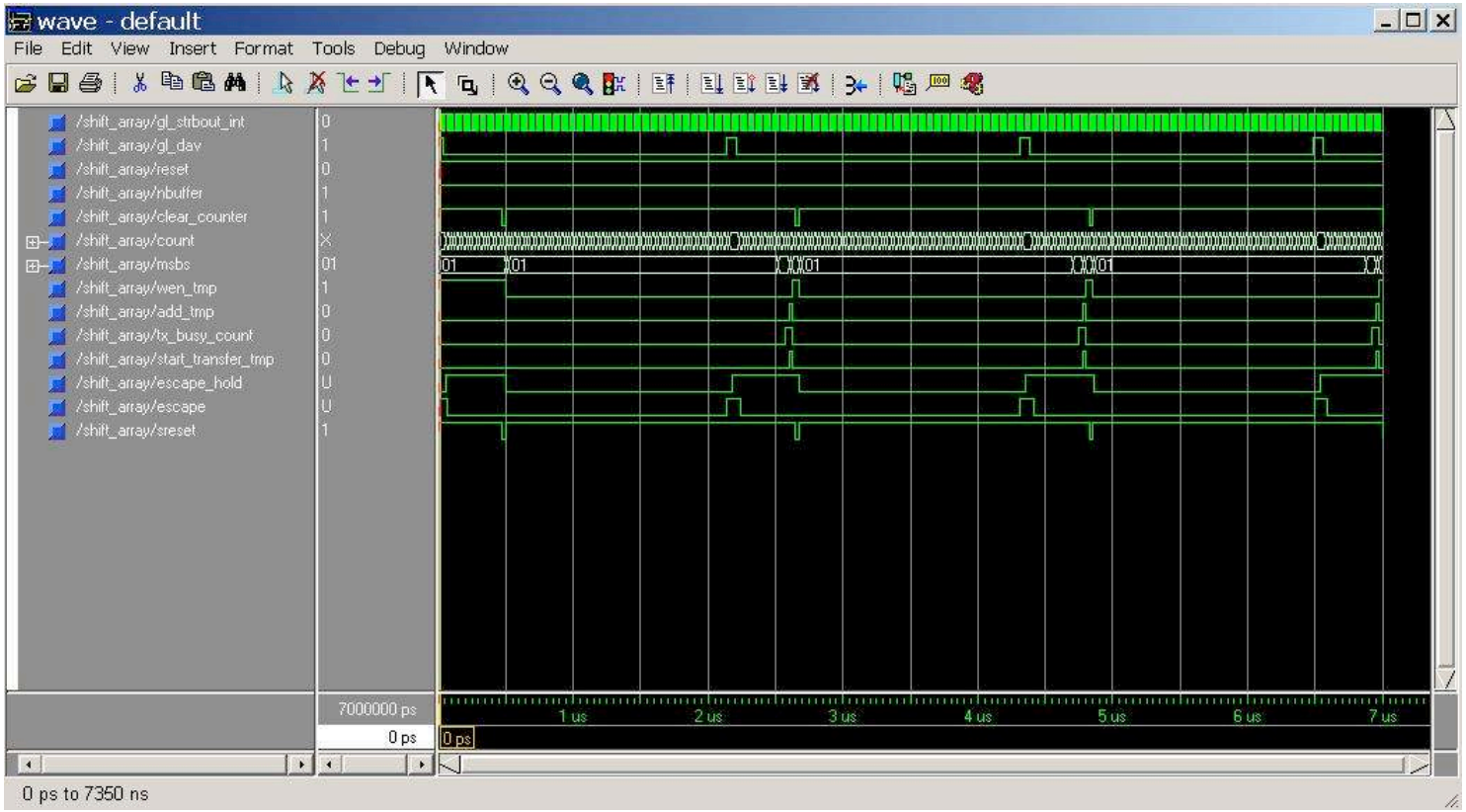
	Additional GLINK DAV GAP needed for State Machine
6U ROD CPM DAQ	3
6U ROD JEM DAQ	3
…	…

State Machine Simulation 1



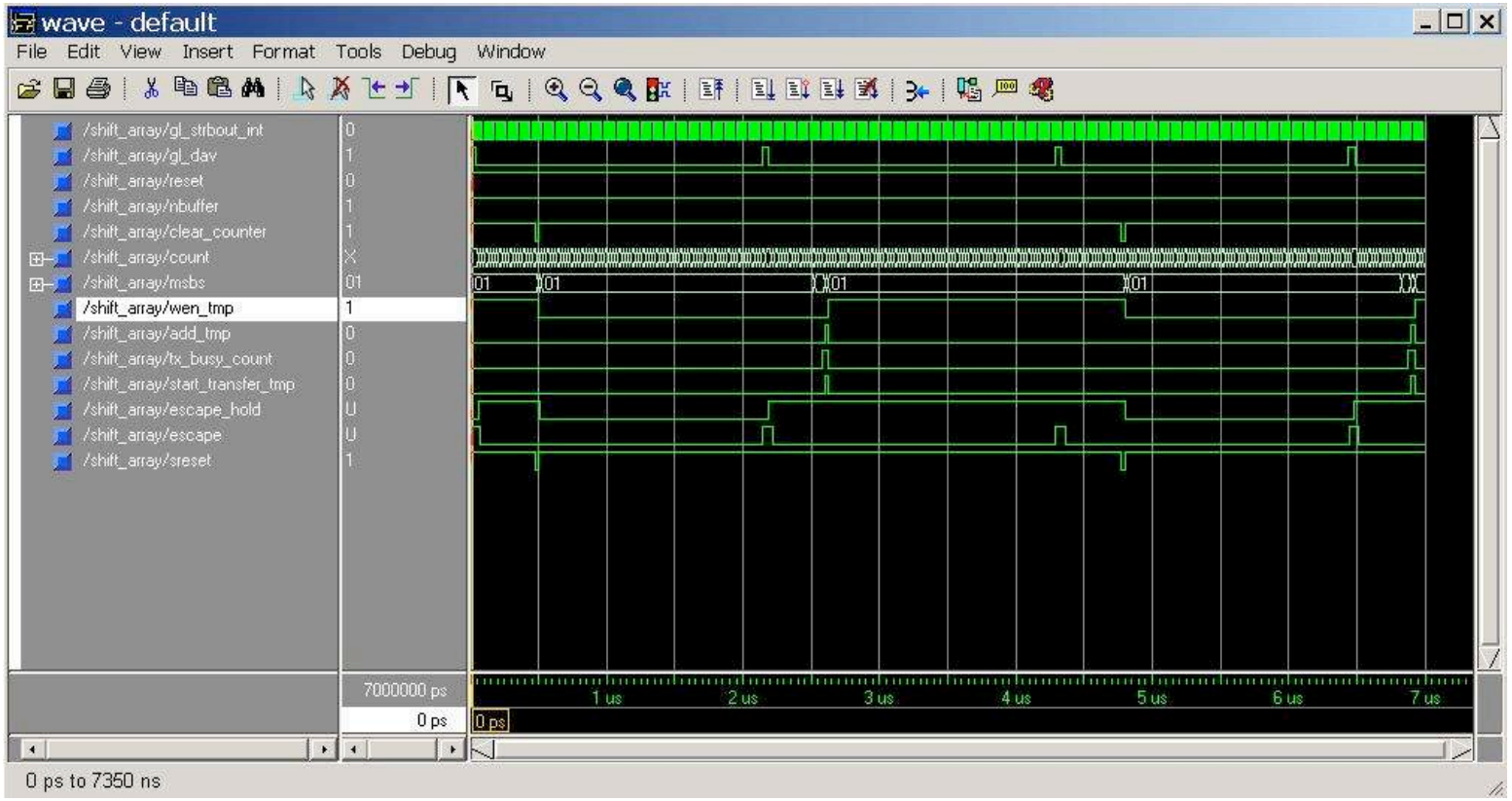
- CPM DAQ State Machine with 5 ticks DAV GAP

State Machine Simulation 2



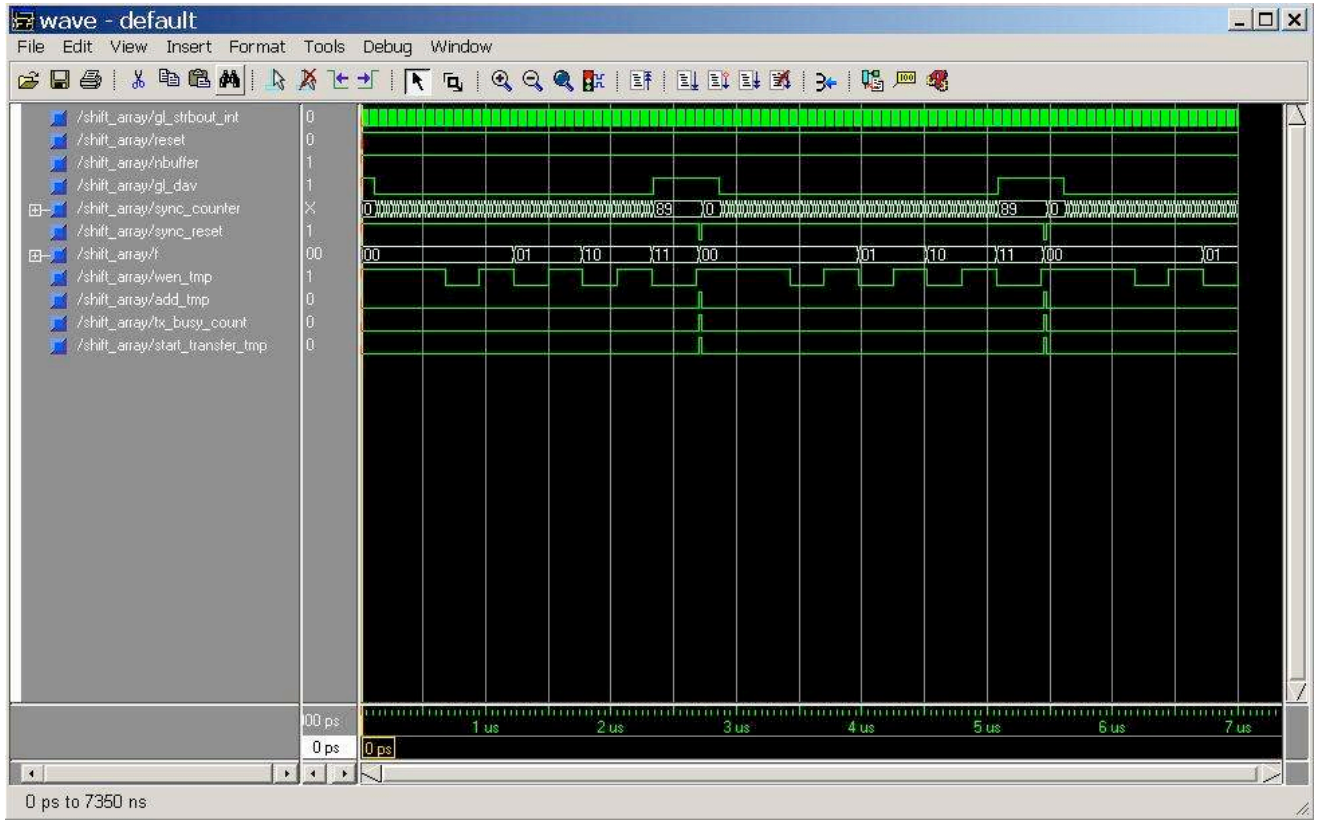
- CPM DAQ State Machine with 3 ticks DAV GAP

State Machine Simulation 3



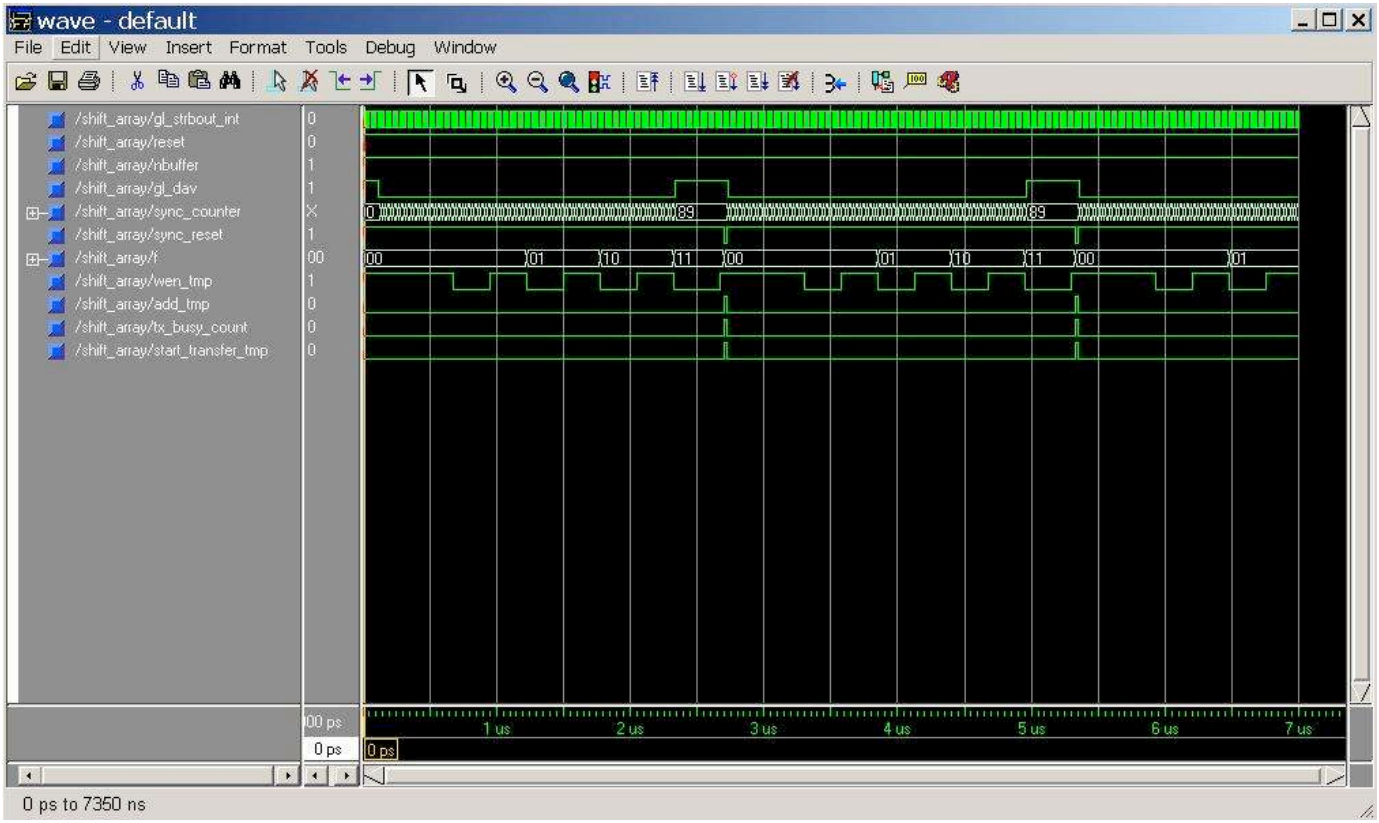
- CPM DAQ State Machine with 2 ticks DAV GAP

State Machine Simulation 4



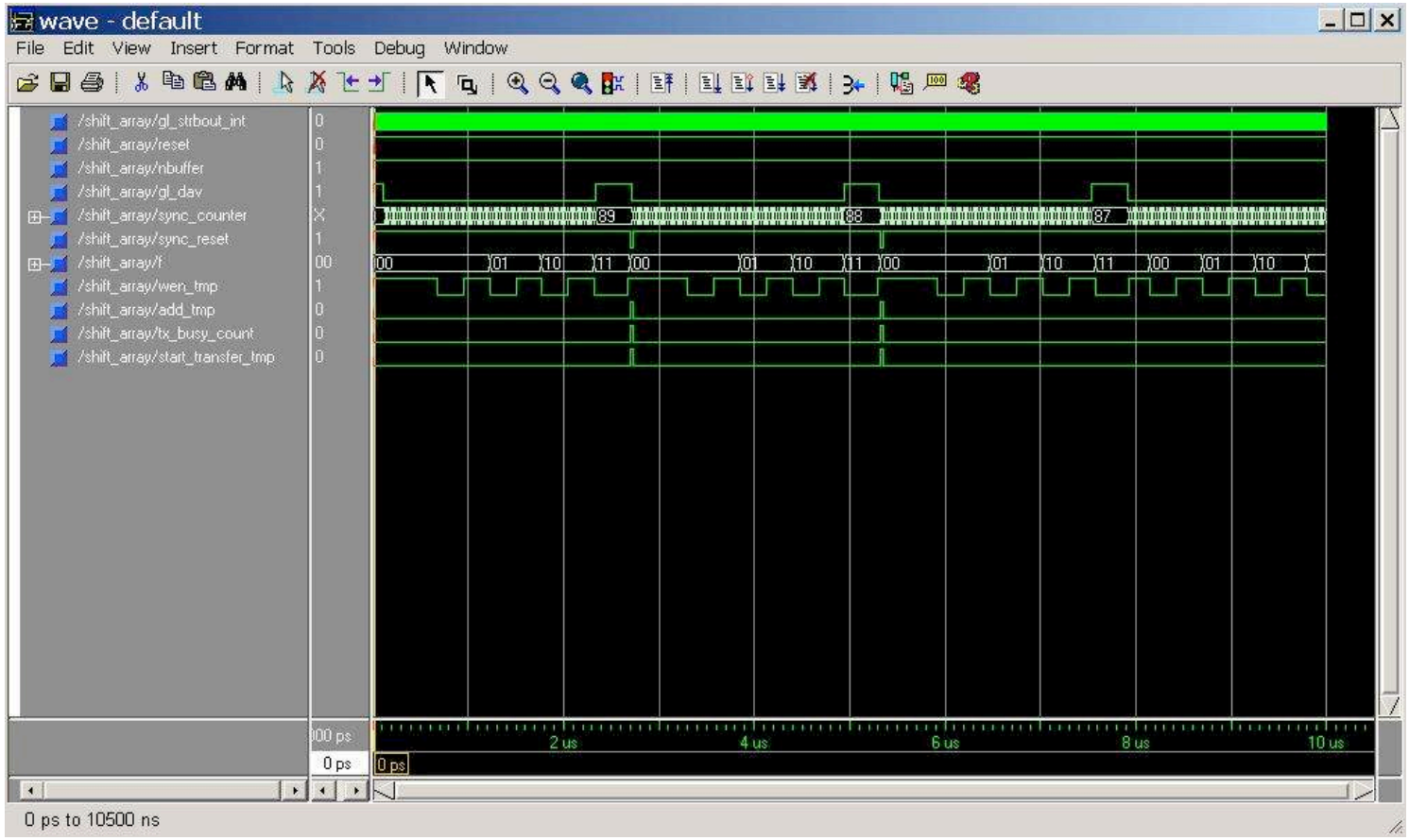
- JEM DAQ State Machine with 21 ticks DAV GAP

State Machine Simulation 5



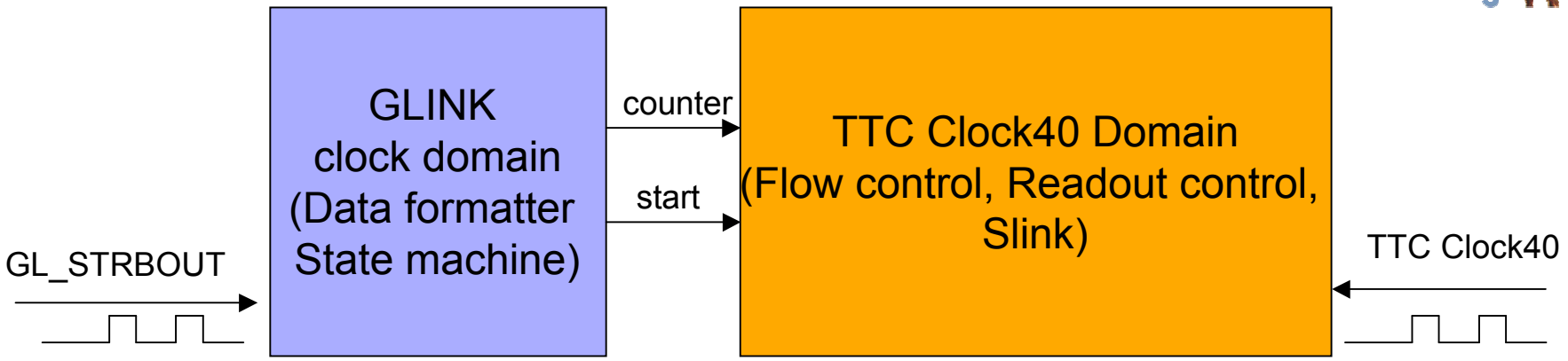
- JEM DAQ State Machine with 16 ticks DAV GAP

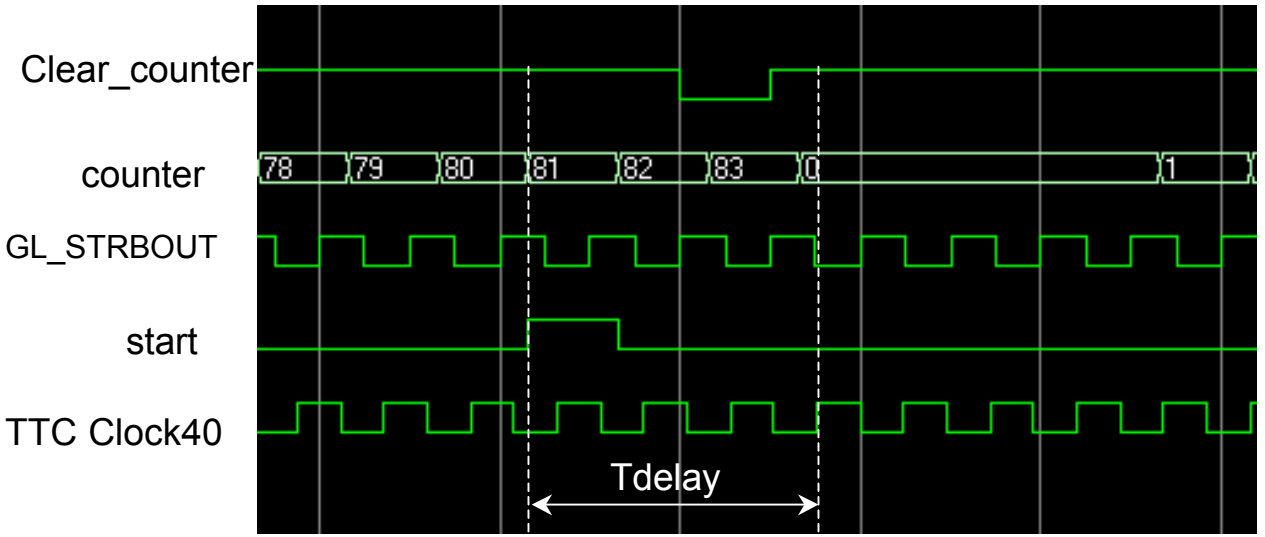
State Machine Simulation 6



- JEM DAQ State Machine with 15 ticks DAV GAP

Clock domains

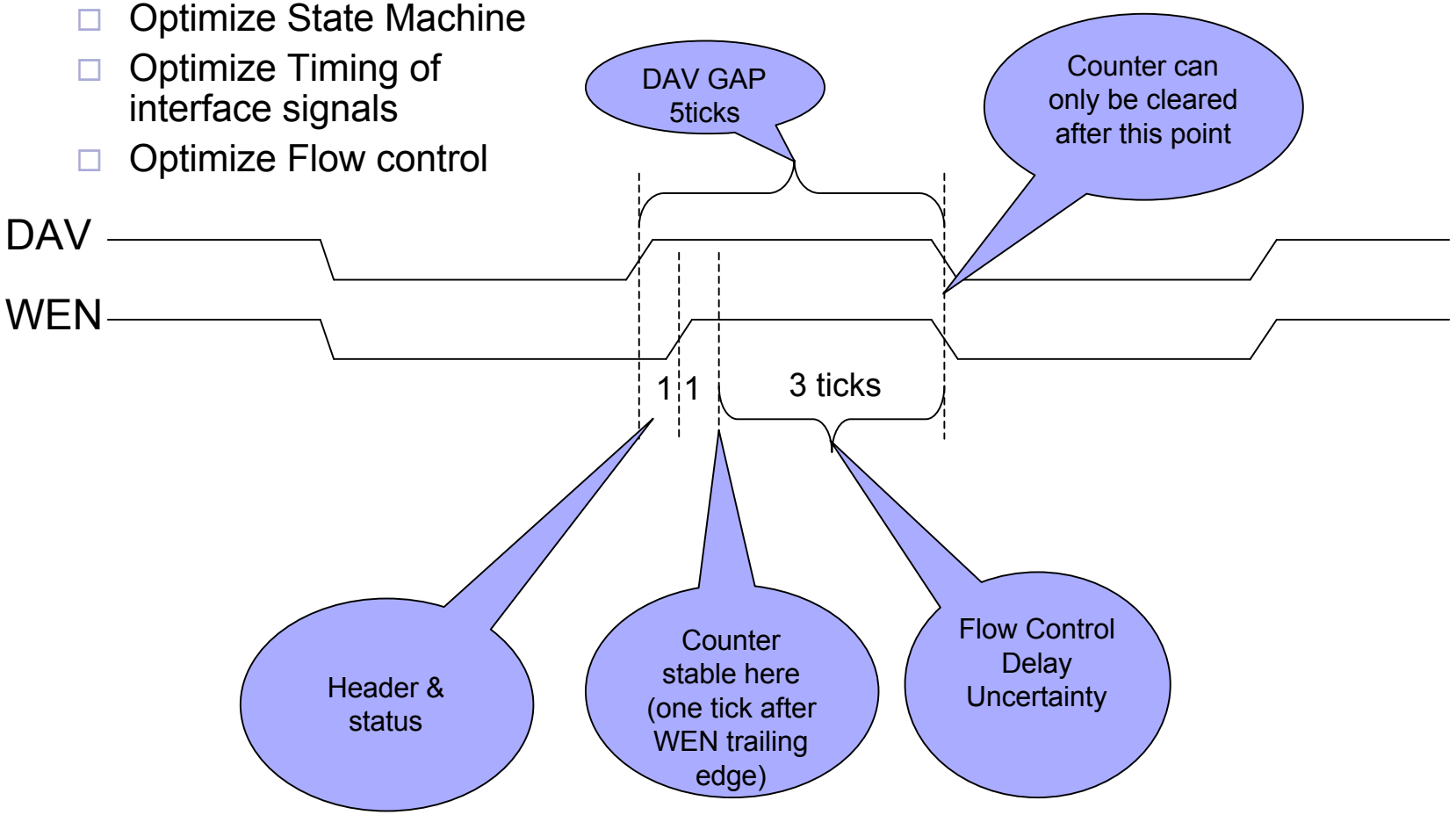




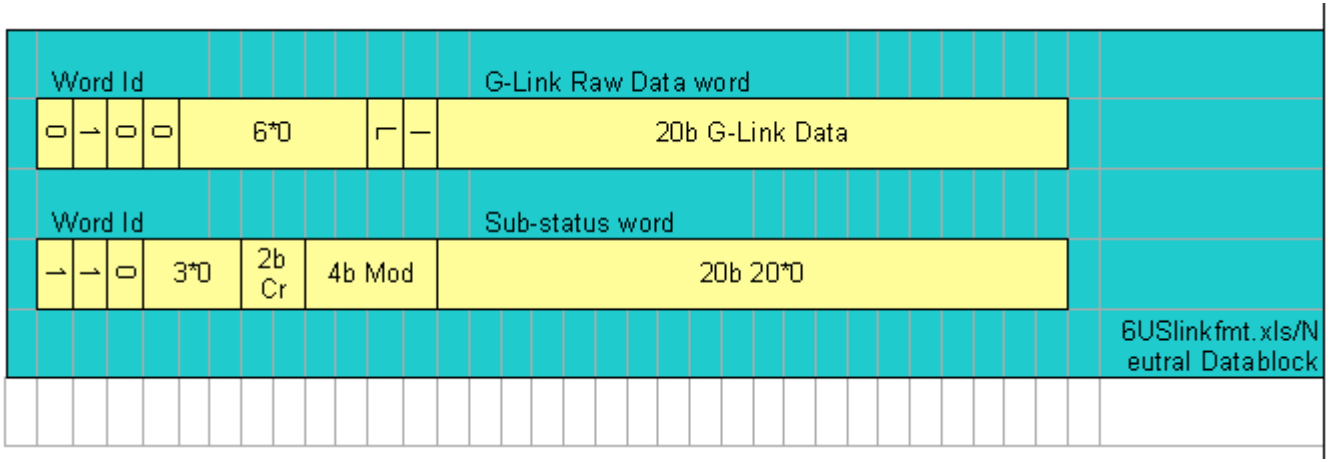
2 ticks of GL_STRBOUT < 3 ticks of clock40 < **Tdelay** < 4ticks of clock40 < 5 ticks of GL_STRBOUT

Minimum DAV GAP for CPM slice data

- Minimize the DAV GAP
  - Optimize State Machine
  - Optimize Timing of interface signals
  - Optimize Flow control



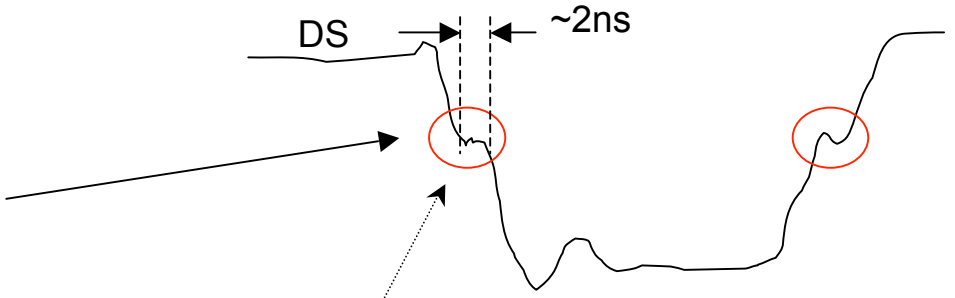
Neutral Format f/w



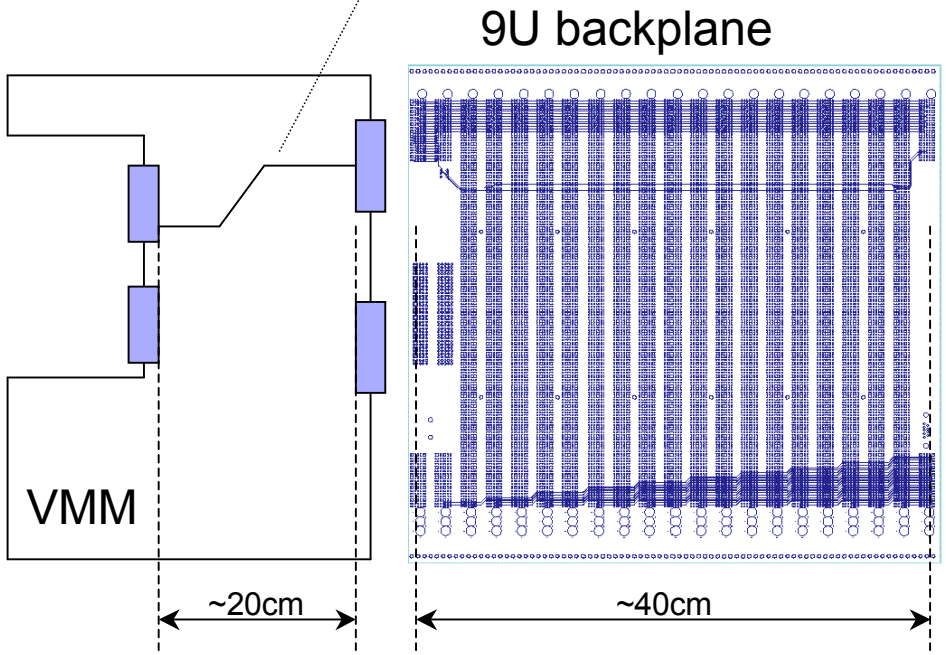
- Minimum DAV GAP
  - 5 ticks
  - Recommending 6 ticks
- Test results
  - Works with CPM_DAQ 1, 2 or 3 slices
  - Works with CPM_DAQ 4 and 5 slices
    - With new version of Controller f/w

VMM signal quality

- VME -- signal integrity problem
  - Edges of DS is not good
  - Small step within input transition area of TTL gate
  - Might cause double latch

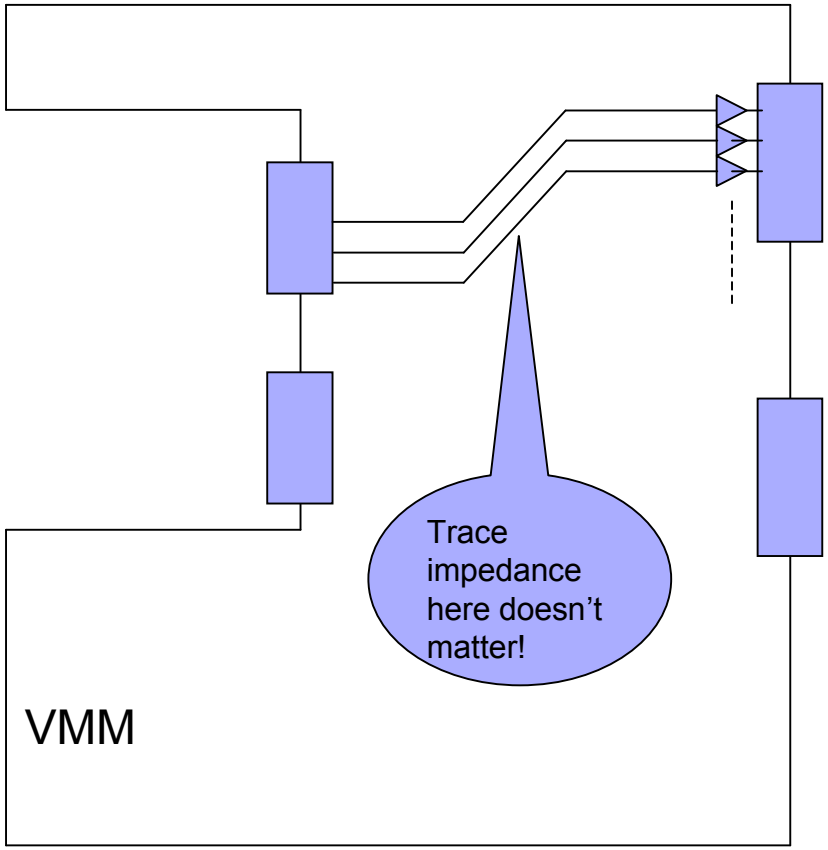


- Signal traces on VMM
  - Over 20cm
  - Impedance not controlled
  - Impedance on VMM can **NOT** match the impedance on backplane anyway
    - Due to load effect on backplane
    - Bare backplane impedance ~50ohms



VMM proposals

- Add buffers near backplane connector
  - DS
  - A01 — A23
  - DTACK
  - WRITE
  - SYSRESET
  - Possible for D00 -- D15
- Choose slower buffers
  - 74LS series instead of 74F series
  - Slower but smooth edge is better than faster but glitch edge
- Remove termination on VMM side
  - DS
  - A01 — A23
  - WRITE
  - SYSRESET



Old TTCDec reset and clock jitter

- To solve DSS clock unstable problem
  - Replace the flying wire from front panel to TTCDec
  - Add a “HUGE” capacitor to the TTCDec reset circuit
    - 5 ~ 10s reset constant, please wait patiently!
- CPM GLINK unstable
  - Old TTCdec clock is too jittery to be reference clock for GLINK
  - Redesign old TTCDec and add PLLs to filter clock jitter.
- New TTCDec address
  - Initial TTC address: 3FC0h, I2C address: 00h
    - Set by 100Kohms pullup or pulldn resistors on new TTCDec
  - Can be override with 4.7Kohms resistor
    - TTCrx output can drive 1.5Kohms load with only 80mV shift