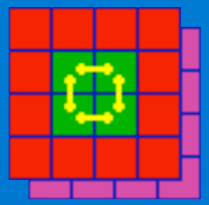
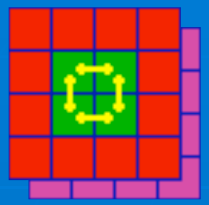


Testing & Integration

(An Overview)

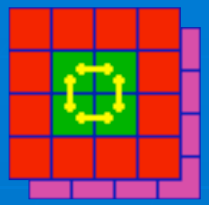
Current Status

Not all Song, Dance and Merrymaking



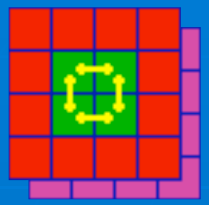
Overview

- Ongoing Sessions
- What has been Tested (2)
- Problems
- What needs Attention
- Strategy for the Future
- Wisdom from the Past



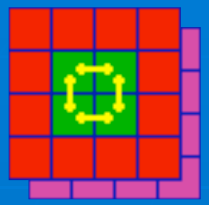
Ongoing Sessions

- For many months now
  - but intensifying.
  - Rhythm:
    - One week CPM:
      - Arrive Tues. Setup. Sort out s/w and d/b problems.
      - Continue Thurs/Friday.
    - One week internal test.
    - One week JEM.
      - Monday Afternoon arrival and setup.
      - Tuesday h/w, d/b and software problems.
      - Wed. Thursday. Serious test. Firmware development when necessary. Software innovation.
      - Friday Morning: Pack-up.



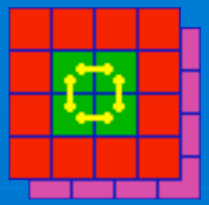
What has been Tested (1/2)

- Test infrastructure.
  - DSS GIO trigger input. Synchronous operation.
  - System control and simulation s/w.
- CPM.
  - 1,2,3. Mostly with internal playback as source.
- JEM 0.1, 0.2
  - Playback and DSS input. E, Jet f/w but not yet with Energy included. Nor RoI ROC. Support of short broadcasts a problem: use long broadcasts.
- CMM.
  - Hits, E. Various combinations of system, crate (with force-geoaddress)



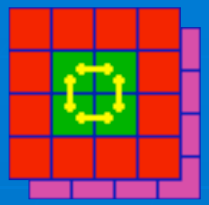
What has been Tested (2/2)

- ROD Readout.
  - Hit and Miss. Various combinations CP/CMM, CPM (DAQ/ROI), CMM e/gamma. JEM DAQ. But not consistently with more than one.
- Backplane.
  - VME--. VME signal integrity. Not systematically slot-by-slot. Loading up to 8 slots.
- TTC.
  - Effect of B-channel loading (started in Birmingham.)
  - Clock jitter. Needs systematic tests.
- ROS.
  - SSPCI: 3 RODS with CMM, CPM-DAQ and CPM-ROI
  - HOLA/FILAR: one link so far
  - s/w needs integration.



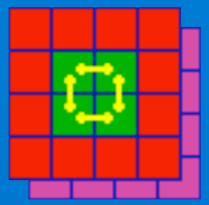
Problems

- When to find the time to:
  - Pursue software development and integration.
  - Make upgrades of Linux, Online-s/w, Dataflow-s/w.
  - Make formal releases.
- How to assure:
  - We come back to where we left off (tests.)
  - We don’t forget what we’ve learned.
- Are we close enough to the RT path?
  - L1A effectively allows us to sample the state of the system.
  - What about synchronous RT test of CMM output to CTP?



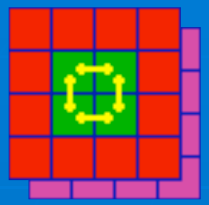
What needs Attention

- Calibration. Run Stepping.
- Test Phase Space:
  - Definition
  - Mapping
- ROS Integration
- Systematic soaking.
- “Check lists”
  - Per module
  - Per subsystem
- Qualification programme.
  - What info is required for FDR.
  - What info is required per module in production.



Strategy for the Future

- Combined Sessions (JEP +CP)
- 6U Rod Firmware.
  - Consolidation and remaining CMM (JEM Hit/Roi. Energy Hit/RoI)
  - Migration towards 9U formats.
- New Modules:
  - Preprocessors
  - CPM and JEMs
  - And Monster RODs:
    - 3-man f/w development collaboration. Will require collaborative design, code-management (repository) and extensive simulation in the sensitive phase spaces (flow control, time-domain matching, etc.)
- How does the test beam fit in to all this:
  - Are the impedances matched?
- Is there life after the test beam?
  - Towards Installation and commissioning.



Wisdom from the Past

Phylogeny recapitulates ontogeny…

Or was it the other way around?