Cluster Processor Modules Testing

Uk Meeting, Friday the 6th of February 2004

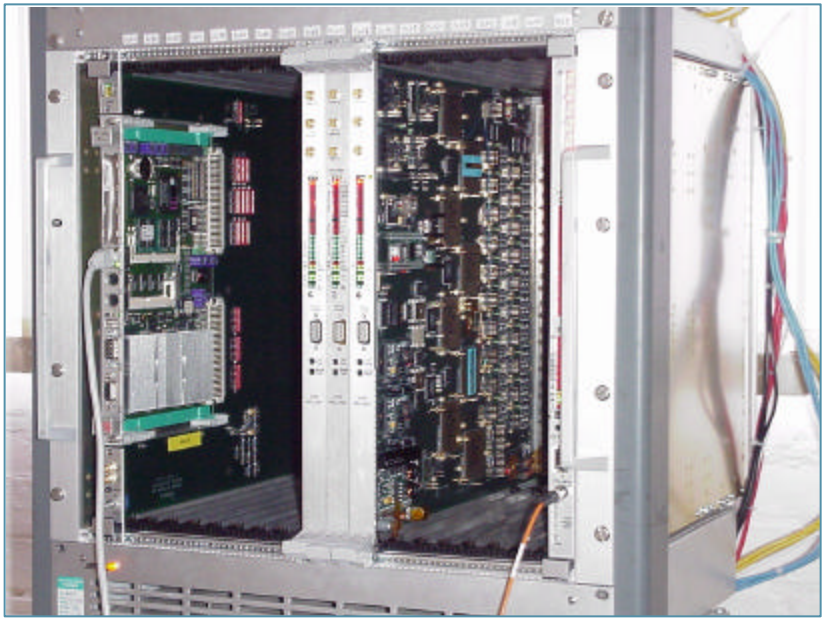
Three CPMs under test

Problems Found:

- Parity Error
- Glink lost locked
- VME Access
- CP Chip misbehaving

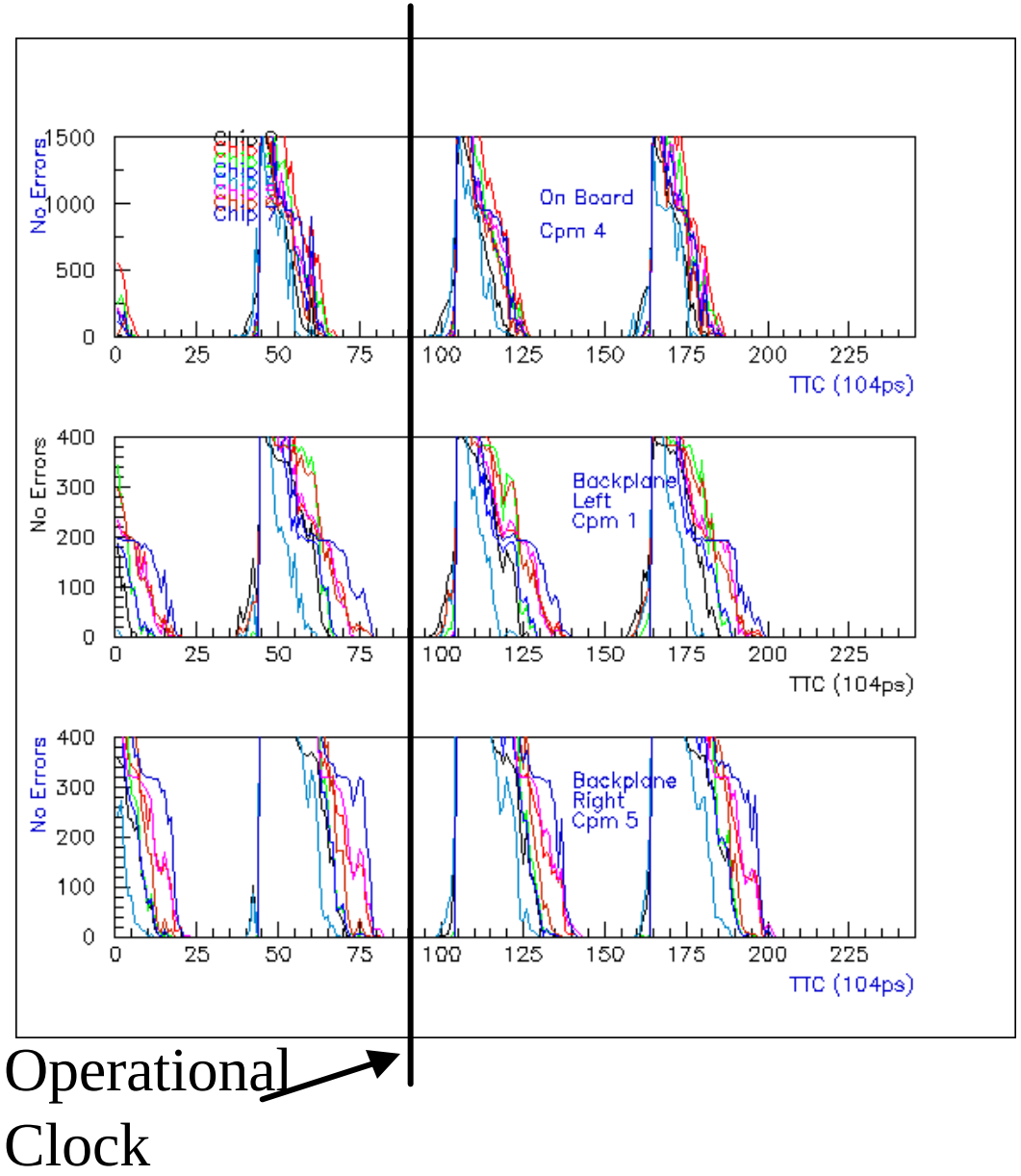
F/W upgrade:

- Min delay between DAV
- Constant BCN



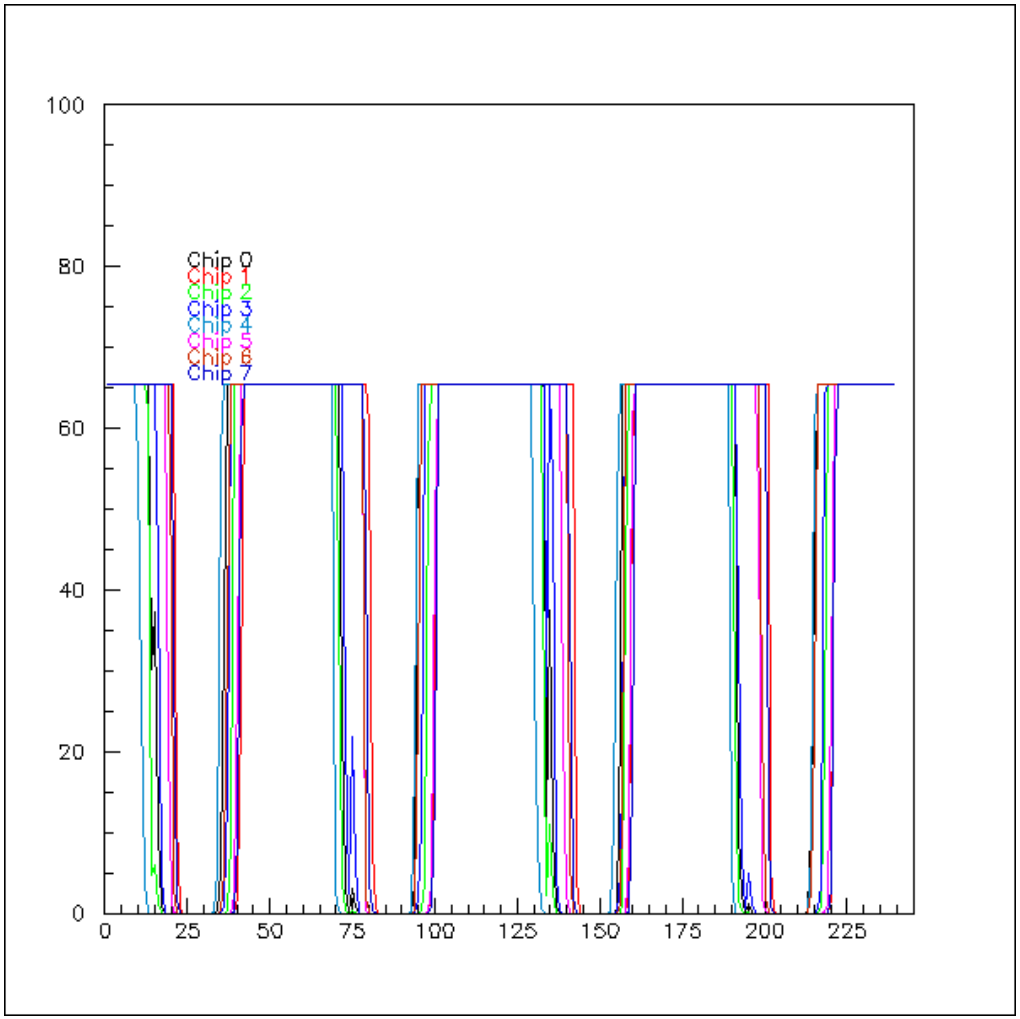
Backplane Scan with 3 CPMs

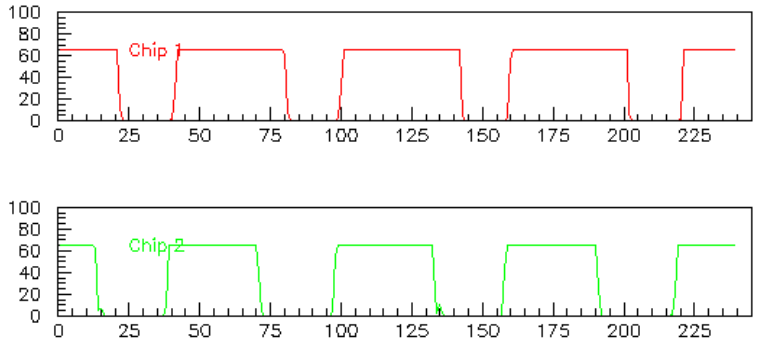
- ScanPath Mode used
- Scan taken at RAL
- Clock Timing set relative to Middle Cpm :
  - Cpm Left: - 104 ps
  - Cpm Right: + 1040 ps



3 CPMs Parity Error Scan

- Parity error are counted in the CP algorithm F/W
- Front LeD reds when parity error detected on input CP chip
- “parity error free” timing windows reduce to 400 ps, nearly 1 ns at the chip level

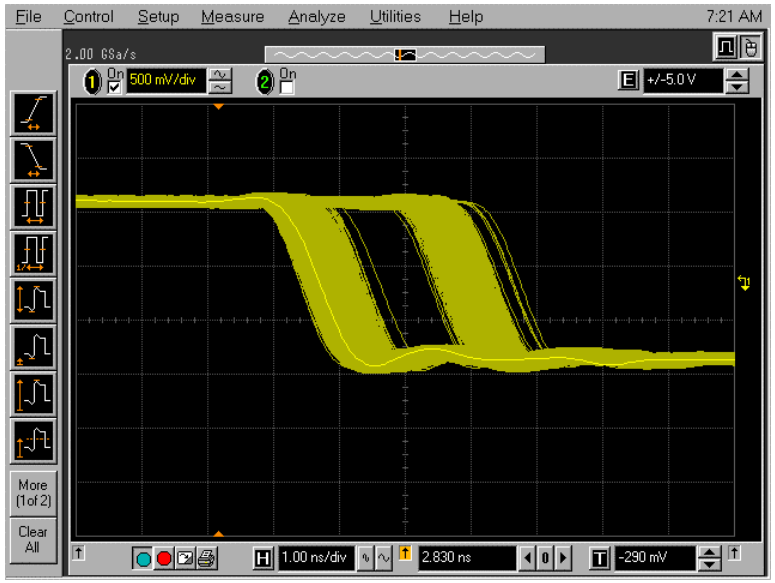




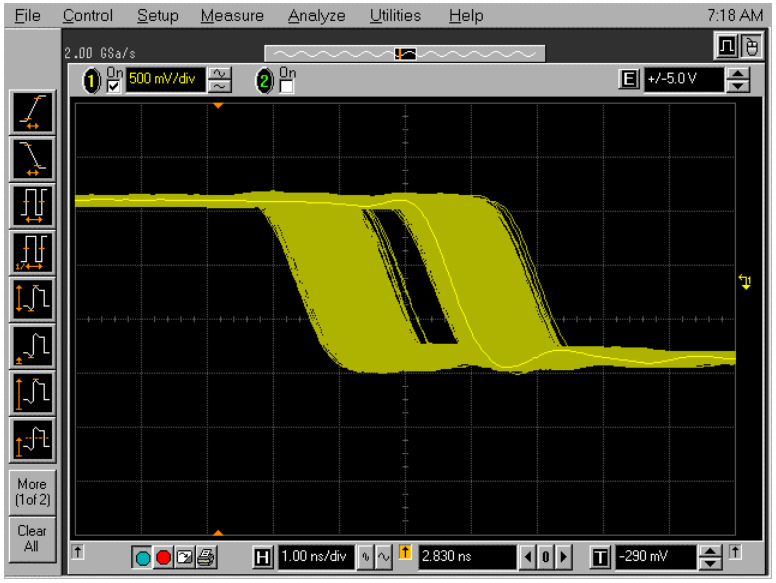
Readout : Glink Lock Lost

- As soon as we've got 2 Cpms on adjacent slot, Glink lost its locked signal
- Depend of the TTCdec card
- Due to jitter on Clock?

See shoot of Glink data->



No L1A



With L1A

CP chip behavior on “Stop” Broadcast

- After Stopping a run, i.e. sending broadcast command 0x00, all CP chips belonging to one CPM generate Parity Error
- Somehow the CP chip ignore its delays setting, but recovered them immediately after a CP Reset
- Problems seen if CPM5 involved
- CPM5 was created VME problems at RAL …see next slide

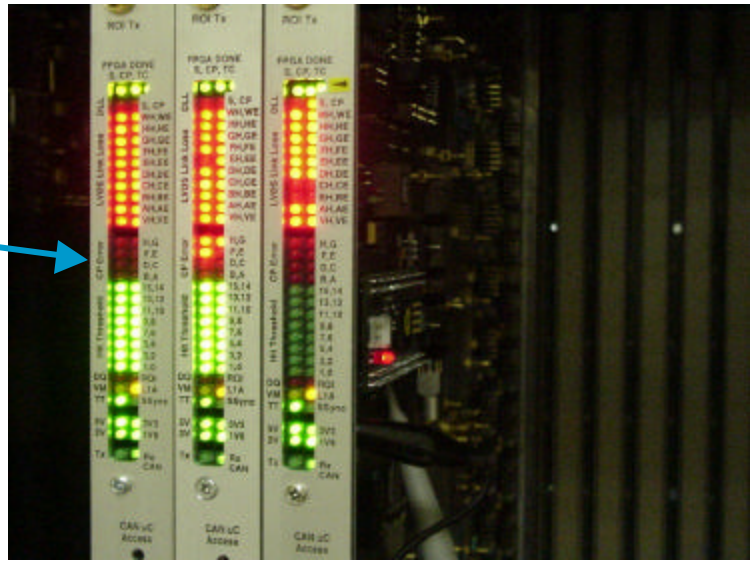
VME Problem on CPM5

- When addressing VME space not belonging to CPM5, CPM5 was immediately asserted a DTACK (VME Data ACKnowledge) signal
- Problem seen at RAL but not seen once the board was back at B'ham…
- ..and back at RAL, the problem disappeared
- Could the problem be related to the CP chip behavior now observed?

Status with 3 CPMs: Real Time

- Three CPMs can shared their data successfully across the backplane,
- Working timing window around 400 ps
  - Parity error check need further measurement, data used were not stressing all CP input channels

Parity Error



Status with 3 CPMs: Readout

- F/W modification to accommodate RoD:
  - Min. delay of 3 ticks required between 2 consecutives DAV
  - BCN constant between slices
- PLD Modification
  - To start/stop playback via same command as new Dss command “0x40”/”0x80”
- DAQ Run works
  - Run for 1 h so far, need longer run
  - Work at different L1A speed and different number of slices except for 5 ticks between L1A, BCN number wrong
- RoI Run works but Glink lost their lock quickly
  - Can manage to do long run of 15 min
  - Different Glink driver part