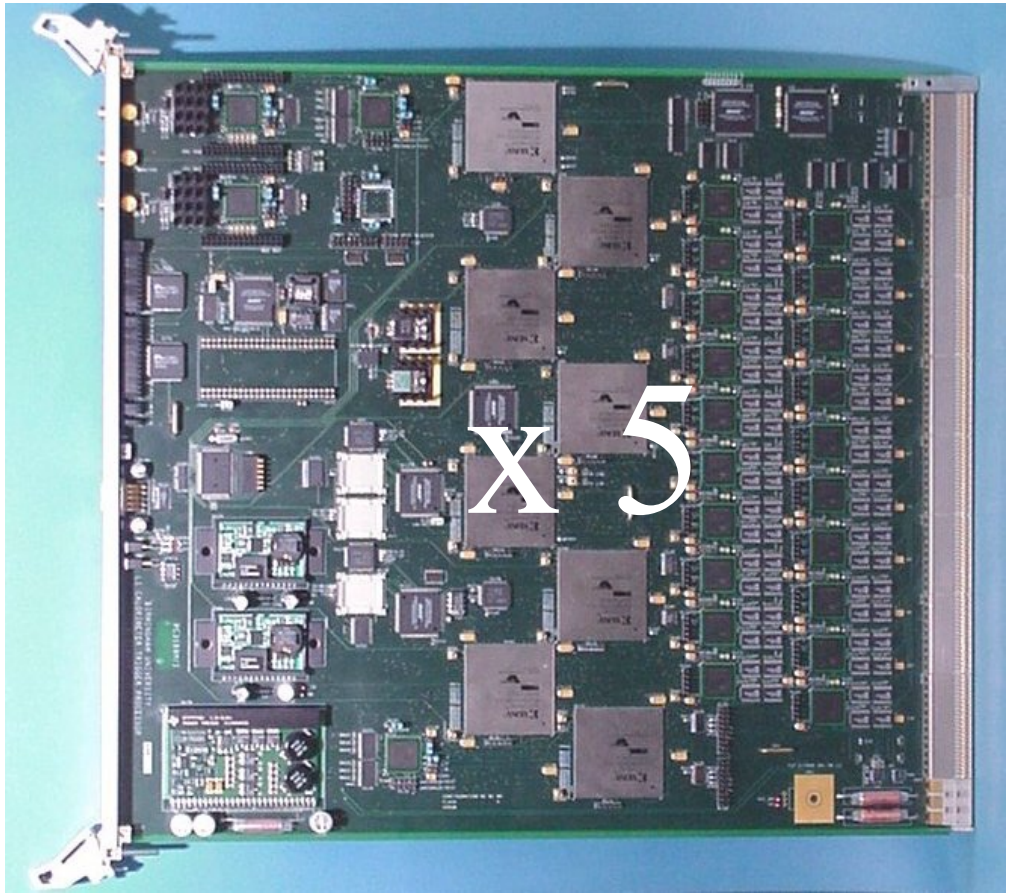
CPM Prototype Hardware

Hardware Status (1.0)

- CPM#5
- G-Links
- TTCdec
- Jitter

Next Version (1.5)

- Reminder
- Timescales
- Summary



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Hardware Status (1.0)

#1 - Assembled and fully working

#2 - Assembled, but assembly defects with 4 CP FPGAs .
Used for driving data onto backplane.

#3 - Assembled, but assembly defects with 5 Serialiser FPGAs .
Being used to test onboard CAN uC at RAL.

PCB Surface finish Tin , was Gold / Nickel

#4 - Assembled and fully working.

#5 - Assembled reworked and fully working…

CPM#5

A number of LVDS links were unstable. 24 RXs found to be of earlier revision. Now replaced , all LVDS links are now stable.

Problem with spurious (strange) VME response in RAL crate. Nature of fault suggests bad supply connection to CPLD, or fault within device. CPLD verifies OK.

CPLD reprogrammed and fault has dissapeared.
CPLD package examined, no assembly faults. ?

G-Links

G-Link TXs were unstable when CPMs placed together.

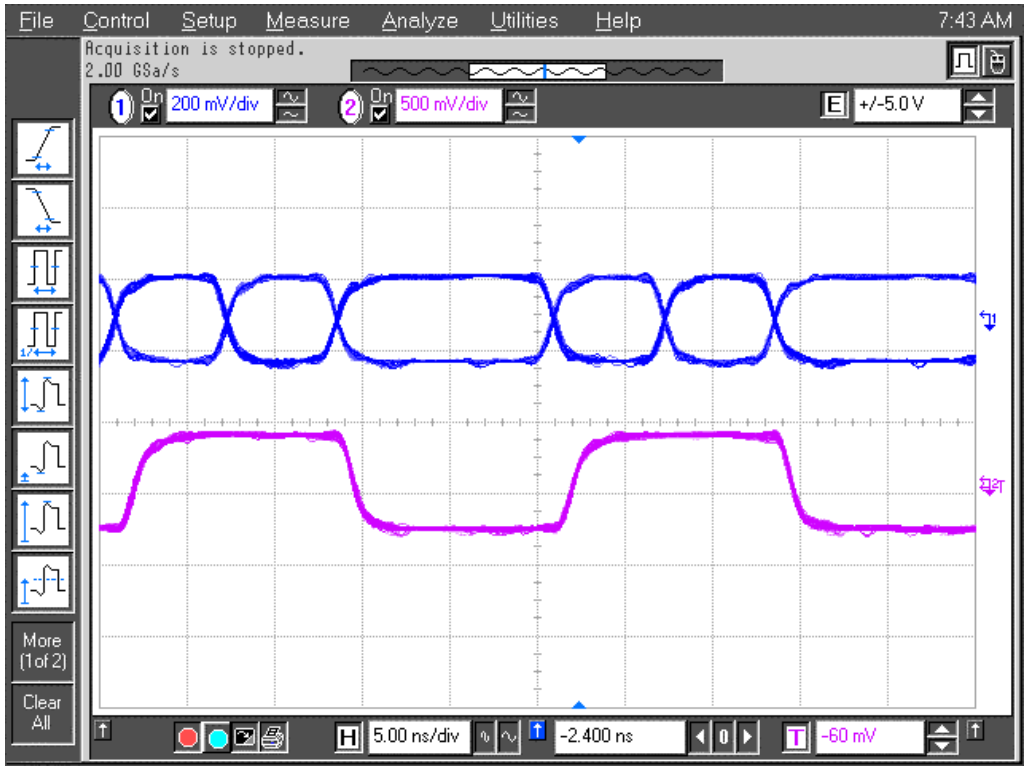
CPM (1.0) Vtt oscillation cured. G-Link TXs stable, but …

Still a problem with Glink. RXs lose lock more frequently when:
CPMs are adjacent
L1As are sent

CPM (1.5) Vtt different circuit, isolated from 5V.
G-Link Tx supply + extra filtering.
Improved TTCdec.

TTCdec

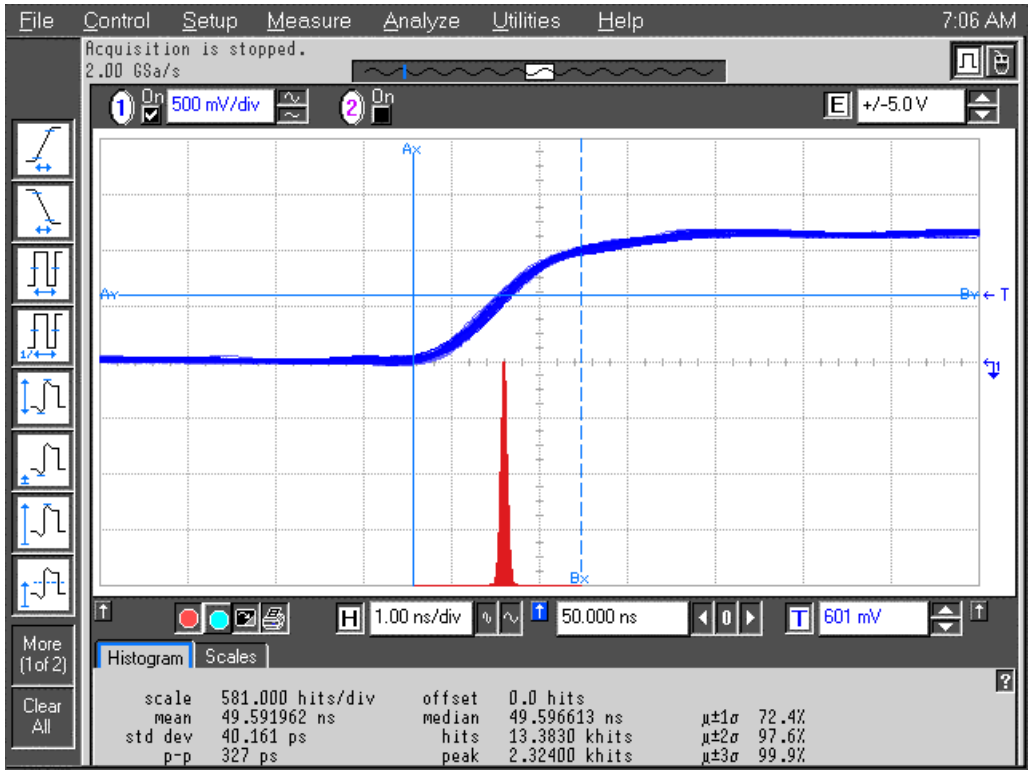
input waveform seems clean…



TTCdec in

TTCvx out

CPM 40 MHz Clock out



'Cycle-cycle' Jitter = 327ps p-p

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CPM Jitter measurements

	'Cycle-cycle' p-p / ps
TCM out (fp)	**218**
TTCdec in	**273**
TTCdec out	**291**
PLL out (fp)	**327**
GLink out	**218**

CPM Jitter measurements

	@ 50ns p-p / ps	@ 1us p-p / ps
TCM out (fp)	**218**	**564**
TTCdec in	**273**	**853**
TTCdec out	**291**	**1218**
PLL out (fp)	**327**	**1218**
GLink out	**218**	**873**

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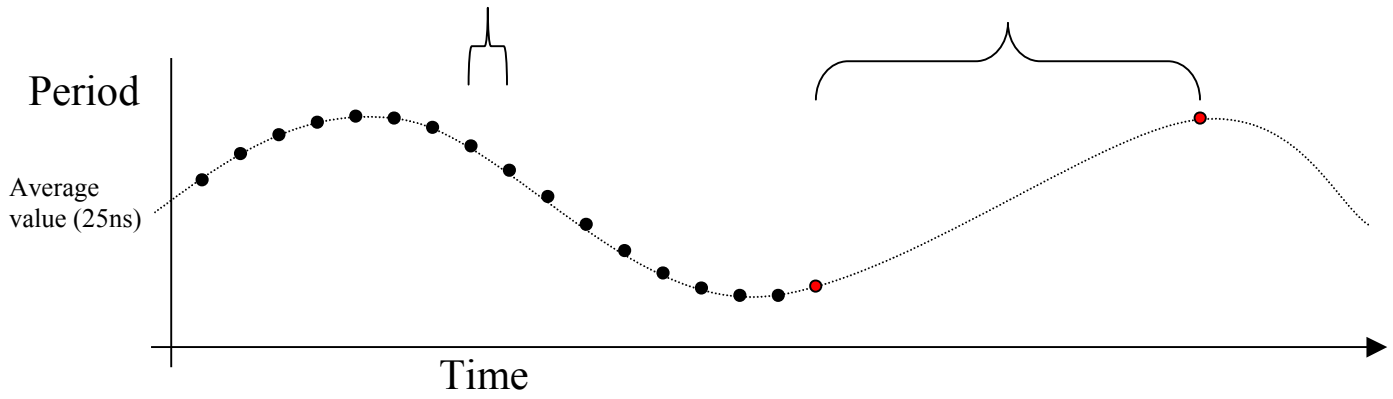
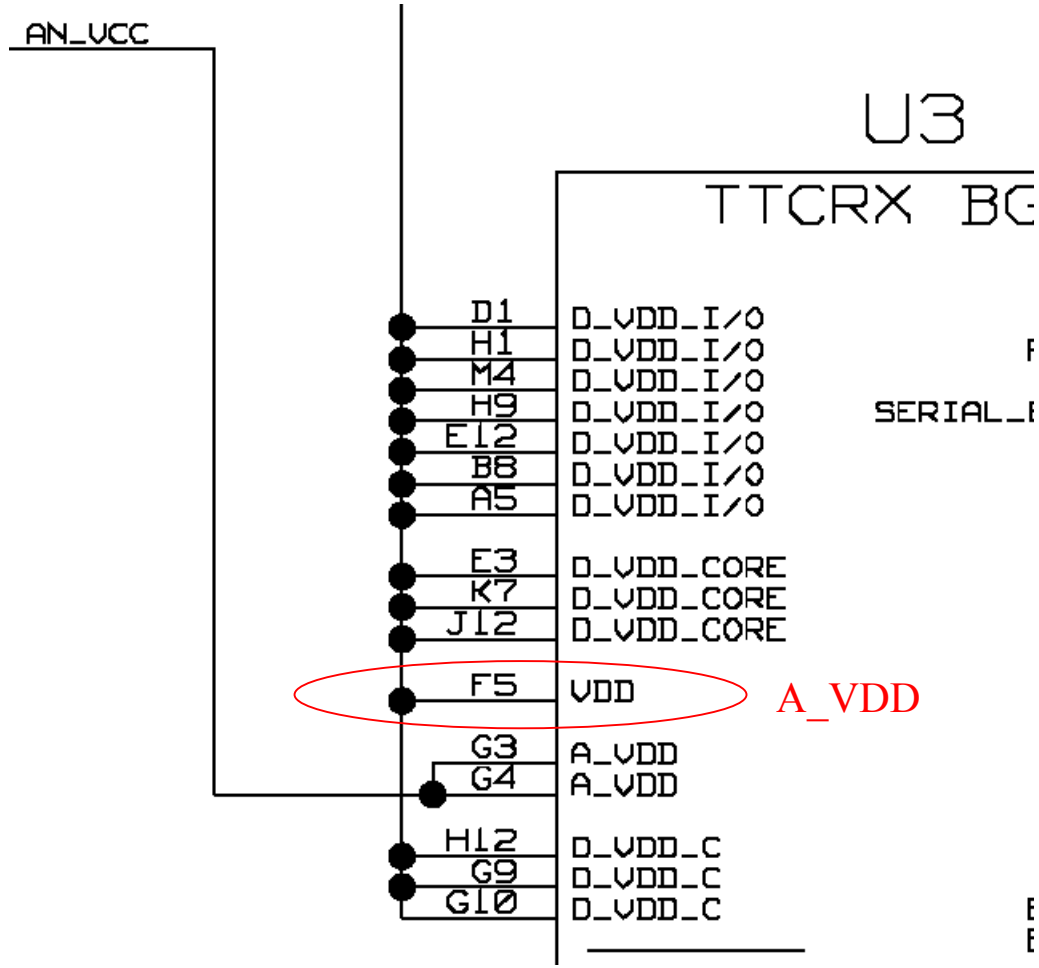


TTCdec on present CPM version:



Reminder(1)

CPM1.0 is a "Prototype module designed to production specification"

CPM1.5 is CPM1.0 with 'minor' changes.

Mechanical bracing
CP chip calibration was removed
Clock distribution tighter
Signal layout improved.

Still a prototype. Not yet ready for production.

CPMs old & new

Next version will be fully compatible with present hardware (CPM/CMM/TCM) CMOS I/O , GLink etc.

Existing FPGA Firmware can be used without modification on next version PCB.

One CPLD needs a minor change for it to work on both versions of PCB. All other CPLDs will remain the same.

Reminder(2)

Firmware for CPM(v1.5)

CP FPGA needs an update to split the "Backplane FIO " clock from the "Hit merger" clock, ie decouple the input and output timings.

CP and Serialiser I/O eventually needs to be changed to SSTL2 levels.

Timescales for CPM(v1.5)

Layout was finished just before XMAS.

Gold or Tin plating ?

Assembly company to take responsibility for PCB

Thanks to Viraj , Tony …

Contract for 2 Assembled CPMs (HAL Tin) placed (today?) with DDi.

Assembled CPMs expected mid-March.

Summary

- CPMs (v1.0) #1 , #4 & #5 working well.

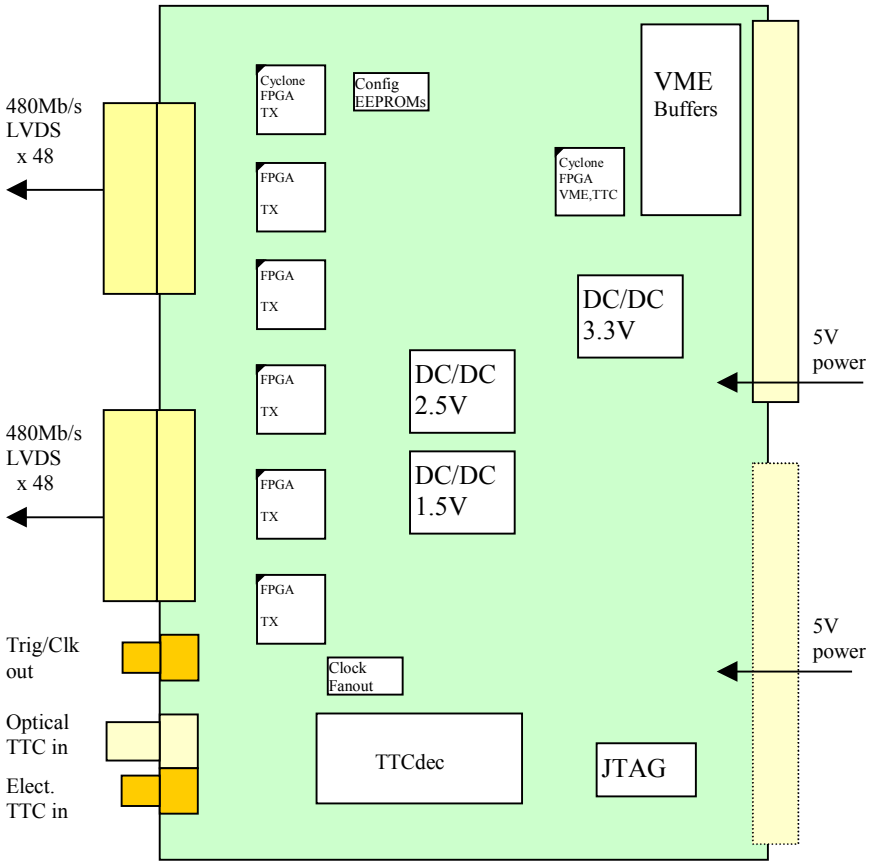
Need to understand problems with GLinks and TTC

- CPM (v1.5) layout finished. Expect delivery mid-March

To be debugged and tested by mid 2004.(FDR)

and finally…

LVDS Source Module



LSM 6U VME format

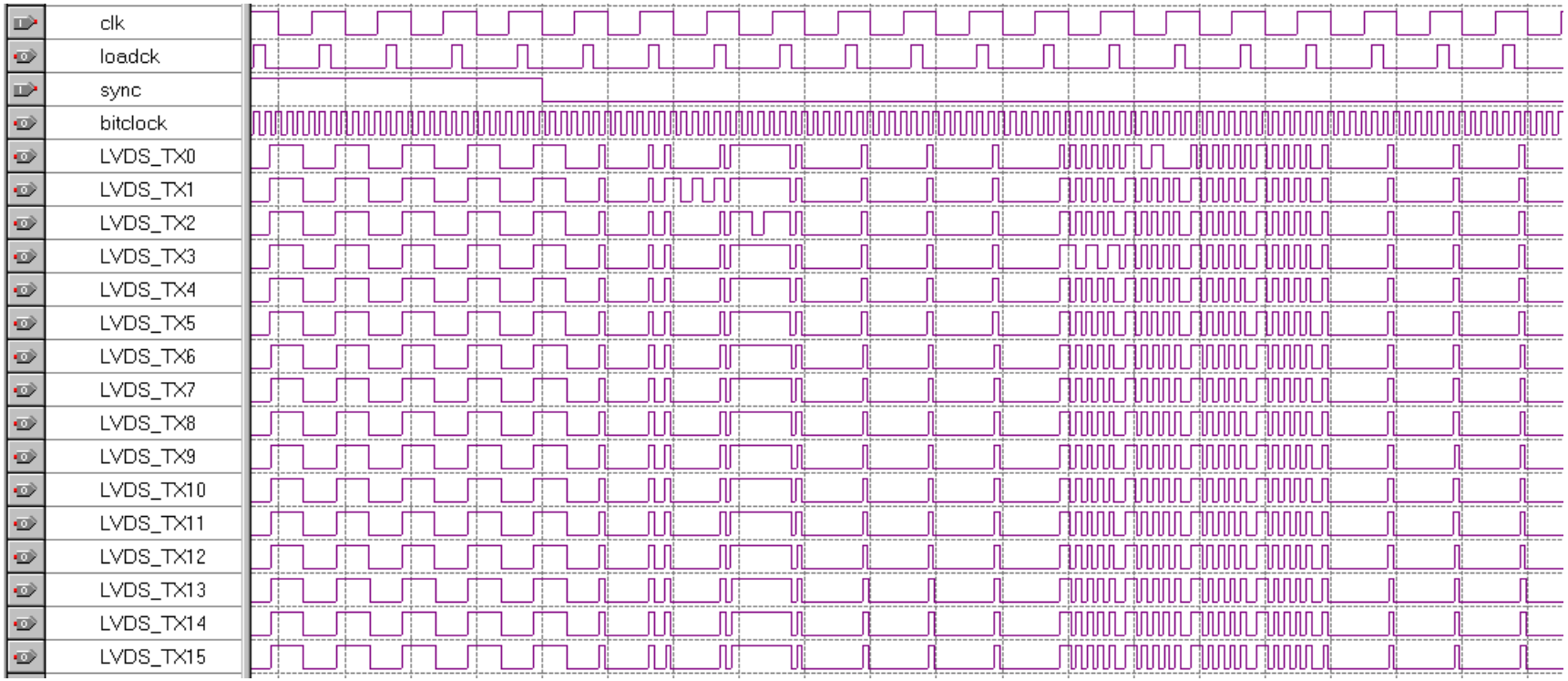
6 layers , 7 BGA packages

Can RAL Drawing Office help with library and layout work?

March / April would be useful.

LSM

Tx FPGA simulation:



16 LVDS channels @ 480Mb/s

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