ATLAS T1

TTC Clock Jitter

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TTC Clock Jitter test results from FEB

1. GLink data rates and reference clock jitter requirement
   - Unfortunately, no reference clock jitter specification for Glink chipset HDMP 1022
   - FEB: 1.6Gbps
   - L1calo DAQ: 0.96Gbps, presumably less stringent jitter requirement than FEB
2. Deterministic Jitter observed: ~0.2UI (120ps)
3. Main jitter source is identified as the TTCvx itself.
   - Mainly low frequency jitter (below 600KHz)
   - Modify the power filtering for TTCvx
   - Jitter improved, but very little
4. Change PLL current setting within TTCrx
   - Affect the clock jitter
5. Using TTCex as TTC source
   - Much better jitter performance than TTCvx
   - Many FEBs output a sufficient low jitter clock suitable for BER 10^{-12}
6. TTCrx with QPLL
   - Jitter improved, but not dramatically
   - On the other hand, small jitter difference translates into big difference in BER
7. What BER do we need?
   - 10^{-12}
   - Soak test with readout Glink is needed to qualify MARK 3 TTCDec as GLink reference clock at such a BER.
8. Mark 4 TTCDec with QPLL
   - Confirmed better clock jitter performance
   - Dramatical changes needed (card space, clock signal logic level, etc…)

Jitter measurements of FEB

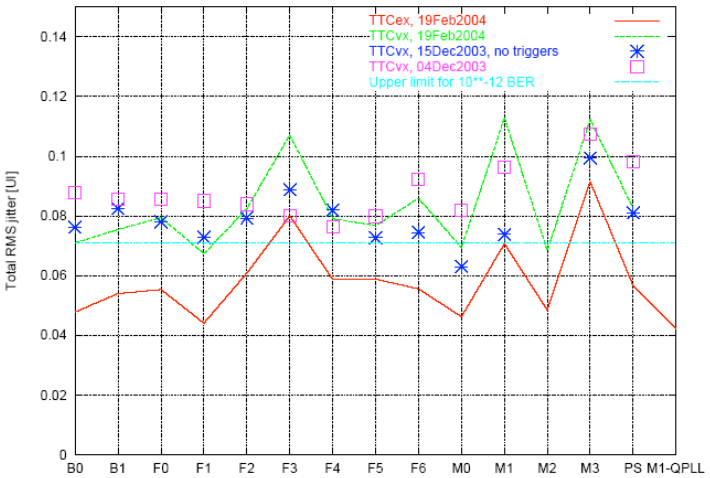

Figure 4: Estimate (pessimistic) of total RMS jitter as seen by the HDMP-1024. Total jitter is obtained by adding in quadrature the weighted spectral estimates of the TIE without correcting for deterministic jitter.

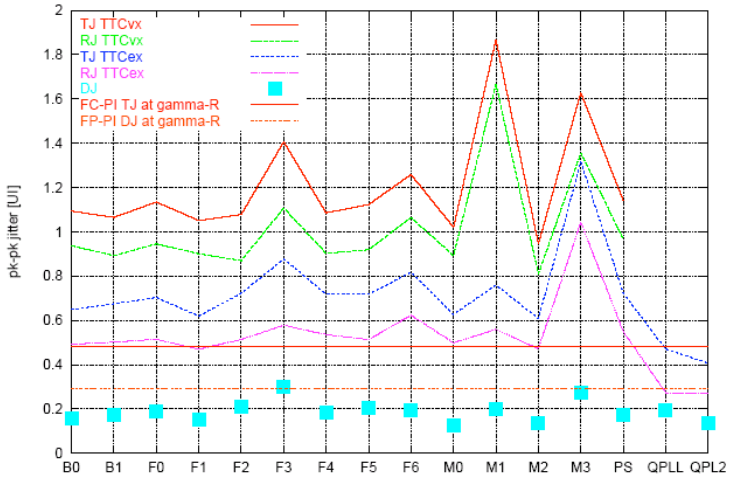

Figure 10: FEB optical output jitter (measured at point γ_R) calculated using a 625 kHz single-pole highpass filter. The peak-to-peak random jitter is calculated for a BER of 10^{-12}. TJ stands for total jitter, DJ for deterministic jitter; and RJ for random jitter.