# Minutes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 1st September 2005


***Birmingham:*** **Dave Charlton*, Stephen Hillier, Richard Staley, Peter Watkins**

***Heidelberg:*** **Victor Andrei, Florian Föhlisch, Paul Hanke, Eike-Erik Kluge, Victor Lendermann, Karlheinz Meier, Frederik Rühr, Hans-Christian Schultz-Coulon, Pavel Weber**

***QMUL:*** **Eric Eisenhandler****

***RAL:*** **Bruce Barnett, Ian Brawn, Tony Gillman**

***Stockholm::*** **Christian Bohm, Sten Hellman**

**at CERN*

***at RAL*


## *1. Birmingham*

- The RPPP schematics designs are all complete and in the RAL Drawing Office awaiting the start of PCB layouts.
- The design of the TileCal cable test rig will be completed during the next three weeks.
- The design of the JTAG-based Patch-Panel test rig is almost complete, and will also be finished before the end of September.
- The bare PCBs for the pre-production CPMs will be completed next week, and the first two assembled modules should be ready for testing by the end of September.
- Dave Charlton summarised the current status of the preparations for cabling installation in USA15:
    - The custom upper cable trays have been installed satisfactorily, and only need some minor cutting away of their side walls to provide sufficient clearance and access
    - The false floor panels have been cut with enclosed holes, which will need to be extended into slots to allow easy cable access
    - Hardware (cables, TCPP crate/modules, dummy TCPP panels and cable stocks, etc.) will be shipped from RAL to CERN at the end of next week, ready for Dave, Simon and Xen's visit the following week.
    - It is important that the order of sector cabling on the TileCal be determined very soon, so that the appropriate short cables can be installed first
    - The request for cable labels to be printed must be made by 12$^{th}$ September, in order to be ready for the probable start of cable installation on 14$^{th}$ September

## *2. Heidelberg*

- Two full batches of assembled MCMs have now been tested, with 900 passing successfully, representing an excellent 89% yield
- Ralf has started testing the third batch of MCMs, which so far has shown a 100% yield (27 good from 27 tested), and a web page has been set up to show the current status
- There had been a problem with the attachment of the brass lids, which Klaus has now solved by soldering locally just at the edges, and Hasec will use this technique for their assembly of all the remaining MCMs
- The six more ASIC wafers that were fabricated at the X-Fab foundry two months ago have now been tested, yielding only 35% good dies, although this exercise has provided ~400 spare chips

- The PPM had exhibited some VME problems when last tested at RAL, and finding a solution to these is urgent as it prevents further integration tests, e.g. verifying correct operation of the new LCD design

### *3. QMUL*

- Eric noted that the PRR for the CMM cannot be formally signed off until a small number of the final recommendations have been addressed

### *4. RAL*

- The PCBs for the pre-production TCPPs have now been fabricated, but final assembly of the first five modules awaits the delivery of connectors
- As soon as the deeper side panels arrive, the best depth for the TCPP crates will be determined, and the three remaining crates will be ordered for direct delivery to CERN from the Swiss factory
- Components for the production CMMs have been ordered, and the updates to the schematics and layout are in progress
- Following some minor layout iterations, two further ROD modules have been ordered
- All components for the production RODs will be ordered next week, although uncertainties about the size of the code for the compressed PPM data mean that the FPGA size is still indeterminate
- The schematics for the production VMM have been updated, but require a final independent check
- The specifications for the production TCM are being finalised

### *5. Stockholm*

- A new tender for the Processor Backplane (PB) production is being prepared, and a draft plan to determine the appropriate acceptance test procedures for the 10% trace impedance tolerance now exists
- It was noted that for the CMM a PCB trace impedance tolerance of 5% was offered by the PCB manufacturers at only a modest incremental cost
- The delay to the PB production implies a delay in assembling the final Processor crates in Stockholm
- The pre-production batch of 400 LVDS cables will be delivered to Stockholm at the beginning of October, with the remainder expected the following month. Acceptance tests for these cables are still to be defined as soon as possible

### *6. AOB*

- Plans for the TileCal "Experts' Week" must be defined very soon, in order for flights to be booked. First preparations for the necessary infrastructure will start during the week beginning 12th September, and the main integration work with the TileCal group will take place during the following two weeks

**Next Phone Conference – Thursday 15th September 2005 at 10:00 *(UK)*, 11:00 *(Germany, Sweden)***

***Tony Gillman***