Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 3rd March 2005

Birmingham: **Stephen Hillier*, Gilles Mahout*, Richard Staley, Peter Watkins**

Heidelberg: **Ralf Achenbach, Florian Föhlisch*, Christoph Geweniger, Paul Hanke, Kambiz Mahboubi, Frederik Rühr, Klaus Schmitt, Pavel Weber**

Mainz: **Stefan Rieke*, Uli Schäfer**

QMUL: **Eric Eisenhandler**, Murrough Landon***

RAL: **Bruce Barnett*, Ian Brawn, Norman Gee*, Tony Gillman, Viraj Perera, Weiming Qian**

Stockholm: **Sam Silverstein**

**at QMUL*

***at RAL*

1. Birmingham

- Studies of the performance of the new CPM (v1.9) have continued. The addition of around 500 psec extra delay into the CP FPGA firmware has extended The parity error-free Backplane timing window has been extended to 2.0 nsec by adding a further 500 psec of delay into the CP FPGA firmware by moving the combinatorial logic block away from the I/O pins.
- The clocks from the TTCdec appear more stable when operating inside a room with air conditioning.
- Tests of the optical G-link output signals have been satisfactory; the links locked correctly and the received DAQ data agreed with simulation predictions. High-statistics runs will be performed at RAL.
- Tests were satisfactorily carried out using two LSMs as data sources connected to two CPMs via 15 metre LVDS cables. Broadcast commands worked correctly, and the CP algorithm was exercised with both CPMs exchanging their data via the Backplane. A scan revealed that the parity error-free window width was not reduced in the presence of Backplane LVDS activity.
- One remaining problem is that of parity errors being observed in the CMM when fed with real-time data from v1.9 CPMs. The actual data in the CMM spy memories are always correct, but the parity bit is always low. This is still being investigated.
- Design of the "other" Patch-Panels (Receivers→PPMs, not the TCPPs) is under way. (An appropriate name/acronym must be found for these boards.)

2. Heidelberg

- There has been some progress on trying to understand the poor yield of PPr ASICs. Ralf Achenbach visited the Fraunhofer Institute for discussions about QA issues of wafer production at the X-Fab silicon foundry. To help them identify the problem, they would like to obtain a more detailed breakdown of the PPr ASIC yield figures, as suggested by Philippe Farthouat at the recent PPr ASIC/MCM PRR, in order to isolate those failures relating to memory functionality, where ~100% fault coverage is provided.
- Information from AMS about the problems with the PPr ASIC fabrication is still not forthcoming, and there have apparently also been problems with fabrication of other ATLAS ASICs.
- MCM production is almost ready to proceed, and the first pre-production batch of 500 substrates will be ordered from Würth as soon as the full contractual arrangements are agreed between Würth and Hasec (KIP are no longer included in the legal contract).
- Another LCD card, with a modified pre-compensation network (similar to that used in the LSM design), has been tested at KIP. It will be tested with a CPM later this week at RAL, so that data

integrity on the LVDS links may be studied. If it provides stable, error-free link operation then another four (three?) LCD cards will be modified in the same way, to supply all the current PPMs. *(Note that the use of Virtex II FPGAs in this design will inevitably exhibit an intrinsic ~300 psec time skew between the two sides of the differential LVDS signals.)*

- It seems that true current-mode LVDS drive is not possible with the Virtex II FPGAs, as they provide insufficient current per channel.
- Simulation studies have been carried out using Spartan-3 FPGAs instead of the present Virtex II devices in the hope of removing the LVDS differential timing skew, but although some channels are skew-free others still exhibit skew.
- For the final production LCD card design, the goal would be to improve the layout by reducing the component density around the FPGAs, by using four instead of the present two devices.
- Whichever variant of these new designs is chosen, there will probably need to be a modified footprint for the LCD card connectors and hence layout changes to the PPM motherboard itself.
- 18 new PCBs for the latest 1-channel op-amp AnIn design are now available for assembly and test, which will be sufficient to populate all four of the current PPMs. Measurements indicate that inter-channel crosstalk is now much improved, and acceptable.

3. Mainz

- The design iterations for the latest JEM have been incorporated into the next version of the PCB layout, and the first module should be available in about one month from now.
- All components for the production JEMs which have a long lead-time have been identified, and hopefully can be ordered very soon. It is already known that some component types will certainly be used in production – *e.g.* the Backplane connectors – and so can safely be ordered now.
- The availability of System ACE chips is believed to be a possible problem.

4. RAL

- The PRR for the CMM was successfully passed on 28th February 2005.
- Adam Davis is updating the specifications for the CANBus implementation.
- There are long lead-times on some of the components for the production CMMs, *e.g.* PLLs.
- JTAG testing of the second 9U ROD has been successfully completed.
- The production TTCdec cards must be equipped with mounting holes, for secure attachment to all production modules.

5. Stockholm

- The draft Report from the Backplane FDR has been issued, and most of the design changes recommended have already been incorporated. It is expected that the final points will be resolved by the end of this week, and the production tendering exercise can begin. Once all the recommendations in the Report have been agreed, it will be submitted to EDMS.
- The seven water-cooled Wiener crates now at CERN will be shipped to Stockholm within the next week or so.

Next Phone Conference – Thursday 17th March 2005 at 10:00 *(UK)*, 11:00 *(Germany, Sweden)*

Tony Gillman