Minutes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 5th/12th May 2005*

Birmingham:	**Richard Booth**, Dave Charlton**, Stephen Hillier, Gilles Mahout**, Richard Staley**
Heidelberg:	**Ralf Achenbach, Paul Hanke, Eike-Erik Kluge, Kambiz Mahboubi**, Frederik Rühr, Klaus Schmitt, Hans-Christian Schultz-Coulon, Pavel Weber**
Mainz:	**Uli Schäfer**
QMUL:	**Eric Eisenhandler****
RAL:	**Bruce Barnett, Ian Brawn, Norman Gee, Tony Gillman, Viraj Perera, Weiming Qian**
Stockholm:	**Sten Hellman, Attila Hidvégi**

***at RAL*

**N.B. The Minutes cover both the meeting of 5th May and the meeting of 12th May, which had UK-only attendees as it coincided with a public holiday in Germany and Sweden.*

1. Birmingham

- Dave Charlton has spent some time at CERN last week gathering information on the analogue cable installation. He spoke with Luis Hervas regarding the assembly of connectors on to the long and short 16-pair cables, and to Bill Cleland about their proposed cable strain relief mechanics. Some of this will be followed up at the Installation/Calibration workshop at CERN next week. Vittorio Paolone (University of Pittsburgh), who is involved in the cabling mechanics, will attend this workshop.
- Gilles has made measurements of the parity error-free FIO windows on CPM v1.9, after adding a third strobe clock to the CP chips. The windows have increased from 2.0 nsec to 3.0 nsec when using the diagnostic scan-path firmware, but only to 2.2 nsec with the full algorithm firmware, which is not yet understood. He believes that further improvements from firmware are not possible, but the windows could be increased to a maximum of 2.7 nsec by adding on-board clock delays to selected CP chips.
- The SSTL2 signalling standard has been tested on CPM v1.9, and works well, although so far it has been tried with only the CP chip interfaces. SSTL2 levels on the Serialiser interfaces will now be tested as well. The overall effect should be to widen the FIO data timing windows, although the effect may only be small.
- Temperature studies on eight TTCrx chips (mounted on TTCdec cards) have been carried out, over the range 10 – 50 degrees Celsius. It is encouraging to note that Des1 and Des clocks track each other extremely well, both having a temperature coefficient of ~50 psec/degree Celsius, which agrees well with the quick measurements that Weiming made originally at RAL. Also, there was very little spread in this coefficient between the eight chips, which is also very encouraging.
- For two of the TTCdec cards intended for these tests, it was found impossible to enable the Des2 clock. Philippe Farthouat suggested that a floating JTAG input pin might cause this problem, so this will be checked.
- The seven different types of Patch-Panel (TCPP and six flavours of RPPP) are almost ready to go to the RAL Drawing Office for layout, with slots already reserved for mid-June. The TCPP needs some minor design iterations, as the TileCal group have requested that a sixth muon trigger signal be accommodated on each of the Barrel input cables, and there are also some changes to the grounding scheme. Bill Cleland will send details of the part numbers for the 37-way sub-D connector used in the Receiver modules, which will then also be used for all of the Patch-Panels.

2. Heidelberg

- All of the ASIC dies are now at HASEC. When the MCM substrates also arrive (~now), MCM assembly will begin.
- The test and database software is ready for the first batch of 500 assembled MCMs, as required for the tests demanded by the ASIC/MCM PRR.
- The re-designed LCD card is being sent out for manufacture ~now, and will be back at KIP for assembly by Klaus (~two days) in ~two weeks time.
- A batch of 500 PHOS4 dies has been ordered, for which the mask set is expected in about one week from now.
- There is no further news from AMS about the reasons for the low-yield wafers.
- Kambiz and Florian have made good progress so far with the PPM readout tests at RAL. The readout links are stable, but the data packets are very often too long, although the data appear broadly correct. The problem is not believed to be caused by hardware, and it is expected that a solution involving firmware modifications only should be possible.
- The readout is currently limited to a low L1A rate, with a minimum DAV gap of 760-780 ticks, so more work will be needed to establish the full L1A rate, but only after reliable error-free readout has been demonstrated at low rates.
- Bruce is writing some software to present the output data packets in a user-friendly display format.

3. Mainz

- JEM1.1 is back from the manufacturer. Tests won't, however, be possible until the control daughter module (4-layer board) is available. That will go into production starting 6th May (7 working days for PCB production).
- Signal integrity measurements have been carried out on JEM1.0 FIO, with maximum FIO activity on three JEMs and one signal probed. Considerable noise levels have been observed, and also signal distortion apparently due to wrong DCI driver impedance control. The problems are now being studied in detail. So far there is no hint at any problems related to JEM main board or backplane connection.
- Corrections might be necessary to the DCI parameters for the Input daughter modules, probably by means of different DCI reference resistor values.
- It is not understood how the maximum spike on the nearest neighbour signal line is induced, not at the time of the signal edge but rather at the centre of the bit field, although the signal comes from the same FPGA with global clocks used on output flip-flops. Cross-talk was expected, but a capacitively-coupled spike was expected at the signal edge, which would have been safe since the signal is sampled far from the edges. However, with the spike seen in the centre, the noise margins are not as hoped for, but probably acceptable if the signal distortion due to DCI can be dealt with.
- More information is now available on the FIO noise/cross-talk problems. With L/H logic thresholds at 520 mV and 980 mV, it is clear why the noise/cross-talk level of 480 mV observed on at least one trace on a JEM would produce bit errors.
- The source of the cross-talk is mysterious. It appears in the middle of the bit period, rather than at the time of transitions, so the hypothesis is that it may be produced by reflections from incorrectly source-terminated Xilinx outputs. Indeed, probing the FIO signals around the main processing FPGA shows degraded shapes consistent with incorrect source (DCI) terminations. Xilinx have been notified in the hope that they can suggest the cause of this mismatch.
- The magnitude of the effect can be reduced by:
  - adjusting the value of the source termination → noise/cross-talk reduces to 430 mV

- disabling nearest-neighbour signal drivers → noise/cross-talk reduces to 330 mV

  As it would be impossible to fine-tune ~150 DCI values per JEM, suggestions are awaited from Xilinx.

- More radical solutions might involve using different signalling standards with higher thresholds, changing the layer spacing on the motherboard pcb, or adding extra ground planes, but at present these are not thought necessary.
- It is unfortunately impossible to reduce drive currents to slow down the edge speeds when using DCI.
- Readout firmware has been modified for 9U ROD formats but has so far not been tested. Without a ROD available tests are difficult, in particular since the above FIO noise problem takes a lot of effort.
- The online software is currently not very stable and every other hour a re-boot is required due to segmentation faults turning up in otherwise apparently working code.
- The new G-link daughter-card is now being assembled, and will hopefully be available for the RAL integration tests next week.
- The new JEM1.1 may also be available in time for tests at RAL next week.

4. RAL

- The new batch of 12 LSMs for the pre-production full-crate tests of CPMs (and JEMs) is currently being manufactured, and is scheduled to be delivered to RAL on 2nd June.
- Quotations from three companies for the first four optical RGTMs for the PPMs are awaited.
- Richard has approved the Bill of Materials for the CPM v1.9, and Xilinx devices sufficient for a total of 12 modules will be ordered now, to minimise problems of potentially long lead-times.
- Firmware upgrades (error-handling, etc.) to the 9U ROD have been implemented.
- The Drawing Office will start modifying the schematics and layout for the production CMM in about one week.
- The production VMM and TCM designs will soon be required.

5. Stockholm

- Production of the ~2100 LVDS cable assemblies from AMP-Tyco remains unclear. Sten is in discussion with their Swedish distributors, but has not yet obtained confirmation that they will provide the cables. This is becoming very urgent, as an initial batch of ~400 cable assemblies is needed quite soon (~July) for the full-crate tests of CPMs (and JEMs) demanded by the CPM (and JEM) FDRs, which are pre-requisites for full module production.
- Murrough will send details of final numbers and lengths of the cable assemblies for Sten to forward to the AMP-Tyco distributors.
- The acceptance criteria for the completed cable assemblies, and the procedures required to measure them, must be specified very soon.
- Where are the specifications of the cable parameter to be found? They are apparently no longer to be seen on the AMP-Tyco web pages.
- The call for tenders for the Processor Backplane (PB) has been made public, with a closing date for returns of June 10th, followed by a 10-day evaluation period before a contract can be raised.

Next Phone Conference – Thursday 2nd June 2005 at 10:00 *(UK)*, 11:00 *(Germany, Sweden)*

Tony Gillman