Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 13th January 2005

Birmingham:	**Richard Booth, Stephen Hillier, Gilles Mahout, Richard Staley, Jürgen Thomas, Dimitrios Typaldos, Pete Watkins**
Heidelberg:	**Ralf Achenbach, Paul Hanke, Eike-Erik Kluge, Kambiz Mahboubi, Frederik Rühr, Klaus Schmitt, Hans-Christian Schultz-Coulon**
Mainz:	**Stefan Rieke, Uli Schäfer**
QMUL:	**Eric Eisenhandler***
RAL:	**Bruce Barnett, Ian Brawn, Norman Gee, Tony Gillman, Weiming Qian**
Stockholm:	**Christian Bohm, Sten Hellman, Sam Silverstein**
	**at RAL*

1. *Birmingham*

- Continuing tests of CPMs at RAL took place before Christmas, in particular checking the new firmware designed for asynchronous G-link readout mode. All links remained stable over periods of several hours.
- The two new LVDS Source Modules (LSMs) arrived in Birmingham just before Christmas, after successful JTAG testing at RAL. Delivery of front-panels is expected soon. Unfortunately, the appropriate ByteBlaster II data download cable was not available, so the modules could so far only be checked out on the bench, loaded with test data via the FPGA and not yet from a PC. The appropriate download cable is now on order.
- Assembly of the two new CPMs has been slightly delayed, due to a problem of over-etching of some of the fine-pitch pcb traces. Delivery of assembled modules is now scheduled for 15th January.
- Richard has located a company in the USA which will sell LVDS cables with appropriate connectors and of customised lengths. He will order a few short (~2m) assemblies for tests with the LSMs, although we agreed that the production testing of CPMs and (JEMs) should be carried out in a realistic environment with full-length (15m?) LVDS cable assemblies, which will also ensure that the pre-compensation is operating correctly.

2. *Heidelberg*

- The Production Readiness Review for the PPr ASIC/MCM will be held on Friday 14th January at KIP. Eric, Viraj and Tony will travel to Heidelberg, with Philippe Farthouat and Stefan Haas participating via a video link from CERN.
- The second (replacement) batch of ASIC wafers was delivered to KIP in December, but only contained 15 wafers having had 9 wafers fail QA checks. The overall yield on this batch is ~40%, even lower than for the first batch (~57%), which is very worrying, as the yield was predicted to be >60%. The overall yield from a total of 35 wafer is now only ~50%.
- A further batch of 15 wafers will be delivered to KIP at the end of January to complete the original order. With the overall yield so far only ~50%, at least 7 wafers must be good from this last batch to yield a further 662 working dies, to provide the required total of 4000 Known Good Dies.
- Tests and modifications (hardware and firmware) continue to be made with the PPM.
- Kambiz and Florian will visit RAL the week beginning 17th January 2005 to resume the PPM-CPM integration studies.

3. Mainz

- The System ACE configuration problems on the JEM have now been solved satisfactorily, by the addition of appropriate clock buffers.
- An additional (seventh) daughter-board will be added to the JEM design, to contain VME, configuration and CAN logic. Bruno is currently modifying the schematics to accommodate these changes, which should be complete by next week.
- Preparations for the forthcoming Final Design Review for the JEM are progressing, starting with updates to the module specifications, for which some documentation from Stockholm will be needed.

4. RAL

- Twelve new TTCdec cards have been manufactured and were delivered to RAL on 7th January 2005.
- Tests of the new 9U ROD are progressing well, so an order has now been placed for the second board. This board will be assembled using a larger Xilinx device for the Switch FPGA, and should be delivered to RAL by the first week of February 2005.
- All necessary modifications to the CMM schematics have now been completed:
  - All CMM Problem Reports have been dealt with.
  - System ACE has been incorporated
  - The front-panel and RTM connector types have been changed to match the CTP input connectors
  - The mother-board has been modified to accommodate the new TTCdec
- The CMM schematics and netlist need to be checked before the pcb layout is finalised. The layout has commenced and should be completed next week.
- The TCM-VME64, TCM-CJEP and the VMM require Final Design Reviews so that the designs can be finalised. In the meantime, quotations for manufacture and assembly of these modules will be requested by the end of January 2005.

5. Stockholm

- The Final Design review of the Processor Backplane at RAL went well, and the report containing conclusions and recommendations will be circulated as soon as possible. There have been some recent difficulties concerning the exact specification of the VME—bus, and in particular the problems associated with using a second processor in crate slot 2.
- Updates to the Processor Backplane schematics are being worked on.
- The cable strain relief system has been tried out, and found to exhibit weakness in the central region of the module connector. A third retaining bar appears to fix this problem.
- Some work has been going on to improve the module insertion/extraction mechanics at the front of the crate. Mechanical parts from different companies are not always compatible in certain combinations. A strong stainless-steel extrusion is available from a company in the USA, but would require major modifications to all the existing Wiener processor crates. Possibly the existing extrusions could be further strengthened…?
- Richard has not yet tried out the "TripleEase" ejector handles from Triple E with a CPM.

Next Phone Conference – Thursday 27th January 2005 at 10:00 *(UK)*, 11:00 *(Germany, Sweden)*

Tony Gillman