Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 17th February 2005

Birmingham: **Stephen Hillier, Gilles Mahout, Richard Staley**

Heidelberg: **Ralf Achenbach, Florian Föhlisch, Christoph Geweniger, Kambiz Mahboubi, Karlheinz Meier, Frederik Rühr, Klaus Schmitt, Hans-Christian Schultz-Coulon, Pavel Weber**

Mainz: **Stefan Rieke, Uli Schäfer**

QMUL: **Eric Eisenhandler***

RAL: **Ian Brawn, Tony Gillman, Weiming Qian**

Stockholm: **Christian Bohm, Sten Hellman, Sam Silverstein**

**at CERN*

1. Birmingham

- The two new version 1.9 CPMs continue to be tested at Birmingham. The effect of using different low-jitter PLLs and improved Backplane signal routing has increased the overall Backplane data timing window (using the parity error-free criterion) from 1.0 nsec to 1.5 nsec. Hopefully, this may still be further increased to 2.0 nsec. For a single CP FPGA, the timing window is already ~2.0 nsec.
- All LVDS inputs on the new CPMs have been checked to work correctly, but the optical G-link data outputs have not yet been checked.
- One CPM displays much more TTC clock jitter than the other module, which may be derived from its TTCdec card. This will be studied further.
- It has been observed that when operating both CPMs together in adjacent slots (with FIO dialogue), their relative TTC clock timing appears to drift with time by up to 500 psec. It is currently necessary to check and correct the timing settings every few hours. The cause of this behaviour is unknown at present, but is possibly a temperature effect in the TTCrx chip. It was suggested that the TTCdec card be temperature cycled over a wide range to observe if the deskewed TTC clock timing changes. Also, it may be useful to subject the entire CPM to a controlled oven test at Birmingham whilst monitoring the relative delay of the deskewed TTC clock.
- The LSMs have now been extensively tested, and we need to define how many more to order to fulfil the test requirements for the CPM and JEM production.
- The TripleEase ejector handles have been tried (after some *bricollage*) on an old CPM, and appear to be a significant improvement on the original type.

2. Heidelberg

- The ASIC wafer tests are now complete, with a total of 4480 Known Good Dies having been produced. The spread of yields across all wafers is very high, with a range from 70% down to 2% per wafer. The six lowest-yield wafers will be returned to the manufacturers to try to negotiate a further production batch. This will leave a total of 4332 Known Good Dies until this further production batch becomes available, some of which will have derived from wafers with yields as low as 20%.
- The MCM production contract is still being negotiated between KIP, Würth and Hasec.
- The KIP response to the recommendation in the ASIC/MCM PRR Report have been drafted and will be sent to the Review panel within the next few days.
- Tests are now under way of the AnIn daughter-cards for the PPM, and in particular to measure the level of inter-channel cross-talk. The final AnIn design will then be made, and full production can take place.

- The recent integration tests of the PPM at RAL highlighted some continuing problems with the LVDS Cable Driver (LCD) card, relating to LVDS signal quality. Three separate solution are being tried:
    - change the configuration and values of the existing CR pre-emphasis network to match those on the LSM
    - change the Virtex-II pin driver configuration to provide a true LVDS current source, which should have zero time-skew between the LVDS+ and LVDS- halves (*c.f.* the 300 psec time-skew measured at present when driven as a voltage source), and change to an LR pre-emphasis network as required
    - change the Virtex-II device for a more recent FPGA version (Virtex-4)?, which will provide zero time-skew LVDS drivers

  Only the last of these options would definitely require a PCB layout change, although it would be hoped that the re-designed LCD could retain the same footprint on to the PPM motherboard.
- There are several integrated design changes to be made to the PPM, which will be carried out once the full testing is complete, which should lead to the final production design.

3. Mainz

- Following the recent PPM-JEM integration tests at RAL, studies of the JEM FIO performance have been continuing in Mainz, and the error-free Backplane data timing window has been measured to be 6.5 nsec (in a data cycle period of 12.5 nsec). Bit-error rates down to 10^{-14} have been measured so far, which is extremely good.
- A test module for the optical G-links on the JEMs is being designed to provide automated testing of this functionality in the production JEMs, to check BERs down to very low levels (low statistics measurements have so far enabled BERs to be measured down to only 10^{-9}). It is intended to be operated by the module assembly company (Rhode & Schwartz), and may also be a useful instrument for testing the similar functionality of other trigger modules (PPMs, CPMs and CMMs), unless the ROD can be used for this purpose with special firmware.
- The next (hopefully final) design iteration of the JEM is under way, but awaits the return of Bruno, who is currently ill.
- The Final Design review of the JEM will be held in Mainz on Tuesday 5th April, the day before the next Joint Meeting starts, and it will be chaired by Eric. Everyone will be encouraged to read the documentation once it is made available.

4. RAL

- The change requests generated for the ROD firmware are steadily being worked through.
- Weiming has brought all of the ROD input data formats (except for that of the PPM) up to the latest version of the specifications.
- The first ROD module is now ready to be driven from the TTC system, and may be brought to the PPD Trigger Lab.
- The second ROD has been successfully JTAG-tested, and is ready for the next stage of bench-testing.
- Ian has completed a draft of the CMM Test Plan required for the PRR on 28th February at RAL.
- Adam continues to work on preparing generic CANBus software for use in different modules.

5. Stockholm

- Sam and Christian have been correcting the known errors in the original Backplane PCB design files. They await the Report from the Final Design Review, which has a number of recommendations. This is now almost complete, and Tony will send out the draft by the end of this week.
- The LVDS cable/connector retention scheme has been modified to provide improved bracing in the centre of the connectors, and this requires some new parts to be machined. Ian will send dimensional details of the current RTM retention mechanics to Sam for information.
- The final water-cooled Wiener crates have still not been delivered to Stockholm. This is becoming urgent in order to check compatibility between their mechanics, the Backplane, the power bus-bar system and the cable/connector retention mechanics.

6. AOB

- The first batch of Transition Modules for the TileCal receivers has arrived in CERN.

Next Phone Conference – Thursday 3rd March 2005 at 10:00 *(UK)*, 11:00 *(Germany, Sweden)*

Tony Gillman