Notes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 21st April 2005

Birmingham: **Richard Booth*, Stephen Hillier, Gilles Mahout, Richard Staley, Dimitrios Typaldos, Peter Watkins**

Heidelberg: **Ralf Achenbach, Victor Andrei, Christoph Geweniger, Paul Hanke, Eike-Erik Kluge, Victor Lendermann, Kambiz Mahboubi, Frederik Rühr, Klaus Schmitt, Hans-Christian Schultz-Coulon, Pavel Weber**

QMUL: **Eric Eisenhandler***

RAL: **Ian Brawn, Tony Gillman, Weiming Qian**

Stockholm: **Attila Hidvégi**

**at RAL*

1. Birmingham

- Gilles has made excellent progress in extending the FIO data timing window on the CPM, as recommended at the FDR. By modifying the CP chip firmware (scan-path diagnostic mode only, so far) to accept a third clock phase for latching the 160 Mbit/s data, the timing window has increased from 2.0 nsec to 3.0 nsec. He believes that this cannot be further improved without providing each CP chip with customised firmware. This would be very difficult to maintain, and will not be further pursued unless found absolutely necessary.

  A fully-functional version of this new code, incorporating the CP algorithm, is now being written.

- Richard has completed the schematics for all six versions of the Receiver-Preprocessor Patch-Panels (RPPPs), and a slot has been provisionally booked in the RAL Drawing Office in May to carry out the layouts. The appropriate 37-pin sub-D connectors have still to be identified.

- The CPM FDR recommendations are being worked through, and it is hoped that the PRR can be held some time in May, after which module production can begin. Some guidelines for the necessary documentation will be provided, based upon experience with the recent PRRs for the CMM and the PPr ASIC/MCM assembly.

- A final decision on the number of LSMs to manufacture was taken; a total of 14 new modules will be built to add to the existing two modules, enabling a full crate of JEMs (or CPMS) to be tested. This system test was strongly encouraged by the reviewers at the recent CPM and JEM FDRs.
  n.b. This test will require the procurement of a number of production LVDS cables. A maximum number of 384 cables are needed, *i.e.* a further 224 over the existing number of 160, on a timescale of about the end of July.

2. Heidelberg

- The first batch of MCM substrates is due to be delivered in mid-May.

- A lot of work has been done on the re-design of the LCD card for the PPM. The schematics of the new 4-FPGA daughter-card are now finished, and the layout has been started by Peter Stock.

- The design for the PPM CANBus controller has been started, based upon Adam's documentation, but omitting the RS232 port as there would be no space for it on the PPM front-panel.

- Paul will send the G-link transmitter chips to Viraj, for assembly on to the PPM new optical Rear G-link Transition Modules (RGTMs).

- Kambiz has been working on the PPM readout, and will visit RAL for the planned integration week starting on 9th May.

3. Mainz

As he was unable to be present, Uli had sent the following short status report on the JEM:

- Stefan and Bruno have started to look into FIO signal integrity with various data patterns, recording eye diagrams on the scope. Final results are not yet available.
- A new iteration of the readout module (4-layer daughter-card PCB) is currently in production.
- Bruno is now working on the JTAG test adapters and should be able to start with the control module design next week.

4. RAL

- Tests of the second 9U ROD have been continuing: two bugs in the VME address decoding and S-link controller have been fixed, and the real-time data path has been checked.
- System ACE in the 9U ROD is working, and different firmware versions can be selected.
- Changes to the schematics for the CMM are being made, and it will then go to the RAL Drawing Office for the (fairly minor) layout changes required to meet the PRR requirements. Production can then start.
- The TileCal Patch-Panel (TCPP) prototype module is believed to need some design changes before production can start. The major concerns are grounding and shielding, and Weiming and Tony have been looking into these issues.
- Weiming has modified the firmware in all of the 6U RODs to accept neutral format data.
- Two Mark-I TTCdecs have been located to populate two DSS modules.

5. Stockholm

- Several issues connected with the jet algorithm firmware have been resolved.
- Sten is looking into the ordering of the LVDS cable assemblies. The final lengths are still uncertain, but it is hoped to make some routing measurements in USA15 next week when several trigger people will be at CERN (assuming they can obtain authorisation to descend into the ATLAS cavern – safety training is mandatory). It seems that only insignificant savings in latency can be obtained by CP and JEP sub-systems fed by different length cables, so probably all cables will be cut to the same length. *(n.b. It is important that a figure for the minimum bend radius is obtained for these cable assemblies before routing length estimates are made.)*
- The tendering requests for manufacture of the Processor Backplanes will be issued by the end of this week. It is hoped that the first Processor Crate/Backplane assemblies will be available for shipment from Stockholm by around the end of August.
- Some informal discussion took place at the end of the Mainz meeting between Sam, Uli, Richard and others on the issue of system grounding. Richard will try to summarise some of the conclusions.

Next Phone Conference – Thursday 5th May 2005 at 10:00 *(UK)*, 11:00 *(Germany, Sweden)*

Tony Gillman