Minutes of ATLAS Level-1 Calorimeter Trigger Phone Conference – 29 Sept. 2005

Birmingham: Richard Booth, Dave Charlton, Gilles Mahout, Richard Staley, Dimitrios Typaldos, Pete Watkins
Heidelberg: Ralf Achenbach, Victor Andrei, Christoph Geweniger, Paul Hanke, Kambiz Mahboubi, Klaus Schmidt, Hans-Christian Schultz-Coulon, Pavel Weber
Mainz: Uli Schäfer
Queen Mary: Eric Eisenhandler (at RAL; chair and minutes)
RAL: Bruce Barnett, Weiming Qian
Stockholm: Christian Bohm, Sten Hellman

Note that a number of people at CERN could not phone in. Paul Hanke gives a report on their behalf under Heidelberg, and Norman Gee has circulated daily reports by e-mail.

Viraj Perera could not attend but sent a status report that was only received by the chairman after the meeting due to an email problem at Queen Mary; it is included in these minutes.

Birmingham
Gilles reported that they are waiting for the two CPM pre-production modules, now due back next week. He estimates it will take about a week to test these, and if all is well a further 10 will be ordered, to allow a full-crate test before full production. The 10 could be back by end-October/early November.

Firmware work has got the fan-in/fan-out timing windows up to 2.7 ns for signals from the left but it remains at 2.5 ns on the right. Latency may now be better, perhaps by 1 b.c.

The CPM has continued tests with the ROD.

The first RPPP (patch panel): see RAL, below. These will be tested at Birmingham.

Heidelberg
Kambiz reported on a very successful few days of PPM tests at RAL. Klaus had fixed the VME firmware and everything seemed to be stable. The new LCD card was tested. All e.m. outputs to the CPM first ran overnight without error (12–13 hours) with the same data on all links. More stressful patterns revealed one stuck bit in one MCM, which went away if the MCM was changed. A second overnight run with somewhat more stressful data was also error-free, excepting of course that one bit. There was not much time to test JEM inputs, but a half-hour test of almost all inputs with stressful data had no link-loss or obvious errors.

Finally, tests were made of ROD readout, first electrically into a 6U ROD overnight, which was error-free. Going via the optical rear G-link card there were problems at high rates with data headers that were traced to the ROD firmware, but at a somewhat lower rate the readout ran successfully overnight. The data read out was also verified by the simulation.

Paul reported on events at CERN. Both TileCal and Liquid Argon groups supplied fibres with clocks and triggers. Eventually Florian and Frederik managed to see calibration pulses successfully in the PPM memories. However, then some problems set in and everything seemed to stop working. This is not yet understood, so it is clear that the problem must be found, and things must be sorted out to be easier to set up and reproducible.

MCM production continues with unchanged high yield.

Mainz
Uli reported that JEM 1.2 came back from the manufacturer with the two big FPGAs swapped. They will have to be re-worked, and it should be done by next week. This board is crucial because the signals have been re-routed in an attempt to reduce the crosstalk problem on fan-in/fan-out signals.

New TTC decoder cards do not match the mounting holes on this board. There has been some confusion about mirror-imaging due to the components on the card facing the motherboard. People should check all modules to make sure they are the right way around; Eric proposed that in case of problems the simplest solution is for all non-production designs to adapt to the present decoder card layout in the final version. We should also avoid having two types of TTC decoder cards in the system.

Queen Mary
Eric said that an agreement had now been reached on the format of all labels for level-1 trigger (i.e. L1Calo, L1Muon, CTP) equipment. We will use four-character IDs at the start of the serial number, similar to what was proposed earlier by email but with a few detailed changes for specific items. In order to make the information easy to find for getting labels made, a table will be put on the web.

RAL
Weiming reported that he is working on uncompressed PPM readout firmware for the ROD, and Dave Sankey has made good progress with firmware for compressed PPM readout. The compressed-readout firmware now fits into the FPGA.

Bruce said there was progress with testing the CPM readout format, though in general when testing modules the emphasis is mainly put on trying the neutral format initially.

Viraj reported the following items:

The CMM design changes have been finalised and checked. The layout is now completed. Order for components for 21 boards were placed on 24th August and the order to manufacture the first two boards will be placed soon after the final drawing office checks are made today and the design data based is released for manufacture (tomorrow or Monday).

Two more RODs are being built. Design and layout changes have been completed. Orders to manufacture the two boards, and for components for 26 boards (excluding Xilinx FPGAs), were placed yesterday.

The VMM schematics has been updated to reflect specification version 2.1. It is in the final stages of layout now.

Work on implementing the TCM design will start soon after the VMM is completed

Richard's Patch Panels: Type 1 has been completed, is awaiting checks and has gone out for quotation. Meanwhile work has started the design for the second. Design work will continue on the patch panels until all have been completed.

Stockholm
Christian said that Sam had already received some interesting responses to the tender for the Processor Backplane; the deadline is tomorrow and it is hoped that a decision can be made by next week.

On the TileCal cables, 1 km was due from the Swedish supplier by today, but they had a problem making it: either it has to be 10% larger diameter, or the impedance must be 75 ohms rather than 88 ohms. Larger is not ok, but 75 ohms is ok since that is close to the what Weiming measured for the LAr cable. The 1 km is now due 13 Oct., then the remaining 4 km 2–3 weeks later. At the same time, 12 km has been ordered from the LAr supplier.

Sten said the LVDS cables are due to arrive in three batches: 900, 900 and 300. The first batch is due on 11 Oct. and the last at the end of Oct. Sten said only connectivity tests will be done at the factory, and Bruce stressed that it is very important to test these as quickly as possible for bit-error rate.