ATLAS Level-1 Calorimeter Trigger
Prototype Processor Backplane

Project Specification (FDR)

Version 1.1

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Table of Contents

Document History

Version 0.1	(November 8, 2004)	Initial review and advance distribution to manufacturers
Version 0.2	(November 21, 2004)	Addition of new test results from RAL Clarification of differential impedances Most initial corrections suggested by reviewers
Version 0.3	(December 1, 2004)	More corrections suggested by reviewers Added CANbus pinout (2.9.5) Connector numbering and silkscreen (2.10) TTC signal quality (3.5) Module keying (3.8) Treatment of mixed LVDS/FIO cable headers (3.10.2) Expanded test planning for production PB (4.4 - 4.6)
Version 1.0	(April 10, 2005)	Implemented changes recommended by FDR committee Updated BOM and other manufacturer specifications
Version 1.1	(May 2, 2005)	Added last-minute changes to specification before starting tender process

1 Introduction

This document has been produced for the final design review (FDR) of the ATLAS Level-1 Calorimeter Trigger Processor Backplane and its respective mechanical hardware. It includes updated specifications based on prototype experiences, as well as test results from the prototype programme.

1.1 Overview

The Processor Backplane (PB) for the ATLAS Level-1 calorimeter trigger is used for both the Cluster Processor (CP) and the Jet/Energy Sum Processor (JEP) subsystems. Its functions include:

- Hosting 14 Cluster Processor modules (CPMs) or 16 Jet/Energy Modules (JEMs), two data-merging modules (Common Merger Modules, or CMMs), one Timing and Control Module (TCM) and at one or two local VME CPUs (CPU).
- Receiving serial cable links from the PreProcessor system (PPR) and feed their signals to the JEMs or CPMs in the crate.
- Providing point-to-point connections for data sharing between neighbouring CPMs or JEMs.
- Providing point-to-point connections from each processor module to both CMMs for real-time results merging.
- Distributing timing, trigger and control (TTC) signals from the TCM to all other modules.
- Provide a reduced-function VME-based bus to all modules in the crate (VME--).
- Host a differential CAN bus for slow control and monitoring of all modules.
- Provide extended geographical addressing system with unique identifiers for every module in the CP and JEP systems, for specifying VME, TTC, and CAN addresses for that board, and select position-dependent configuration options.
- Provide up to 25A of combined 5V and 3.3V power to each module.

1.2 Scope of this document

The scope of this document is to describe the specification for the production Processor Backplane, including changes from the prototype design, and to review the results of the prototype test program. The appendices include documentation necessary for prospective backplane manufacturers to submit a bid during the tendering period.

The document is structured as follows: Section 2 describes the functional requirements of the Processor Backplane and how these are implemented. Section 3 describes the results for prototype backplane test program. Section 4 describes aspects of the management of the project, and Section 5 provides time scales for production and installation of the production backplane.

1.3 Related projects

The PB provides the primary interface between several other components of the Level-1 Calorimeter Trigger, which are being developed in parallel with this project. Existing documentation for these components can be found at http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html. The relevant modules and their latest document versions at the time of writing are:

CPM	Version 1.03 (post PDR)
JEM	Version 1.0.1 (PDR)
TCM	Version 1.0 (PDR)
CMM	Version 1.5 (Module Specification)
VMM	Draft 1 (2002)

These related components have been through, or will shortly undergo, reviews of their own, and the requirements for the PB are matched to the components of the CP and JEP systems.

2 Functional requirements and implementation

This section introduces the requirements on the functions of the Processor Backplane, and how they are implemented

2.1 Backplane dimensions and organisation

The Processor Backplane is installed in a modified CERN standard crate with 9U nominal height (400.05 mm) and 84 HP width (426.72 mm), conforming with IEEE 1101.10 specifications. The crate accepts up to 21 modules of 4HP width (20.02 mm) each, with a vertical height of 366.7 mm and a depth of 400mm. Each position is designed to service only one type of module. The organisation of modules in the processor crate is presented in Table 1.

Table 1: Processor Backplane Organisation.

Position(s)	Module Type
1 and/or 2	VME Controller (CPU), mounted in 9U VME Mount Module (VMM)
3	Common Merger Module (CMM)
4-19 (or 5-18)	Jet Energy-Sum Module (JEM) or Cluster Processor Module (CPM)
20	Common Merger Module (CMM)
21	Timing and Control Module (TCM)

Position 1 is located at the left side of the crate, viewed from the front, while position 21 is at the right side. In this document, “left” and “right” refer to lower and higher position numbers, respectively. The “front” side of the backplane refers to the side facing the front panel of the rack, where the processor modules are connected.

The processor modules are arranged in order of increasing η with increasing position number. Each JEP crate hosts two contiguous groups of 8 JEMs corresponding to opposite quadrants in ϕ. This arrangement is designed to expedite missing energy calculations in the merger modules by allowing direct subtraction of E_x and E_y values. In both JEP crates, the left-most group of 8 JEMs is assigned to a quadrant with smaller ϕ than the right-most group.

Table 2: Organization of Processor Backplane layers. Approximate diagrams representing each type of signal layer are illustrated in Figures 1, 2 and 3.

Layer #	Signal types in layer	Figure
1	Chassis ground	---
2	VME--, Geographic address lines, TTC fanout	1
3	Signal ground	---
4	VME--, Module Fan in/out connections, CAN bus	2
5	Signal ground	---
6	Crate merger lines for modules 0, 4, 8, and 12	3
7	Signal ground	---
8	Crate merger lines for modules 1, 5, 9, and 13	3
9	Signal ground	---
10	Signal ground	3
11	Crate merger lines for modules 2, 6, 10, and 14	---
12	Signal ground	---
13	Crate merger lines for modules 3, 7, 11, and 15	3
14	Signal ground	---
15	VME--, Module Fan in/out connections	2
16	Signal ground	---
17	VME--, Geographic address lines, TTC fanout	1
18	Chassis ground	---

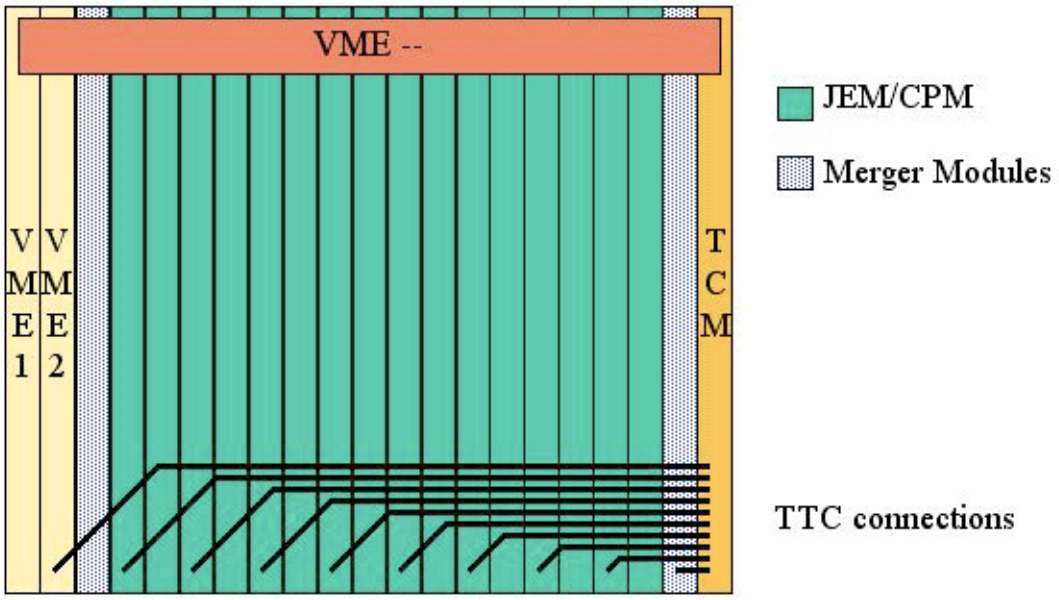

Figure 1: Conceptual layout of an outside layer of the PB (1 of 2), with VME-- and TTC signal distribution. These layers also contain the bussed geographic address lines (not shown). View from front of crate

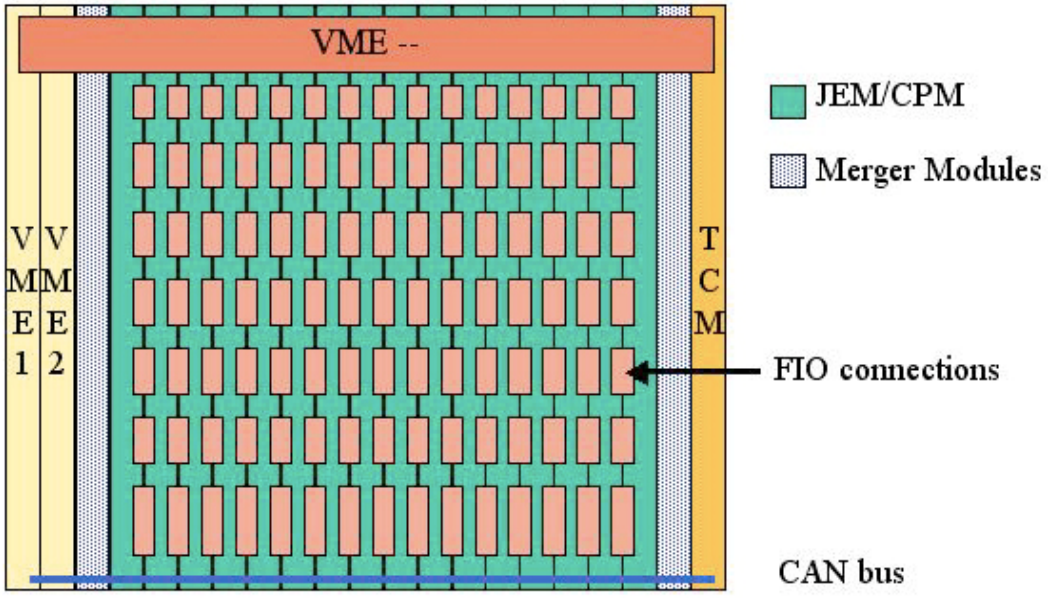

Figure 2: Conceptual layout of a fan-in/out (FIO) layer of the PB, with VME-- and CAN buses. Gaps between the FIO connections are reserved for serial input cable connections. View from front of crate. The small rectangular boxes represent large numbers of short FIO connections between adjacent modules.

2.2 Printed circuit board

The Processor Backplane is a large, monolithic custom PCB, populated largely with 2mm Hard Metric connectors. It is 399.2mm high and 425mm wide, and is designed to reside in a 9U x 84HP chassis.

The PB thickness is 5.8mm and it contains 8 signal layers, which are separated by 8 signal ground planes. An additional two outside chassis ground planes are provided for input cable shields, giving a total of 18 layers. All traces are stripline. There are no power planes; all power is distributed from bus bars near the bottom of the crate, and brought to the modules via high-current (40A) pins. The signal

distribution among the different layers is shown in Table 2, and conceptual layouts of the different layers are depicted in Figures 1, 2, and 3.

To simplify routing through the 2mm pitch connectors, only one signal line per layer is routed between any two pins. This, combined with the separation of neighbouring layers with ground planes, is expected to reduce cross-talk to negligible levels [4].

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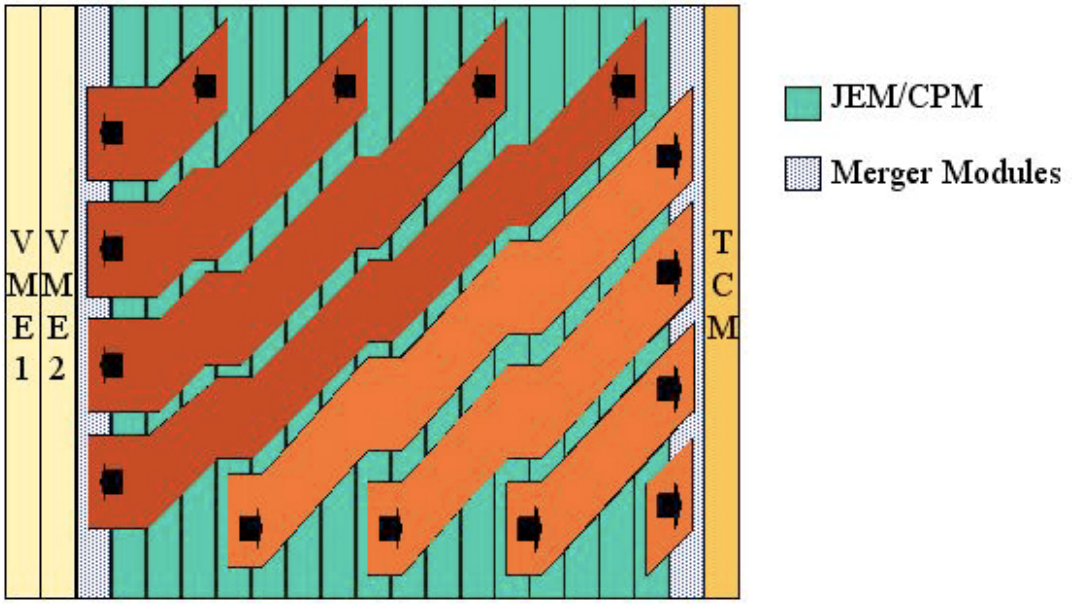


Figure 3: Conceptual layout of a merging layer of the PB (1 of 4). View from front of crate.

2.3 Connectors

The primary connector choice for the PB is the 2mm Hard Metric (HM) family, specified by the international standard IEC 1076-4-101. The large number of high-speed input and output signals required by the CPM, JEM, and CMM make it necessary to use connectors with high density, good signal characteristics, and high reliability. This connector style provides connections on a 2mm pitch, 5 columns wide and with a choice of connector heights. Ground-return shields are available for both sides of the female (card) connectors, which make contact with two additional outside columns on the backplane. By using 2mm HM connectors with 5 rows of signal pins plus two dedicated rows of ground pins, a signal density of 20 signals per centimetre of card edge can be attained while maintaining a signal/ground ratio as low as 4:3. The total width of the connectors is 15.4mm, leaving a space of approximately 5 mm between adjacent connectors.

The 2mm HM connector range (IEC 1076-4-101) has also been chosen due to the availability of a halogen-free cable assembly compatible with the IEC 1076-4-101 specification that is suitable for carrying high-speed LVDS data links from the PreProcessor system to the CPMs and JEMs. These cable links are routed to the back of the processor crates and brought to the modules through the backplane using long through-pins and custom-length shrouds. Custom-built B-19 connectors (Table 3) with eight rows of long through-pins are used to achieve the desired pin configuration. These connectors have three mating levels on the front side to reduce the maximum insertion force.

The modules each consume up to 25 Amperes of 3.3V and 5V DC power. The 2mm HM family includes connectors with DIN cavities that accommodate high-current power pins (up to 40 Amp/pin), which more than suit the system requirements. Tyco/AMP also produces a guide-pin assembly compatible with the 2mm HM family. This assembly helps ensure alignment during board insertion, thus reducing insertion force and minimizing the risk of damage to the PB from improper insertion.

The PB also includes three connectors that do not belong to the 2mm HM family. In each CPU position is a 160-pin VME64-standard J2 connector with through-pins to accommodate eventual daughter cards behind the backplane. There is also a standard 9-pin male DSUB connector behind position 21 to accommodate a standard external CANbus cable

Table 3: Pin configuration of custom B-19 connector for CPM/JEM positions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Z	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
A	B	B	B	B	B	B	B	B	B	C	R	R	R	R	R	R	R	R	B
B	B	B	B	B	B	B	B	B	B	C	R	R	R	R	R	R	R	R	B
C	B	B	B	B	B	B	B	B	B	C	R	R	R	R	R	R	R	R	B
D	B	B	B	B	B	B	B	B	B	C	R	R	R	R	R	R	R	R	B
E	B	B	B	B	B	B	B	B	B	C	R	R	R	R	R	R	R	R	B
F	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Key (Front / Rear) : B: 6.8 / 0 C: 8.3 / 0 R: 5.3 / 8.25
Note: Estimated pin lengths with shroud and PCB thickness subtracted

2.4 Backplane connections

2.4.1 Serial link inputs

Serial link data inputs to the CP and JEP system will be brought to the back side of the backplane via untwisted shielded pair cable assemblies from the PreProcessor system. The current baseline solution for these assemblies are commercially assembled Z-Pack HM assemblies from AMP. Each assembly contains 2 or 4 differential input pairs, plus 1 additional ground shield per two differential cables. While the 4-pair cable assemblies will be used in most cases, the 2-pair assemblies may be required for data at large η, where the calorimeter granularity becomes coarser.

To isolate the high-speed LVDS signals from potential sources of noise, the cable inputs are arranged in blocks of 4 cable assemblies (16 pairs), with ground (or inactive geometric address) pins between the LVDS signals and any other signal pins. The cable ground shields, connected to the middle row of contacts, are connected to the PB chassis ground.

2.4.2 Data fan-in/-out

Both the CPM and JEM share their input data with neighbouring modules, to provide each module with a complete environment for cluster and jet identification algorithms. This is done using short point-to-point, unidirectional fan-in/out (FIO) links between modules. Each CPM uses 320 FIO links at 160 Mbit/s, while the JEM uses 330 FIO links at 80 Mbit/s.

The FIO pins occupy the majority of the processor card edge. They have been placed according to the following guidelines to preserve signal integrity and minimise cross talk at 160 Mbits/s:

- Each FIO pin is adjacent to at least one ground pin.
- Blocks of FIO pins contain even numbers of FIO pins (to balance input and output)
- FIO signals leaving a processor module should arrive at the neighboring module on a pin no than one row above or below the source pin. This simplifies layout and reduces FIO routin more g to two signal layers.

2.4.3 Real-time results merging

Each processor module sends its real-time output to two merger modules (CMMs) via unidirectional, single-ended point-to-point backplane links from two 25-bit output ports, one at the top and one at the bottom of the module. Each CMM therefore receives level-1 real-time results from up to 16 processor modules, each with a width of 24 data bits and one bit of parity. The merger signals are routed diagonally from the processor modules to the CMMs using four signal layers.

2.4.4 Timing, trigger and control (TTC) distribution

A timing and control module (TCM) in each crate receives the 160 Mbit/s TTC signal via an optical fibre, and distributes it electrically to all other modules in the crate as differential PECL signals in a

star configuration. The electrical signals are sent along pairs of parallel 50Ω lines to produce the equivalent of a 100Ω differential impedance.

2.4.5 CAN bus

The TCM also provides the interface between the crate and the ATLAS Detector Control System (DCS). A differential CAN bus is provided to all modules in the crate, and allows readout of temperature and supply voltage information through the TCM to the DCS. A 9-pin D-sub connector is also provided in the rear of the PB to allow a standard CAN cable to be connected to the bus for monitoring and diagnostics. The CAN bus is terminated at position 21 on the TCM. Termination at position 1 is provided on the VMM.

Power for the CAN controller comes from the 5V crate supply to the TCM. No specific provision is made for an auxiliary +5V CAN power supply.

2.4.6 Reduced VME bus

A commercial VME crate processor (CPU) is used for configuration and control of the CP and JEP subsystems. To economise on signal pins, the CPU interface with the processor modules is over a custom, compact bus, called "VME--", which carries only a subset of the full VME64 standard.

Table 4: VME-- signal pins.

Signal name	Number of pins
SYSRESET	1
A[23..1]	23
D[15..0]	16
DS0*	1
Write*	1
DTACK*	1
Total pins used:	**43**

The CPU is carried on a 9U by 400mm VME Mount Module (VMM), which can be inserted in slot 1 or 2 of the PB. The VMM receives +5V through the high-current power connectors at the bottom of the board, and is connected to the VME-- bus via a 2mm HM connector. A VME64 standard J2 connector is also provided with thru-pins for mounting adaptor boards in the rear of the crate. While it is not currently foreseen for two VME masters to function in the crate at once, signal lines are provided on the J1 connectors between these two positions for carrying the bus grant, request and status signals BGIN*(3:0), BGOUT*(3:0), BR*(3:0), BBSY* and BCLR*, as well as the interrupt chain signals IACK*, IACKIN*, IACKOUT*, and IRQ*(7:1), should they be needed.

Termination on both ends of the bus is provided on the modules. The VMM in position 1 should provide termination as near as possible to the bus transceiver buffer chips. Termination in position 21 is provided on the TCM.

2.4.7 Geographic addressing

Dedicated address pins on the Processor Backplane provide every module in the CP and JEP subsystems with the information to uniquely determine their position in the system, and accordingly select appropriate VME, CAN, and TTC addresses. Some modules also load different FPGA configurations based on their geographic address.

Three bussed address lines with switches are needed to identify the system (CP or JEP) and crate number (up to 4 crates). Each module requires up to four additional pins to uniquely identify its position within the crate. Table 5 lists the assignments of geographic address pins to the different modules in the crate. Note that only two bussed address pins are necessary for the CPMs and JEMs, since they "know" which system they are in. The TCM requires three address pins to determine which processor crate it is in. The addresses encoded by local address pins for each type of module in the crate begin with 0, and increase sequentially in the order of increasing position number (left to right).

Table 5: Geographic Addressing.

Module Type	# of bussed crate address pins	# of local address pins

CMM	3	1
CPM/JEM	2	4
TCM	3	0

The geographic address pins are specified as active high. Their values are set by either connecting them to the backplane signal ground (0), or by leaving them unconnected (1). To provide usable geographic addresses on the modules, these pins are connected to pull-up resistors on the modules. Local address pins can be pulled up to any desired voltage, while the bussed crate address pins must be pulled up to 3.3V, using resistor values of at least 10 kΩ. An error in the prototype backplane caused the bussed crate-id address pins to be active low, and the local address pins active high. For the final system, a uniformly active high convention is desired. A rotary decade switch with complementary encoding will be used to achieve this.

2.4.8 Power distribution

The processor crates supply regulated +5V and +3.3V power to high-current bus bars, which in turn provide power to each module in the crate. Other voltages needed by a module may be derived locally from the +5V supply. Each module is supplied with three high-current power pins that carry +5V, +3.3V and ground return from the local bus bars. Each backplane power pin is rated at up to 40A, providing a substantial safety margin for all modules in the system.

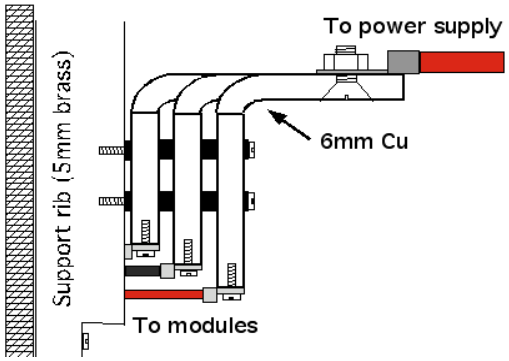


Figure 4: Cross section of power bus bars (not to scale). The bus bars run along the entire width of the PB, and distribute 3.3V, 5V, and signal ground to all modules. Two horizontal tabs on each bus bar accept cables from the crate power supply. The bus bars are mounted on the vertical support ribs. Insulating layers (Plexiglas and Delrin) between and outside the bus bars are included, but not shown in this drawing.

2.5 Line impedance

The Processor Backplane must carry a large number of high-speed digital signals, some for long distances, with minimal distortion, reflection, or cross talk. Single-ended signal lines should have an impedance of 60Ω, while differential signals should be implemented using pairs of parallel lines with 100Ω differential impedance. To simplify routing and make it easier to achieve the desired differential impedance, the prototype backplane simply routed differential traces as two single-ended lines with 2mm between them, with each trace having a 50Ω impedance. The VME-- bus is drawn using 60Ω traces, but the large number of vias connected along it brings the impedance of that bus down to approximately 50Ω. For the prototype backplane, all 50Ω lines were drawn using 0.008” traces, and 60Ω lines were drawn using 0.006” traces, corresponding to widths of approximately 0.007” and 0.005” after the etching process. The backplane manufacturer is responsible for controlling the final impedances. All line impedances are specified to have a tolerance of ±5%.

2.6 Mechanics

The Processor Backplane must be able to withstand repeated insertion and extraction of 9U-height boards with high-density connectors. It is reasonable to expect the number of module insertions/extraction cycles over the lifetime of the backplane to meet or exceed the minimum connector lifetime of 250 such cycles per position (at least for test rigs). Excessive flexing of the backplane during module insertion and extraction can compromise contacts between signal lines and

vias. Flexing also causes connector pin misalignment, which significantly increases insertion/extraction force, thus resulting in even more severe flexing.

To minimize flexing and the problems that it causes, the following measures have been taken:

- An 18-layer backplane PCB with 5.8mm thickness is used. The unusually thick PCB with its many ground planes provides substantial rigidity.
- Custom built B-19 connectors make up the majority of the connector height in the 16 central JEM/CPM positions. These connectors are built with three mating levels which reduces the insertion force in those positions by a few percent.
- A guide pin at the top of each module ensures correct alignment during board insertion, reducing both insertion force and the chance of damage from incorrect alignment.
- Six 20mm-deep vertical support ribs of 5mm-thick brass mounted on the back side of the PB provide a substantial amount of extra stiffness to the PCB, and additionally serve as mounting points for the power bus bars and the input cable strain relief assembly.

2.7 Grounding

The processor crates require two grounds: a chassis ground for terminating the cable shields of the LVDS serial links from the PreProcessor system, and a signal ground for local signals within the crate. Since the PreProcessor to CP/JEP connectivity is many-to-many, the proposed grounding scheme for the final system is for all cable shields to be connected to a common chassis ground in each CP/JEP crate, while in the PreProcessor a passive filter between the cable shields and that chassis ground breaks any potential chassis ground loops. To avoid common mode noise in the LVDS links, the chassis and signal grounds in the CP/JEP crates are connected through a resistor. The Processor Backplane is designed to implement this scheme, with some flexibility in how it is done.

The Processor Backplane contains 8 connected signal ground planes separating the different signal layers, and two outside chassis ground planes. The ground return shields and signal grounds of the modules are connected to the PB signal ground planes, while the LVDS cable shields are connected to the chassis ground. The chassis ground is also electrically connected to the crate and support ribs.

The connection between the chassis and power grounds can be implemented in several ways. Two large vias (ca. 3mm diameter) near slot 1 of the PB can be used for a single-poing conection between the signal and chassis grounds. These vias can also be used for connections with the power bus bar grounds, or the crate. The CPM and JEM also have the possibility to connect signal and cable grounds on those modules, if a multi-point ground connection proves more useful.

2.8 Environmental conditions

The Processor Backplane must be able to tolerate the following environmental conditions:

1. Storage temperature: -20°C to +85°C
2. Operating temperature: 0°C to +70°C
3. Relative humidity: 20% to 70%

These tolerances are similar to those required for other components in the Level-1 calorimeter trigger, and are included in the requirements on the manufacturer.

2.9 Backplane-to-module pin assignments

The detailed backplane pin assignments for each module are presented in Appendices A through D. All pin assignments are specified according to IEC 1076-4-101, with column A on the left side of the connector and row 1 at the top when viewed from the front. These appendices were used as the authoritative reference both for the backplane and module schematics.

2.9.1 CPU

The PB has two CPU interfaces in positions 1 and 2, as presented in Appendix A. The pin naming follows the following conventions:

VME* **	VME-- bus connections
BG*(3:0)(IN/OUT), BR*(3:0), BCLR*, BBSY*	Bus grant signals for determining the priority of the VME masters on the bus. The bus grant inputs are held low in position 1, and the BG(3:0) outputs are connected to their corresponding inputs in position 2.
IACK*,IACKIN*, IACKOUT*, IRQ*(7:1)	Signals used for interrupt requests between the VME masters. The IACKOUT* pin in position 1 is connected to IACKIN* in position 2.
GEOADDX	Geographic address pins. GEOADD(6:4) are bussed lines that identify the crate, while GEOADD(0) identifies the position in the crate.
CAN+/-	Differential CAN bus connection.
TTC+/-	Differential TTC input.
<G>	Ground pins, connected to the PB ground planes.

Connector 2 provides a standard VME64 J2 connector for use by possible personality modules mounted in the rear of the backplane. In the center row (B), signals A(31:24), D(31:16) and RETRY are bussed between positions 1 and 2. Grounds in row B are connected to signal ground. All other pins have no connection.

2.9.2 CMM

The Common Merger Modules (CMMs) are located in positions 3 and 20 of the PB. The pin assignments for these modules are presented in Appendix B. The pin naming follows the convention:

P(15:0)_(24:0)	40 MHz inputs from up to 16 processor modules
M_(83:0)+/-	Through-pins for 84 differential signals routed to a daughter card on the rear of the PB, where inter-crate cables are attached.
VME* **	VME-- bus connections
GEOADDX	Geographic address pins. GEOADD(6:4) consists of bussed lines that identify the crate, while the other pins are module specific.
CAN+/-	Differential CANbus connection
TTC+/-	Differential TTC input
<G>	Ground pins, connected to the PB ground planes
<CG>	Cable ground pins, fed through the PB to daughter cards at the rear.

2.9.3 CPM/JEM

The pin list for the processor modules (CPMs or JEMs), located in positions 4 to 19 of the PB, is presented in Appendix C. The pin naming follows the convention:

FL(164:0)	Fan in/out pins between the module and its neighbour on the left.
FR(164:0)	Fan in/out pins between the module and its neighbour on the right.
SMM(24:0)	40 MHz output pins to the CMM on the left side of the crate.
JMM(24:0)	40 MHz output pins to the CMM on the right side of the crate.
VME* **	VME-- bus connections.
GEOADDX	Geographic address pins. GEOADD(6:4) consists of bussed lines that identify the crate, while the other pins are module specific.
CAN+/-	Differential CANbus connection
TTC+/-	Differential TTC input
<G>	Signal ground pins, connected to the PB ground planes.
<SG>	LVDS cable ground pins, connected to the PB chassis ground plane.
+1, -1, etc.	LVDS cable inputs, Implemented as through-pins.

In position 4, pins FL(164:0) are not tracked, since they would be connected to non-existent modules. Likewise, FR(164:0) are not tracked in position 19.

2.9.4 TCM

The pin list for the TCM, mounted in position 21, is presented in Appendix D. The pin naming follows the convention:

VME* **	VME-- bus connections
GEOADDX	Geographic address pins. GEOADD(6:4) consists of bussed lines that identify the crate number.
CAN+/-	Differential CANbus connection
TTC(20:1)+/-	Differential TTC outputs, sent to modules in positions 1 to 20 of the PB.
<G>	Signal ground pins, connected to the PB ground planes.

Connector 1 is implemented with long through-pins to accept bus-termination daughter cards.

2.9.5 CANbus connector

A 9-pin male DSUB connector behind position 21 of the PB can be used to connect a standard CANbus cable to the internal bus on the backplane. The connected pins are:

Pin 2:	CAN_L	Connected to CAN- on the PB
Pin 3:	CAN_GND	Connected to the PB signal ground planes
Pin 5:	CAN_SHLD	Connected to the PB chassis ground planes
Pin 7:	CAN_H	Connected to CAN+ on the PB

All other pins are unconnected on the PB.

2.10 Connector numbering and silkscreen

A simple connector numbering convention has been chosen to make locating connectors on the PB as simple as possible. Connector names are in the form Jxxy, where xx indicates the slot number (from 01 to 21) and y is the connector number (from 1 to 9) counting from the top of the PB. On the prototype backplane, the connector names and outlines were included on the front side silkscreen. For the production backplanes, they will be provided on both the front and back sides.

Other additions to the silkscreen for the production PB include:

- Marking selected VME signal pins (DS0*, WR*, DTACK*, RESET*)
- Improved labelling on the back side to aid in locating connectors and pins.
- A numbering scheme for the cable input shrouds. The shrouds in each JEM/CPM slot are numbered 1 to 6, counting from top to bottom.

3 Prototype PB test results

Following the PB preliminary design review (PDR) in 2001, four prototype processor backplanes were manufactured, assembled in crates with prototype mechanics, and distributed to labs in Birmingham, RAL and Mainz for testing and integration of prototype trigger hardware during 2002-2004. A series of tests was carried out in conjunction with the larger testing programme in order to verify all aspects of the PB design. Below are the results of these tests.

3.1 Connectivity

The connectivity of the PB is specified in Appendices A through D of this document. These appendices have also been used to specify the backplane pin assignments for all modules interfacing with the PB. To test all backplane connections, test patterns and data have been sent between all modules in all positions. These tests included:

- **VME:** Modules in all positions can be accessed and configured using the VME-- bus.
- **TTC and CAN:** The TCM provides TTC signals and CAN access to all other modules in the crate. The correct distribution of both of these was tested both experimentally, and by manual inspections of the backplane traces in the artwork.
- **FIO:** Data fan in/out between processor modules has been verified by running test data patterns between adjacent JEMs (which use all 330 FIO lines between each position) in all 16 processor module positions
- **Merger data:** Random test patterns were sent from CPMs in all 16 processor module positions to each CMM position, where correct reception was tested. For three CPM-CMM connections where firmware problems made this test difficult, all lines were tested and verified by hand. In all other cases, the data were received correctly in the appropriate places.

3.2 Impedance

Impedance tests of the backplane traces were carried out both at RAL and Stockholm University.

The RAL tests used a time domain reflection technique to measure the reflection of square pulses at the interface between a 50Ω coaxial cable and the backplane traces. The impedance of selected 60Ω merger traces were measured to be ~67.5Ω, while the impedance of a 50Ω TTC trace was found to be ~60Ω. The VME-- bus traces were drawn as 60Ω, but the large numbers of connected vias along them bring down the measured impedance to roughly 50Ω.

The Stockholm tests used a miniature trim-pot at the far ends of selected backplane traces to cancel out reflections, and the trim-pot resistance was then measured with an ohm-meter to give an impedance measurement. The results of these tests were 58.6±2 ohms for the 60Ω traces, and 49.2±2.5 ohms for the 50Ω traces. Although these results were much closer to the initial specifications, the Stockholm tests do not account for inductive trim-pot impedance at high frequencies, which would reduce the apparent impedance of the trace. Therefore the RAL results are considered more reliable.

For the production PB, 50/60 ohm single-ended impedances will be specified with 5% tolerances, and arrangements will be made with the manufacturer to ensure that these tolerances are met.

3.3 Propagation delays

Propagation delay was measured at Stockholm by introducing fast square pulses (rise time ~2ns) to one end of a signal trace, and leaving the far trace unconnected. The timing of the reflected pulse was compared for merger and TTC signals in each position.

Delay tests of selected merger and TTC signals on the prototype backplane are shown in Figure 5. The delays of the diagonal merger signals from the 16 CPM/JEM positions have a ~3ns spread, while the spread of the TTC signal delays between the 18 CMM and CPM/JEM positions is roughly 2.5ns. This suggests a signal propagation speed of roughly 16cm/ns.

Given the 25ns period of data on the merger lines, the 3 ns spread between all modules yields ample margins for timing in data at the CMM inputs. The average TTC clock difference between neighbouring modules is 0.15 ns, which again gives ample timing margins even for the 160 Mb/s FIO signals. But it is recommended to correct for the TTC propagation delays through proper deskew clock settings.

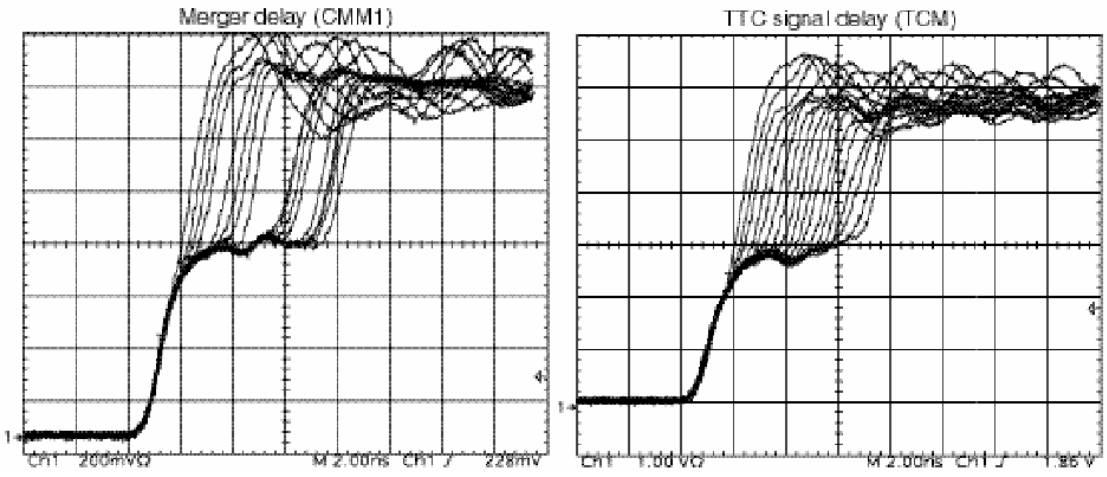


Figure 5: Reflection measurements of merger signal delays. The combined merger delay plot represents transmitted and reflected pulses from all sixteen CPM/JEM module positions to CMM 1. The corresponding plot for CMM 0 is nearly identical. The combined TTC signal delay plot represents transmitted and reflected pulses from all CPM/JEM and CMM positions to the TCM in position 21. The time scale is 2ns/div, giving a signal transmission time scale of 1 nsec/div.

3.4 Cross talk

The Processor Backplane is designed for minimal cross talk. Neighbouring traces on the same signal plane are separated by 2mm, and the signal planes are separated by solid ground planes. Eight signal ground planes provide a strong common ground, minimising any local ground bounce effects. The major sources of cross talk on the backplane are capacitive and inductive coupling between neighbouring traces.

To perform "worst case" tests of cross talk between backplane signals, test patterns were developed to synchronously toggle large numbers of backplane signals while holding a few "test" lines constant. An oscilloscope was used to measure the amplitude of the cross talk on those lines.

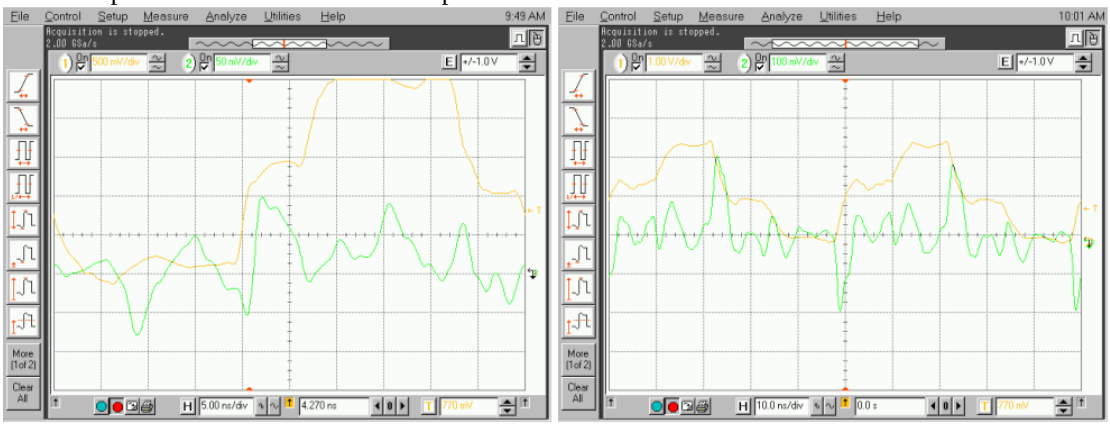


Figure 6: Measured cross talk between merger data lines for a CPM slot next to the CMM (left) and one on the opposite side of the crate from the CMM (right). The time and vertical scales for the cross talk signals (green) on the left and right plots are 5ns/50mVand 10ns/100mV per division, respectively. The vertical scales for signals on the adjacent lines (yellow) are 100 times greater than the cross talk traces.

3.4.1 Merger-Merger cross talk

The greatest expected cross talk is expected to occur on the long merger data lines between the processor modules and the CMMs. To distinguish the "near end" and "far end" components of the cross talk, two tests were performed, one for a CPM adjacent to a CMM, and another near the opposite end of the crate. The results of these two tests are illustrated in Figure 6.

The case where the CPM was adjacent to the CMM is mainly a test of "near end" cross talk (NEXT), which was measured to be less than 5%. The case where the CPM was at a maximum distance from the CMM provided a worst-case test of "far end" cross talk (FEXT). The characteristic pulse at the rising and falling edges of the adjacent arriving signals was less than 10%. This provides ample margin for digital signal integrity. The polarity of the FEXT pulse was the opposite of the rising/falling edges of the driving lines, indicating that the inductive coupling between merger lines is greater than the capacitive coupling.

3.4.2 FIO-LVDS cross talk

The 400 Mbit/s input data links have some sensitivity to common-mode noise, so it was important to investigate the worst-case scenario for FIO noise affecting the input links. To do this, three CPMs in adjacent slots were used, with LVDS data sent from data source/sink modules to all input channels of the center CPM. Synchronous "AA" patterns were sent to the center CPM via the LVDS, and loaded into the playback memories of the neighbouring CPMs, so that all of the FIO lines on all three modules transitioned continuously and simultaneously at 160 Mbit/sec.

This pattern was intended to surround the LVDS links with the largest possible number of simultaneously transitioning signals. After several minutes of running, no parity errors were observed on any of the LVDS links, setting a worst-case upper limit on the bit-error rate at ~10^{-13}. An attempt was made to measure any local ground bounce due to this worst-case test pattern. The absence of an independent local reference ground made it impossible to measure this exactly, but a generous upper limit of 100 mV was obtained, which is well within the tolerance of the LVDS receivers. The true ground bounce amplitude is probably much smaller than this limit.

3.4.3 VME–Merger cross talk

Another potential source of cross talk comes from the VME-- bus, which employs higher-current drivers than other signal sources. There was a concern that VME cycles occurring during data taking might affect signal quality on other signal lines, especially longer lines with large capacitive couplings to the ground planes. To test this, a repeating signal was driven on selected long merger lines while the VME was used to read and write to module addresses in the crate. A sample measurement is shown in Figure 7.

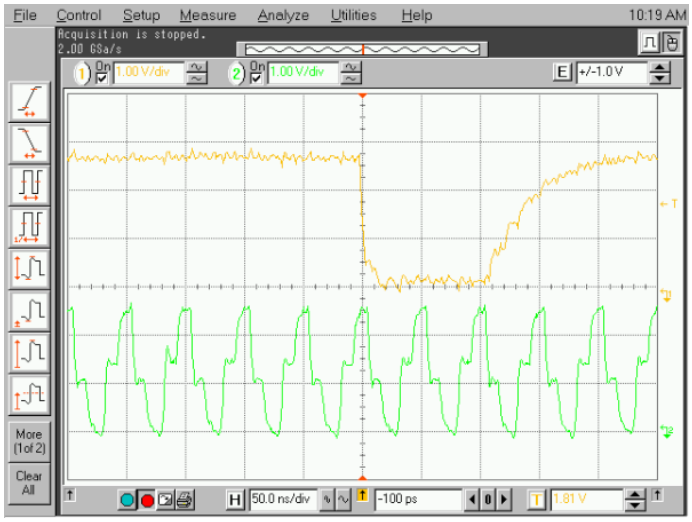


Figure 7: Measured cross talk between the VME bus and merger lines. The DTACK signal (yellow) is asserted at the end of a VME cycle. A repeating signal on one of the longest data merger lines (green) is unaffected by the VME activity. The time scale is 50 ns/div, and the vertical scale is 1.0 V/div for both traces.

Activity on the VME-- bus was found to have no measurable effect on the merger data. This can be attributed to the fact that the merger and VME-- lines are located on different signal layers, and the large number of ground planes minimizes any ground bounce effects. Furthermore, the VME-- bus will be driven with 3.3V signals in the production system, further minimising potential cross talk issues.

3.4.4 Full system tests

To verify that a fully populated processor crate will function properly, a system integration test was performed with six CPMs, two JEMs, two CMMs and a TCM in a single crate. The processor modules ran preprogrammed test patterns on the FIO links between them, as well as data to both CMMs. At the same time, the VME bus was exercised heavily through continuous reading and writing of the dual port RAM of the TCM.

After two hours of continuous operation, no errors had been seen at the CMM inputs, corresponding to a bit-error rate of less than 10^{-13}. This test provides further confidence that the backplane has no serious cross talk or ground bounce issues that threaten data integrity.

3.5 TTC signal quality

The 160 Mbit/sec TTC signal, distributed differentially by the TCM to each module in the crate, must have a very high signal quality in order to provide low-jitter clocks to the system. To test this, a JEM was inserted in slots 4 and 19, corresponding to the lowest and highest processor module distances from the TCM. A high L1A rate (ca. 130k/sec) was transmitted on the A channel to make the TTC signal less deterministic, and possibly introduce more potential instability. A differential probe measured the TTC signal at the JEM position, and a commercial program (Tektronix) was used to calculate the jitter of this signal.

There was no noticeable degradation of the TTC signals from the short to the long TTC tracks on the backplane. The jitter of these signals appeared to depend on the driver channel from the TCM, and the data time interval error (TIE) of these signals had RMS values as low as ~37 ps.

3.6 Power distribution

The prototype processor crates distributed 5V and 3.3V power to all modules in the crate using 1 cm^2 horizontal copper bus bars mounted by insulating holders to the sides of the card cage. The power pins in each slot were connected to the bus bars using short AWG8 cables. This configuration provided excellent current carrying capabilities, but make backplane removal or power pin replacement extremely difficult.

A new power distribution scheme (Section 2.4.8) has been adopted for the production crates. The bus bars have even larger cross sections, and are mounted to the backplane support ribs (Appendix I). The wires between the bus bars and the power pins are thinner (2.5 mm^2), but can be made less than 5cm long. The resistance of these connections at high currents (up to 24A) was measured to be ~1.3 mΩ, which will result in minimal power drops between the bus bars and the modules (less than 25 mV on the CPM). Voltage fluctuations at the module power inputs due to changing load conditions should be negligible.

3.7 Mechanics

The vertical support ribs described in Appendix I are primarily designed to minimize flexing of the backplane PCB during module insertion and extraction. For the prototype processor crates, four aluminium ribs per crate were used. This reduced the maximum displacement from flexing to less than 1mm, resulting in a significant reduction of the insertion and extraction forces. For the production crates the number of ribs will be increased to six, and they will be made of brass instead of aluminium. This should provide even more rigidity, and further reduce insertion and extraction forces.

The most significant mechanical problem seen in the prototype tests was the integrity of the insertion/extraction levers on the module front panels. The front panel hardware for the processor crates is specified by IEEE 1101.10, which includes handles with “hooks” that fit in to the front extrusions and provide leverage for insertion and extraction. On a number of prototype modules, excessive wear was found on these hooks, rendering the handles ineffective. The cause of the problem was found to be vertical flexing of the crate extrusions during insertion, which prevented the hooks from properly engaging. For the production crates, additional reinforcement will be provided to reduce to reduce flexing of the front extrusions. High-quality handles that satisfy the IEEE 1101.10 specifications should also be specified for all production modules. These should be made either of durable plastic (e.g ELMA 81-077/81-078) for modules with low insertion force (VMM and TCM), or preferably solid aluminium (available at www.tripleease.com).

3.8 Module keying

In total, there are five different types of modules (VMM, CMM, CPM, JEM, TCM) that are designed to be inserted in the PB, and each module must be inserted only in the positions designated for it. No keying scheme was used in the prototype crates to prevent inserting modules in incorrect positions (for example, a CPM in a CMM slot). This is clearly undesirable for the final system. Module keying tabs (from e.g. ELMA) can be installed near the front of the crate and behind the module inject/eject handle assemblies that can stop misplaced modules before they make contact with the PB. Such a solution is foreseen for use in the final system.

3.9 Repair and maintenance

The 2mm HM connector family can suffer damage in the form of bent or broken pins, and a method for field repair is essential for maintaining the processor backplane over the lifetime of the ATLAS experiment.

Several backplane pins have been bent or broken during the prototype testing and integration period. In the case of minor bending, the pins can be straightened again without any noticeable problems. However, severely bent pins must be replaced. Tyco/AMP sells a 2mm HM field repair kit (part number 354687-1). This kit has been successfully used for pin replacement on the prototype backplane, and is considered suitable for field replacement of damaged pins. More serious damage

involving a large number of pins will require the backplane to be dismounted and sent to an external company for connector replacement.

3.10 Errata

Comprehensive tests of the prototype backplanes yielded very good results, and the prototypes could be used in the final system if needed. However, a small number of errors were discovered, and these will be rectified in the production series.

3.10.1 PCB errors

- The geographical address pin GEOADDR0 in slot 20 (CMM1) was inadvertently grounded, yielding an incorrect address for that position. The problem was solved for the prototype PB by removing the offending pin. The error in the PB schematics has been identified and corrected.
- The 9-pin male DSUB connector for external access to the CAN bus in slot 21 had the CAN+ and CAN- signals reversed. This will be corrected in the final revision.
- The rotary switch for the crate address resulted in an active low crate ID, while the other geographic address lines are active high. This has been compensated in the prototype design by firmware modifications, but the rotary switch will be replaced with one with complementary encoding in the final design.
- The bus grant and interrupt lines between the two CPU positions were incorrectly implemented in the prototype. The following changes are implemented in the final revision to conform with VME specifications:
    - All BGXIN* signal pins in slot 1 are left floating.
    - All BGXOUT* pins in slot 1 are connected to BGXIN* in slot 2.
    - IACKOUT* in slot 1 is connected to IACKIN* in slot 2.
    - IACKIN* and IACK* are connected together in slot 1.

Another issue with the prototypes was the lack of access to the chassis ground over the back side of the backplane. Pads for 84 surface mount test points connected to chassis ground are provided in the production design.

3.10.2 Mechanical issues

- The cable headers in slots 4-19 had 7 rows (5 signal plus 2 ground). This was found to interfere with the chosen cable connector. The final connectors for these positions have only five rows of long through-pins.
- The shrouds for the cable headers in slots 4-19 were polarised. However, the polarisation was insufficiently strong to ensure correct cable orientation, and the available polarised shrouds had durability issues. The shrouds for the production backplanes have therefore been specified as unpolarised. A visual system for ensuring correct cable orientation (e.g. paint spots on the connector) is necessary, and should be sufficient.
- The two CMM slots (3 and 20) have two types of connectors with long though-pins and shrouds for accepting the Rear Transition Module (RTM), which provides remote cable connection to the CMM. Due to an oversight in specification, the prototype backplanes were delivered with connectors in these positions that had different through-pin lengths, as well as different shroud thicknesses. The combined effect of these differences was that some of the RTM pins had a very short usable length, and the RTM needed to be modified to correct for this. The production backplane will have stricter specifications on the pin length and shroud thickness for connectors in these positions.
- The bottom-most connectors in the CPU and TCM slots had long through-pins and shrouds in the prototype, to allow use of yet-unallocated pins in those positions. No use has yet been found or proposed for these pins, and in practice these long through-pins and shrouds were easily damaged and/or obstructed. They will therefore be removed in the production version.
- The bottom-most cable headers (on connector 7) in slots 4-19 are half populated with LVDS input pins. The other pins are used for FIO signals and signal grounds. In the prototype backplane all of these pins mated with the input LVDS cable, making it possible for the FIO signals to be connected to long, unused cables. To avoid this in the final design, the pins for these FIO signals must be clipped.

4 Project management

4.1 Overview and deliverables

The PB serves both the CP and JEP systems, and naturally must be compatible with all other components in these two systems. Several of these components have already been specified and reviewed, so this specification tries to embody the requirements of those components, as well as to anticipate the requirements of the components yet to be reviewed

This document specifies the production processor backplane of the Level-1 Calorimeter Trigger. Production will be completed in 2005, and installation at ATLAS will be complete by 2006.

The deliverable products of this phase of the project are:

- Specification (this document).
- 11 production PBs (6 system crates plus 1 spare crate for ATLAS, 3 test rigs, and 1 spare PB).
- Support and cable strain relief hardware for 14 crates (production plus prototype)
- Power bus bar assemblies and custom sense wire cards for 10 production crates.
- PB User Reference Guide (This document, suitably modified, may be sufficient).
- Design documentation (schematics, layout information, component data-sheets etc.)

4.2 Personnel

The PB is one of the main hardware responsibilities of the Stockholm group and has been designed there. The main personnel for the project are named below, supported by other members of the Level-1 Calorimeter Trigger Collaboration:

Project Management: Samuel Silverstein (Stockholm)
Project Engineering: Samuel Silverstein, Christian Bohm (Stockholm)

4.3 Design and verification

The design of the PB will be done in Stockholm. The schematic design and layout will be carried out using Mentor Graphics electronics CAD software.

4.4 Manufacturing

The PCB layout and routing will be performed by Stockholm, which will also supervise the manufacture and assembly of the PB. An external company specialising in backplane manufacture and connector fitting will be consulted, and carry out the final PB manufacture and assembly.

The manufacturer will be responsible for PCB production, ordering parts (except for custom parts, which will be the responsibility of Stockholm University), assembly, and testing.

Additional mechanical components including the support ribs, cable strain relief, CMM rear transition module guides, and power bus bars, will be engineered and manufactured in Stockholm. Stockholm University will also receive all production crates from CERN, modify them, and install the backplanes and other hardware before shipping them to their final destinations.

4.5 Pre-production testing

The manufacturer will produce an initial pre-production PCB and test it for connectivity and short circuits. A visual inspection of the board, as well as impedance testing of selected signal lines will be carried out to verify that the PCB meets the specifications

Once it has been established that the PCB fulfills all specifications, the remaining ten backplane PCBs may be produced. The manufacturer is responsible for testing of connectivity/shorts and impedance of selected lines. The test data for each PCB will be made available to Stockholm.
.
The pre-production backplane will then be assembled by the manufacturer, and the assembled PB will be completely tested for connectivity and short circuits. Stockholm University will perform a final

visual inspection of the completed backplane, and resolve any issues with the manufacturer, before assembly of the remaining PCBs is authorized.

4.6 Production testing

Once the pre-production PB has been completed and verified, the manufacturer will then be asked to produce, assemble and test 10 production backplanes.

For the production run, the manufacturer will be responsible for testing the bare PCBs and assembled backplanes for connectivity, short circuits and selected line impedances. Stockholm University will perform additional inspections of the delivered backplanes before finally installing them with associated hardware in the production crates.

4.7 Costs

Detailed cost information for the production PB is not yet available. Preliminary specification documents and artwork will be provided to prospective manufacturers to enable an accurate cost estimate to be obtained

5 Production and distribution

The following approximate milestones are expected for production and distribution:

FDR	Dec 2004
Schematic review and tendering	Jan 2005
Order sent to manufacturer	February 2005
Production complete	April 2005
Crate distribution begins	May 2005

6 Summary

We have presented the specification for the production Processor Backplane for use by the ATLAS Level-1 Calorimeter Trigger. It has evolved from the prototype design with few changes, and tests of the connections, signal quality and mechanical characteristics of the prototype have yielded good results.

Glossary

PB	Proceesor Backplane; the component specified in this document
CP	Cluster Processor sub-system of the Calorimeter Trigger
JEP	Jet/Energy Processor sub-system of the Calorimeter Trigger
CPM	Cluster Processor Module, main module of CP system
JEM	Jet/Energy Module: main module of JEP subsystem
Processor module	Refers to either the CPM or JEM
CMM	Common Merger Module
VMM	VME Mount Module. Hosts a VME CPU in positions 1 or 2.
TCM	Timing and Control Module
TTC	Timing, Trigger and Control
DCS	Detector Control System
LVDS	Low-Voltage Differential Signalling
U	Unit of module height, 1U equals 1.75”
HP	Unit of module width, 1HP equals 0.2”

References

1. ATLAS First-level trigger technical design report (TDR), CERN/LHCC/98-14.
2. IEC Standard 1076-4101
3. IEEE Standard 1101.10-1991
4. ATLAS Level 1 Calorimeter Trigger - Simulation of the backplane for the Common Merger Module. Jayananda, M K, ATL-DAQ-2000-004.

Appendix A: CPU interface connector layout

Pos.	A	B	C	D	E

Guide Pin (0-8mm) (AMP parts 223956-1, 223957-1, or equivalent)

Connector 1 (8-58mm) Type B-25 connector (short through-pins)

1		<G>	VMED00	VMED08	VMED09
2	BBSY*	VMED01	VMED02	VMED10	VMED11
3	BCLR*		VMED03	VMED12	VMED13
4	BG0IN* *	VMED04	VMED05	VMED14	VMED15
5	BG0OUT* **	<G>	VMED06	VMEA23	VMEA22
6	BG1IN* *	VMED07	<G>	VMEA21	VMEA20
7	BG1OUT* **	<G>	VMEDS0*	<G>	<G>
8	BG2IN* *	VMEWRITE*	<G>	VMEA18	VMEA19
9	BG2OUT* **		VMEDTACK*	VMEA16	VMEA17
10	BG3IN* *	VMEA07	VMEA06	VMEA14	VMEA15
11	BG3OUT* **	<G>	VMEA05	VMEA12	VMEA13
12	BR0*	VMEA04	VMEA03	VMEA10	VMEA11
13	BR1*	<G>	VMEA02	VMEA08	VMEA09
14	BR2*	VMERESET*	VMEA01	<G>	<G>
15	BR3*	<G>			
16	IACK*	<G>			
17	IACKIN*	<G>			
18	IACKOUT*	IRQ7*			
19	<G>	IRQ6*			
20	<G>	IRQ5*			
21	<G>	IRQ4*			
22	<G>	IRQ3*			
23	<G>	IRQ2*			
24	<G>	IRQ1*			
25	GEOADD6	GEOADD5	GEOADD4	GEOADD0	

* Set low in Position 1 (bus master)
** Implemented only in Position 1

Connector 2 160-pin J2 VME64 connector
All through pins to rear of backplane for use of personality cards.
All labeled pins (except for ground) are connected between positions 1 and 2. Unlabeled pins have no connection.

Pos:		A	B	C	
1					
2			<G>		
3			RETRY		
4			A24		
5			A25		
6			A26		
7			A27		
8			A28		
9			A29		
10			A30		
11			A31		
12			<G>		
13					
14			D16		
15			D17		
16			D18		

17			D19		
18			D20		
19			D21		
20			D22		
21			D23		
22			<G>		
23			D24		
24			D25		
25			D26		
26			D27		
27			D28		
28			D29		
29			D30		
30			D31		
31			<G>		
32					

Connector 3 (292-336mm) Type B-22 connector (short through pins)

1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20	<G>	<G>	<G>	<G>	
21	CAN+	<G>	TTC+	<G>	
22	CAN-	<G>	TTC-	<G>	

Connector 4 (336-361mm) Type D (N) connector

2	+3.3V
6	Power GND
10	+5.0V

Appendix B: CMM connector layout

Pos.	A	B	C	D	E

Guide Pin (0-8mm) (AMP parts 223956-1, 223957-1, or equivalent)

Connector 1 (8-46mm) Type B-19 connector (short through-pins)

1		<G>	VMED00	VMED08	VMED09
2		VMED01	VMED02	VMED10	VMED11
3		<G>	VMED03	VMED12	VMED13
4		VMED04	VMED05	VMED14	VMED15
5		<G>	VMED06	VMEA23	VMEA22
6		VMED07	<G>	VMEA21	VMEA20
7		<G>	VMEDS0*	<G>	<G>
8		VMEWRITE*	<G>	VMEA18	VMEA19
9		<G>	VMEDTACK*	VMEA16	VMEA17
10	<G>	VMEA07	VMEA06	VMEA14	VMEA15
11	P0_0	<G>	VMEA05	VMEA12	VMEA13
12	P0_1	VMEA04	VMEA03	VMEA10	VMEA11
13	P0_2	<G>	VMEA02	VMEA08	VMEA09
14	P0_3	VMERESET*	VMEA01	<G>	<G>
15	P0_4	P1_0	<G>	P2_0	P3_0
16	P0_5	<G>	P1_1	P2_1	P3_1
17	P0_6	P1_2	P2_2	<G>	P3_2
18	P0_7	<G>	P1_3	P2_3	P3_3
19	P0_8	P1_4	P2_4	<G>	P3_4

Connector 2 (46-84mm) Type B-19 connector (short through pins)

1	P0_9	<G>	P1_5	P2_5	P3_5
2	P0_10	P1_6	P2_6	<G>	P3_6
3	P0_11	<G>	P1_7	P2_7	P3_7
4	P0_12	P1_8	P2_8	<G>	P3_8
5	P0_13	<G>	P1_9	P2_9	P3_9
6	P0_14	P1_10	P2_10	<G>	P3_10
7	P0_15	<G>	P1_11	P2_11	P3_11
8	P0_16	P1_12	P2_12	<G>	P3_12
9	P0_17	<G>	P1_13	P2_13	P3_13
10	P0_18	P1_14	P2_14	<G>	P3_14
11	P0_19	<G>	P1_15	P2_15	P3_15
12	P0_20	P1_16	P2_16	<G>	P3_16
13	P0_21	<G>	P1_17	P2_17	P3_17
14	P0_22	P1_18	P2_18	<G>	P3_18
15	P0_23	<G>	P1_19	P2_19	P3_19
16	P0_24	P1_20	P2_20	<G>	P3_20
17	GEOADD5	P1_21	GEOADD4	P2_21	P3_21
18	GEOADD6	P1_22	P2_22	<G>	P3_22
19	GEOADD0	<G>	P1_23	P2_23	P3_23

Connector 3 (84-122mm) Type B-19 connector (short through pins)

1	P4_0	P1_24	P2_24	<G>	P3_24
2	P4_1	<G>	P5_0	P6_0	P7_0
3	P4_2	P5_1	P6_1	<G>	P7_1
4	P4_3	<G>	P5_2	P6_2	P7_2
5	P4_4	P5_3	P6_3	<G>	P7_3
6	P4_5	<G>	P5_4	P6_4	P7_4
7	P4_6	P5_5	P6_5	<G>	P7_5
8	P4_7	<G>	P5_6	P6_6	P7_6
9	P4_8	P5_7	P6_7	<G>	P7_7
10	P4_9	<G>	P5_8	P6_8	P7_8
11	P4_10	P5_9	P6_9	<G>	P7_9
12	P4_11	<G>	P5_10	P6_10	P7_10
13	P4_12	P5_11	P6_11	<G>	P7_11
14	P4_13	<G>	P5_12	P6_12	P7_12
15	P4_14	P5_13	P6_13	<G>	P7_13
16	P4_15	<G>	P5_14	P6_14	P7_14
17	P4_16	P5_15	P6_15	<G>	P7_15
18	P4_17	<G>	P5_16	P6_16	P7_16
19	P4_18	P5_17	P6_17	<G>	P7_17

Connector 4 (122-160mm) Type B-19 connector (long through pins)

1	P4_19	<G>	P5_18	P6_18	P7_18
2	P4_20	P5_19	P6_19	<G>	P7_19
3	P4_21	<G>	P5_20	P6_20	P7_20
4	P4_22	P5_21	P6_21	<G>	P7_21
5	P4_23	<G>	P5_22	P6_22	P7_22
6	P4_24	P5_23	P6_23	<G>	P7_23
7	<G>	<G>	P5_24	P6_24	P7_24
8	M_00+	M_01+	M_02+	M_03+	M_04+
9	M_00-	M_01-	M_02-	M_03-	M_04-
10	M_05+	M_06+	M_07+	<CG>	M_08+
11	M_05-	M_06-	M_07-	<CG>	M_08-
12	M_09+	M_10+	M_11+	M_12+	M_13+
13	M_09-	M_10-	M_11-	M_12-	M_13-
14	M_14+	<CG>	M_15+	M_16+	M_17+
15	M_14-	<CG>	M_15-	M_16-	M_17-
16	M_18+	M_19+	M_20+	M_21+	M_22+
17	**M_18-**	M_19-	M_20-	M_21-	M_22-
18	M_23+	M_24+	M_25+	<CG>	M_26+
19	M_23-	M_24-	M_25-	<CG>	M_26-

Connector 5 (160-210mm) Type B-25 connector (long through pins)

1	M_27+	M_28+	M_29+	M_30+	M_31+
2	M_27-	M_28-	M_29-	M_30-	M_31-
3	M_32+	<CG>	M_33+	M_34+	M_35+
4	M_32-	<CG>	M_33-	M_34-	M_35-
5	M_36+	M_37+	M_38+	M_39+	M_40+
6	M_36-	M_37-	M_38-	M_39-	M_40-
7	M_41+	M_42+	M_43+	<CG>	M_44+
8	M_41-	M_42-	M_43-	<CG>	M_44-
9	M_45+	M_46+	M_47+	M_48+	M_49+
10	M_45-	M_46-	M_47-	M_48-	M_49-
11	M_50+	M_51+	<CG>	M_52+	M_53+
12	M_50-	M_51-	<CG>	M_52-	M_53-
13	<G>	M_54+	M_55+	M_56+	M_57+
14	P8_0	M_54-	M_55-	M_56-	M_57-
15	P8_1	<G>	<CG>	M_59+	M_60+
16	P8_2	M_58+	<CG>	M_59-	M_60-
17	P8_3	M_58-	M_61+	M_62+	M_63+

18	P8_4	<G>	M_61-	M_62-	M_63-
19	P8_5	M_64+	M_65+	<CG>	M_66+
20	P8_6	M_64-	M_65-	M_68+	M_66-
21	P8_7	<G>	M_67+	M_68-	M_69+
22	P8_8	<G>	M_67-	M_71+	M_69-
23	P8_9	P9_0	M_70+	M_71-	M_72+
24	P8_10	P9_1	M_70-	M_73+	M_72-
25	P8_11	P9_2	<G>	M_73-	M_74+

Connector 6 (210-248mm) Type B-19 connector (long through pins)

1	P8_12	<G>	P9_3	M_75+	M_74-
2	P8_13	P9_4	<G>	M_75-	<CG>
3	P8_14	<G>	P9_5	M_76+	<CG>
4	P8_15	P9_6	<G>	M_76-	M_77+
5	P8_16	<G>	P9_7	<G>	M_77-
6	P8_17	P9_8	<G>	P10_0	M_78+
7	P8_18	<G>	P9_9	P10_1	M_78-
8	P8_19	P9_10	<G>	P10_2	<CG>
9	P8_20	<G>	P9_11	P10_3	M_79+
10	P8_21	P9_12	P10_4	<G>	M_79-
11	P8_22	<G>	P9_13	P10_5	M_80+
12	P8_23	P9_14	P10_6	<G>	M_80-
13	P8_24	<G>	P9_15	P10_7	<G>
14	M_81+	P9_16	P10_8	<G>	P11_0
15	M_81-	<G>	P9_17	P10_9	P11_1
16	M_82+	P9_18	P10_10	<G>	P11_2
17	M_82-	<G>	P9_19	P10_11	P11_3
18	M_83+	P9_20	P10_12	<G>	P11_4
19	M_83-	<G>	P9_21	P10_13	P11_5

Connector 7 (248-286mm) Type B-19 connector (short through pins)

1	<G>	P9_22	<G>	P10_14	P11_6
2	<G>	P9_23	P10_15	<G>	P11_7
3		P9_24	<G>	P10_16	P11_8
4			P10_17	<G>	P11_9
5			<G>	P10_18	P11_10
6			P10_19	<G>	P11_11
7			<G>	P10_20	P11_12
8			P10_21	<G>	P11_13
9	<G>	<G>	<G>	P10_22	P11_14
10	P12_0	P13_0	P10_23	<G>	P11_15
11	P12_1	<G>	P13_1	P10_24	P11_16
12	P12_2	P13_2	P14_0	<G>	P11_17
13	P12_3	<G>	P13_3	P14_1	P11_18
14	P12_4	P13_4	P14_2	<G>	P11_19
15	P12_5	<G>	P13_5	P14_3	P11_20
16	P12_6	P13_6	P14_4	<G>	P11_21
17	P12_7	<G>	P13_7	P14_5	P11_22
18	P12_8	P13_8	P14_6	<G>	P11_23
19	P12_9	<G>	P13_9	P14_7	P11_24

Connector 8 (286-336mm) Type B-25 connector (short through pins)

1	P12_10	P13_10	P14_8	<G>	P15_0
2	P12_11	<G>	P13_11	P14_9	P15_1
3	P12_12	P13_12	P14_10	<G>	P15_2
4	P12_13	<G>	P13_13	P14_11	P15_3
5	P12_14	P13_14	P14_12	<G>	P15_4
6	P12_15	<G>	P13_15	P14_13	P15_5
7	P12_16	P13_16	P14_14	<G>	P15_6

8	P12_17	<G>	P13_17	P14_15	P15_7
9	P12_18	P13_18	P14_16	<G>	P15_8
10	P12_19	<G>	P13_19	P14_17	P15_9
11	P12_20	P13_20	P14_18	<G>	P15_10
12	P12_21	<G>	P13_21	P14_19	P15_11
13	P12_22	P13_22	P14_20	<G>	P15_12
14	P12_23	<G>	P13_23	P14_21	P15_13
15	P12_24	P13_24	P14_22	<G>	P15_14
16			<G>	P14_23	P15_15
17			P14_24	<G>	P15_16
18					P15_17
19				<G>	P15_18
20					P15_19
21				<G>	P15_20
22					P15_21
23	<G>	<G>	<G>	<G>	P15_22
24	CAN+	<G>	TTC+	<G>	P15_23
25	CAN-	<G>	TTC-	<G>	P15_24

Connector 9 (336-361mm) Type D (N) connector

2	+3.3V
6	Power GND
10	+5.0V

Appendix C: CPM/JEM connector layout

Pos.	A	B	C	D	E

Guide Pin (0-8mm) (AMP parts 223956-1, 223957-1, or equivalent)

Connector 1 (8-58mm) Type B-25 connector (short through-pins)

1	SMM0	<G>	VMED00	VMED08	VMED09
2	SMM1	VMED01	VMED02	VMED10	VMED11
3	SMM2	<G>	VMED03	VMED12	VMED13
4	SMM3	VMED04	VMED05	VMED14	VMED15
5	SMM4	<G>	VMED06	VMEA23	VMEA22
6	SMM5	VMED07	<G>	VMEA21	VMEA20
7	SMM6	<G>	VMEDS0*	<G>	<G>
8	SMM7	VMEWRITE*	<G>	VMEA18	VMEA19
9	SMM8	<G>	VMEDTACK*	VMEA16	VMEA17
10	SMM9	VMEA07	VMEA06	VMEA14	VMEA15
11	SMM10	<G>	VMEA05	VMEA12	VMEA13
12	SMM11	VMEA04	VMEA03	VMEA10	VMEA11
13	SMM12	<G>	VMEA02	VMEA08	VMEA09
14	SMM13	VMERESET*	VMEA01	<G>	<G>
15	SMM14	<G>	<G>	FL0	FR0
16	SMM15	FL1	FL2	<G>	FR1
17	SMM16	<G>	FL3	FR2	FR3
18	SMM17	FL4	FL5	<G>	FR4
19	SMM18	<G>	FL6	FR5	FR6
20	SMM19	FL7	FL8	<G>	FR7
21	SMM20	<G>	FL9	FR8	FR9
22	SMM21	FL10	FL11	<G>	FR10
23	SMM22	<G>	FL12	FR11	FR12
24	SMM23	FL13	FL14	<G>	FR13
25	SMM24	<G>	FL15	FR14	FR15

Connector 2 (58-96mm) Type B-19 connector (mixed short/long through pins)

1	FL16	FL17	FR16	<G>	FR17
2	FL18	<G>	FL19	FR18	FR19
3	FL20	FL21	FR20	<G>	FR21
4	FL22	<G>	FL23	FR22	FR23
5	FL24	FL25	FR24	<G>	FR25
6	FL26	<G>	FL27	FR26	FR27
7	FL28	FL29	FR28	<G>	FR29
8	FL30	<G>	FL31	FR30	FR31
9	FL32	FL33	FR32	<G>	FR33
10	GEOADD5	<G>	GEOADD4	<G>	GEOADD3
11	1+ Cable 1	1-	<SG>	2+	2-
12	3+	3-	<SG>	4+	4-
13	1+ Cable 2	1-	<SG>	2+	2-
14	3+	3-	<SG>	4+	4-
15	1+ Cable 3	1-	<SG>	2+	2-
16	3+	3-	<SG>	4+	4-
17	1+ Cable 4	1-	<SG>	2+	2-
18	3+	3-	<SG>	4+	4-
19	GEOADD2	<G>	GEOADD1	<G>	GEOADD0

Connector 3 (96-134mm) Type B-19 connector (mixed short/long through pins)

1	FL34	FL35	FR34	<G>	FR35
2	FL36	<G>	FL37	FR36	FR37

3	FL38	FL39	FR38	<G>	FR39
4	FL40	<G>	FL41	FR40	FR41
5	FL42	FL43	FR42	<G>	FR43
6	FL44	<G>	FL45	FR44	FR45
7	FL46	FL47	FR46	<G>	FR47
8	FL48	<G>	FL49	FR48	FR49
9	FL50	FL51	FR50	<G>	FR51
10	<G>	<G>	<G>	<G>	<G>
11	1+ Cable 5	1-	<SG>	2+	2-
12	3+	3-	<SG>	4+	4-
13	1+ Cable 6	1-	<SG>	2+	2-
14	3+	3-	<SG>	4+	4-
15	1+ Cable 7	1-	<SG>	2+	2-
16	3+	3-	<SG>	4+	4-
17	1+ Cable 8	1-	<SG>	2+	2-
18	3+	3-	<SG>	4+	4-
19	<G>	<G>	<G>	<G>	<G>

Connector 4 (134-172mm) Type B-19 connector (short through pins)

1	FL52	FL53	FR52	<G>	FR53
2	FL54	<G>	FL55	FR54	FR55
3	FL56	FL57	FR56	<G>	FR57
4	FL58	<G>	FL59	FR58	FR59
5	FL60	FL61	FR60	<G>	FR61
6	FL62	<G>	FL63	FR62	FR63
7	FL64	FL65	FR64	<G>	FR65
8	FL66	<G>	FL67	FR66	FR67
9	FL68	FL69	FR68	<G>	FR69
10	<G>	<G>	<G>	<G>	<G>
11	1+ Cable 9	1-	<SG>	2+	2-
12	3+	3-	<SG>	4+	4-
13	1+ Cable 10	1-	<SG>	2+	2-
14	3+	3-	<SG>	4+	4-
15	1+ Cable 11	1-	<SG>	2+	2-
16	3+	3-	<SG>	4+	4-
17	1+ Cable 12	1-	<SG>	2+	2-
18	3+	3-	<SG>	4+	4-
19	<G>	<G>	<G>	<G>	<G>

Connector 5 (172-210mm) Type B-19 connector (mixed short/long through pins)

1	FL70	FL71	FR70	<G>	FR71
2	FL72	<G>	FL73	FR72	FR73
3	FL74	FL75	FR74	<G>	FR75
4	FL76	<G>	FL77	FR76	FR77
5	FL78	FL79	FR78	<G>	FR79
6	FL80	<G>	FL81	FR80	FR81
7	FL82	FL83	FR82	<G>	FR83
8	FL84	<G>	FL85	FR84	FR85
9	FL86	FL87	FR86	<G>	FR87
10	<G>	<G>	<G>	<G>	<G>
11	1+ Cable 13	1-	<SG>	2+	2-
12	3+	3-	<SG>	4+	4-
13	1+ Cable 14	1-	<SG>	2+	2-
14	3+	3-	<SG>	4+	4-
15	1+ Cable 15	1-	<SG>	2+	2-
16	3+	3-	<SG>	4+	4-
17	1+ Cable 16	1-	<SG>	2+	2-
18	3+	3-	<SG>	4+	4-
19	<G>	<G>	<G>	<G>	<G>

Connector 6 (210-248mm) Type B-19 connector (mixed short/long through pins)

1	FL88	FL89	FR88	<G>	FR89
2	FL90	<G>	FL91	FR90	FR91
3	FL92	FL93	FR92	<G>	FR93
4	FL94	<G>	FL95	FR94	FR95
5	FL96	FL97	FR96	<G>	FR97
6	FL98	<G>	FL99	FR98	FR99
7	FL100	FL101	FR100	<G>	FR101
8	FL102	<G>	FL103	FR102	FR103
9	FL104	FL105	FR104	<G>	FR105
10	<G>	<G>	<G>	<G>	<G>
11	1+ Cable 17	1-	<SG>	2+	2-
12	3+	3-	<SG>	4+	4-
13	1+ Cable 18	1-	<SG>	2+	2-
14	3+	3-	<SG>	4+	4-
15	1+ Cable 19	1-	<SG>	2+	2-
16	3+	3-	<SG>	4+	4-
17	1+ Cable 20	1-	<SG>	2+	2-
18	3+	3-	<SG>	4+	4-
19	<G>	<G>	<G>	<G>	<G>

Connector 7 (248-286mm) Type B-19 connector (mixed short/long through pins)

1	FL106	FL107	FR106	<G>	FR107
2	FL108	<G>	FL109	FR108	FR109
3	FL110	FL111	FR110	<G>	FR111
4	FL112	<G>	FL113	FR112	FR113
5	FL114	FL115	FR114	<G>	FR115
6	FL116	<G>	FL117	FR116	FR117
7	FL118	FL119	FR118	<G>	FR119
8	FL120	<G>	FL121	FR120	FR121
9	FL122	FL123	FR122	<G>	FR123
10	<G>	<G>	<G>	FL124	FR124
11	1+ Cable 21	1-	<SG>	<G>	FR125
12	3+	3-	<SG>	FL125	FL126
13	1+ Cable 22	1-	<SG>	<G>	FR126
14	3+	3-	<SG>	FL127	FR127
15	1+ Cable 23	1-	<SG>	<G>	FR128
16	3+	3-	<SG>	FL128	FL129
17	1+ Cable 24	1-	<SG>	<G>	FR129
18	3+	3-	<SG>	FL130	FR130
19	<G>	<G>	<G>	FL131	FR131

Connector 8 (286-336mm) Type B-25 connector (short through pins)

1	FL132	FR132	FR133	<G>	JMM0
2	FL133	<G>	FL134	FR134	JMM1
3	FL135	FR135	FR136	<G>	JMM2
4	FL136	<G>	FL137	FR137	JMM3
5	FL138	FR138	FR139	<G>	JMM4
6	FL139	<G>	FL140	FR140	JMM5
7	FL141	FR141	FR142	<G>	JMM6
8	FL142	<G>	FL143	FR143	JMM7
9	FL144	FR144	FR145	<G>	JMM8
10	FL145	<G>	FL146	FR146	JMM9
11	FL147	FR147	FR148	<G>	JMM10
12	FL148	<G>	FL149	FR149	JMM11
13	FL150	FR150	FR151	<G>	JMM12
14	FL151	<G>	FL152	FR152	JMM13
15	FL153	FR153	FR154	<G>	JMM14
16	FL154	<G>	FL155	FR155	JMM15
17	FL156	FR156	FR157	<G>	JMM16
18	FL157	<G>	FL158	FR158	JMM17
19	FL159	FR159	FR160	<G>	JMM18
20	FL160	<G>	FL161	FR161	JMM19
21	FL162	FR162	FR163	<G>	JMM20
22	FL163	<G>	FL164	FR164	JMM21
23	<G>	<G>	<G>	<G>	JMM22
24	CAN+	<G>	TTC+	<G>	JMM23
25	CAN-	<G>	TTC-	<G>	JMM24

Connector 9 (336-361mm) Type D (N) connector

2	+3.3V
6	Power GND
10	+5.0V

Appendix D: TCM interface connector layout

Pos.	A	B	C	D	E

Guide Pin (0-8mm) (AMP parts 223956-1, 223957-1, or equivalent)

Connector 1 (8-46mm) Type B-19 connector (long through-pins)

1		<G>	VMED00	VMED08	VMED09
2		VMED01	VMED02	VMED10	VMED11
3			VMED03	VMED12	VMED13
4		VMED04	VMED05	VMED14	VMED15
5		<G>	VMED06	VMEA23	VMEA22
6		VMED07	<G>	VMEA21	VMEA20
7		<G>	VMEDS0*	<G>	<G>
8		VMEWRITE*	<G>	VMEA18	VMEA19
9			VMEDTACK*	VMEA16	VMEA17
10		VMEA07	VMEA06	VMEA14	VMEA15
11		<G>	VMEA05	VMEA12	VMEA13
12		VMEA04	VMEA03	VMEA10	VMEA11
13		<G>	VMEA02	VMEA08	VMEA09
14		VMERESET*	VMEA01	<G>	<G>
15					
16					
17					
18					
19	GEOADD6	GEOADD5	GEOADD4		

* Supplied by the TCM or an adapter to power VME-- bus terminators.

Connector 2 (286-336mm) Type B-22 connector (short through pins)

1					
2			<G>	TTC1+	TTC2+
3			<G>	TTC1-	TTC2-
4			<G>	TTC3+	TTC4+
5			<G>	TTC3-	TTC4-
6			<G>	TTC5+	TTC6+
7			<G>	TTC5-	TTC6-
8			<G>	TTC7+	TTC8+
9			<G>	TTC7-	TTC8-
10			<G>	TTC9+	TTC10+
11			<G>	TTC9-	TTC10-
12			<G>	TTC11+	TTC12+
13			<G>	TTC11-	TTC12-
14			<G>	TTC13+	TTC14+
15			<G>	TTC13-	TTC14-
16			<G>	TTC15+	TTC16+
17			<G>	TTC15-	TTC16-
18			<G>	TTC17+	TTC18+
19			<G>	TTC17-	TTC18-
20	<G>	<G>	<G>	TTC19+	TTC20+
21	CAN+	<G>	<G>	TTC19-	TTC20-
22	CAN-	<G>	<G>		

Connector 3 (336-361mm) Type D (N) connector

2	+3.3V
6	Power GND
10	+5.0V

Appendix E: Design checklist for manufacturer

The following design checklist is provided for the manufacturer to assist in the tendering and manufacturing processes.

Mechanical specifications

- The Processor Backplane (PB) is to be installed in a 9U by 84HP chassis, with dimensions according to the IEEE 1101.10 specification.
- The board dimensions are 425 mm wide and 399.2 mm high, with module spacing of 20.32 mm (4 HP) in accordance with IEEE 1101.10, BS 5954 part 3, IEC 297 section 3.
- There are no “keepout” areas or cutouts on the PB.
- The PB printed circuit board has a thickness of 5.8 mm.
- The PB has 18 layers, comprising eight signal layers and ten ground planes.

Connectors

- The PB is populated almost entirely by 2mm HM connectors. Exceptions are two 160 position enhanced Eurocard assemblies in positions 1 and 2, a 9 pin D-sub connector in position 21, and a six-pin rotary switch near position 2.
- Daughter modules have 4 HP (0.8”) spacing. The 2mm HM connectors in each board position are distributed vertically according to the 2 mm grid spacing, with no gaps between them.
- The connector placement and pinouts depend on the daughter board position, and are detailed in Appendices A through D.
- A guide pin (AMP 223956-1 or equivalent) at the top of each position provides alignment during insertion of daughter modules.
- Up to 384 4-pair 2mm HM cable assemblies are received on the back side of the PB. To do this, 96 custom B-19 connectors with 8 rows of feed-through pins each are used. The remaining 11 rows of these connectors do not have long tails. An **8-row, non-latching shroud** mounted behind the backplane is required to receive the cable assemblies. These shrouds may be custom-ordered, or cut from larger, standard shrouds. If a polarised shroud is chosen, the polarisation key must be adjacent to column a.
- In slots 3 to 19, connector Jxx7 is a custom B-19 connectors with feed-through pins and shroud. Unlike Jxx2 to Jxx6, only the cables in columns a and b carry signals. So for connector Jxx7 in these slots, **columns d and e must be clipped short** before they are press-fit. A total of 176 custom connectors must be modified this way. The manufacturer will provide a rig for this purpose.
- The mating length for the cable feed-through pins, after subtracting backplane and shroud thickness, should be at least 5.3 mm.
- A power connector with three DIN cavities (ERNI 140-147 or equivalent) at the bottom of each position provides +5V, 3.3V and power ground, with a capacity of up to 40A per pin. The power pins are connected to bus bars mounted behind the backplane.

Printed Circuit Board

- The backplane is an 18 layer construction up to 5.8mm thick, with eight signal layers and ten ground layers. Impedance control shall be applied to all signal tracks.
- There are no unusual height restrictions or environmental considerations.
- The impedance of single-ended transmission lines shall be 60 Ω ±5%
- The differential signals will have characteristic impedance of 100 Ω ±5% differential.
- The connector hole and plating grade will be in accordance with IEC 1076-4-101.
- Solder masks are foreseen for both sides of the PCB.
- Both sides of the PCB have silkscreen layers.

Electrical Specifications

- The backplane carries no power. Daughter modules in the crate receive power through high-current connectors from separate bus bars mounted in the crate behind the backplane.
- No active or passive termination takes place on the backplane PCB itself
- There are no active components or LEDs on the backplane.
- The maximum signal frequency is 160 MHz. This is only over point-to-point links.

Miscellaneous

- All connections must be tested for short circuits and connectivity. Impedance of selected lines should also be verified.
- User documentation for the backplane is provided by the customer. The manufacturer will make available the production and test data for each backplane produced.

Appendix F: Bill of Materials

This document is an approximate bill of materials (BOM) for obtaining a cost estimate for the ATLAS Level-1 Trigger Processor Backplane (PB).

Item #	Description	MFG item number, if applicable	Qty per Assembly
1	PB printed circuit board	ATLAS-PB-PCB (see Appendix G)	1.00
2	Custom B-19 2mm HM male connector	Provided by customer*	96.00
3	8-row, unpolarised cable shroud	Custom, or cut larger shroud**	96.00
4	Guide Pin	AMP 223956-1	21.00
5	Backplane connector with 3 DIN cavities	ERNI 140-147 or equiv.	21.00
6	High current contact	AMP 1393589-1 or equiv.	42.00
7	High current contact, first make/last break	AMP 148532-1 or equiv.	21.00
8	Male connector type B-25	ERNI 053-008 or equiv.	36.00
9	Male connector B-22	ERNI 914-796 or equiv.	3.00
10	Male connector B-19	ERNI 103-670 or equiv.	14.00
11	Male connector B-19 feed-thru	ERNI 923-132 or equiv	5.00
12	Shroud for B-19 connector	AMP 646481-1 or equiv.	5.00
13	Male connector B-25, feed-thru	ERNI 064-522 or equiv.	2.00
14	Shroud for B-25 connector	AMP 646479-1 or equiv.	2.00
15	160 position enhanced Eurocard assy.	Harting 0202-160-2301 or equiv.	2.00
16	5-row shroud, Eurocard	Harting 0244-000-0004 or equiv.	2.00
17	Rotary switch	Provided by customer	1.00
18	9-pin D-sub connector	AMP 2-1393732-9 or equiv.	1.00
19	PEM studs for mounting guide pins	-	21.00

* 16 of the 96 custom connectors (the bottom row) need to have the pins in columns d and e to be clipped short (16 pins total) so that they do not have long through pins. This is to be done by the manufacturer, preferably with a rig built for this purpose.

** The 8-row shrouds in row 3 of the BOM are not standard parts. They must either be custom ordered, or cut by the manufacturer from larger, standard shrouds. If the cut shroud option is pursued, the standard shrouds used must be constructed of durable, high-quality plastic. If polarised shrouds are used, the customer should be consulted for the proper orientation.

All shrouds in any position must have equal thickness in order to maximise usable pin height. The minimum pin height with PCB and shroud thickness subtracted should be at least 5.3 mm.

Appendix G: PCB Quote Sheet

The following quote sheet provides an approximate description of the PB printed circuit board (PCB) for the manufacturer, to assist in the tendering and manufacturing processes.

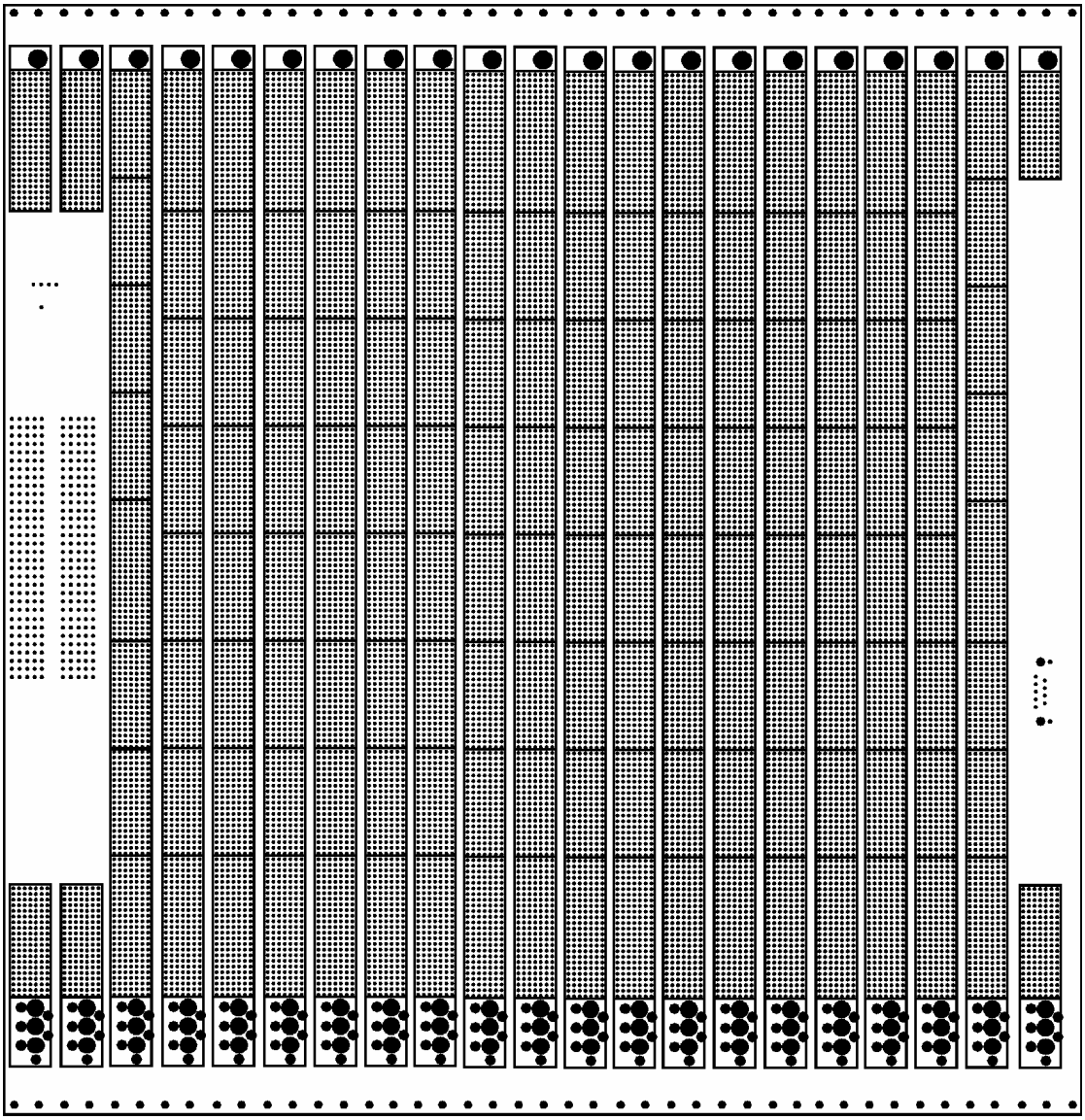
Part Number	ATLAS-PB-PCB
Size	399.2 mm x 425 mm
Thickness	5.8 mm
Number of Layers	18 (8 signal, 10 ground planes)
Number of Holes	~ 22 300
Number of Hole Sizes	10 (4 plated, 6 unplated)
Surface Mount Test Points, Top	0
Surface Mount Test Points, Bottom	84
Solder Mask	2 sides
Silk Screen	2 sides
Quantities	11 final production

Testing: All nets to be tested for connectivity and short circuits. Impedance must be be tested on selected nets to verify that the PCB meets specifications. Test data must be made available to the customer on request.

Special Instructions: Require 60Ω and 50Ω single-ended trace impedances, tolerance ±5%. PCB holes must be drilled and plated to press-fit tolerances according to IEC 1076-4-101

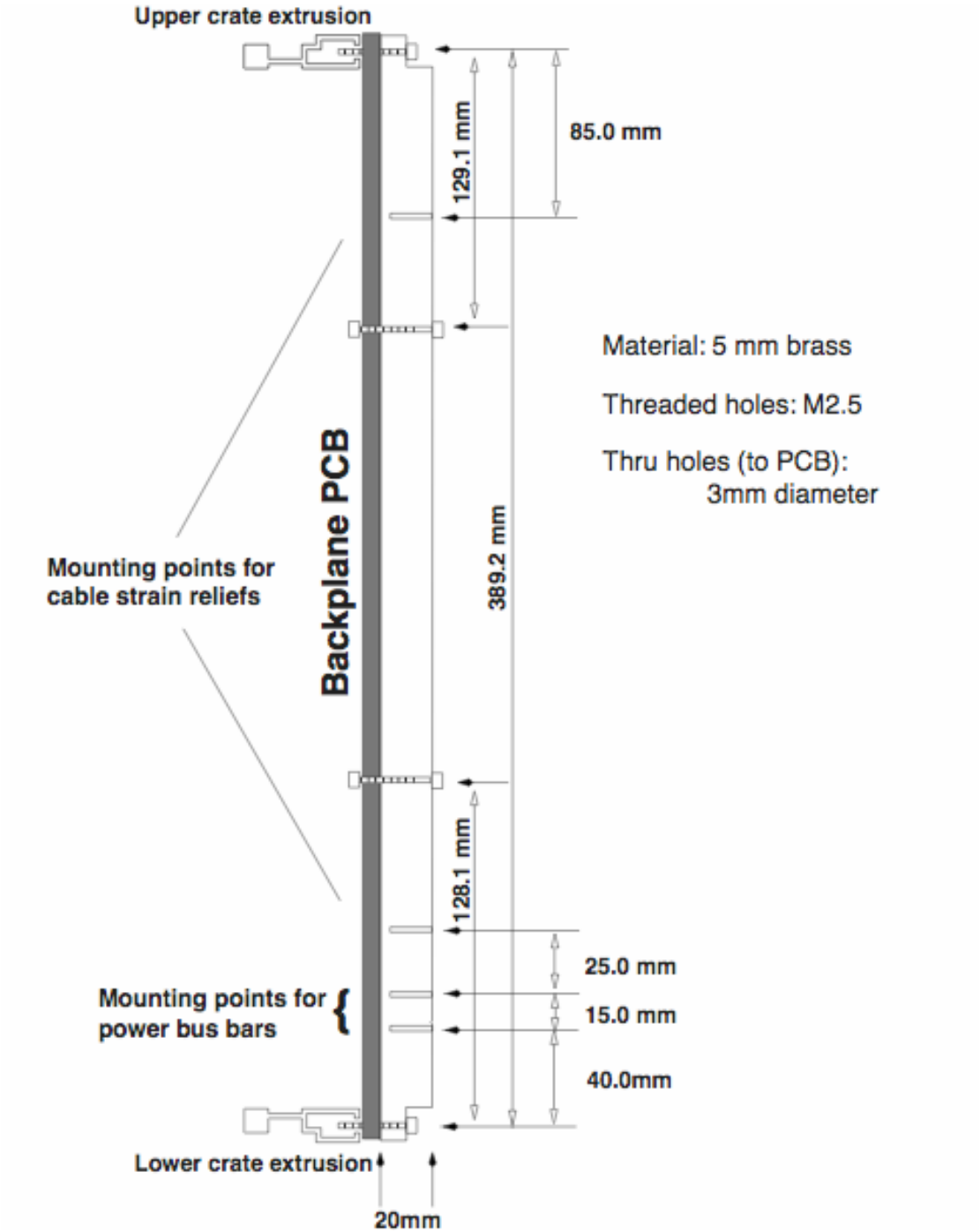
Appendix H: Sketch of PB printed circuit board

The following figure is an approximate drawing of the PB printed circuit board, seen from the front side. The position numbering (1 to 21) is from left to right. The small component near position 1 is a switch mounted on the back of the PCB to set the crate address, and in position 21 a 9-pin D-sub connector is mounted on the back of the plane for a cable connection to the CAN bus.



Appendix I: Sketch of PB support hardware

The following figure is an approximate drawing of the support hardware for the Processor Backplane. The vertical support ribs are made of 5mm brass, and are designed to fit between module positions behind the backplane. Bolts at the top and bottom pass through the PB mounting holes to the crate extrusions, and two retaining bolts at 1/3 and 2/3 of the PCB height prevent the PCB from flexing during module extraction. Holes with M2.5 threads provide mounting points for the power bus bars and the cable strain relief assemblies. Provision is made on the PB for six support ribs spaced in intervals of three module positions, with the first rib between positions 3 and 4.



Appendix J: Vertical positions of module connectors

The following diagram shows the vertical reference coordinates for module connectors in different PB positions, relative to the module centerlines.