# ATLAS Level-1 Calorimeter Trigger

# Clock Alignment Module (CAM)

### A module for Automating CPM - CPM clock synchronisation.

# Design Specification

Version: 1.01
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# Table of Contents



# Document History

Draft 7c. Programming of CANuC via front-panel connector added.
Version 1.0. CANuC Daughter card detail added. Test section updated.

Updates to this document “CAM_Specification.pdf” and other information can be found at:

http://www.ep.ph.bham.ac.uk/user/staley/CAM/

# 1 Introduction

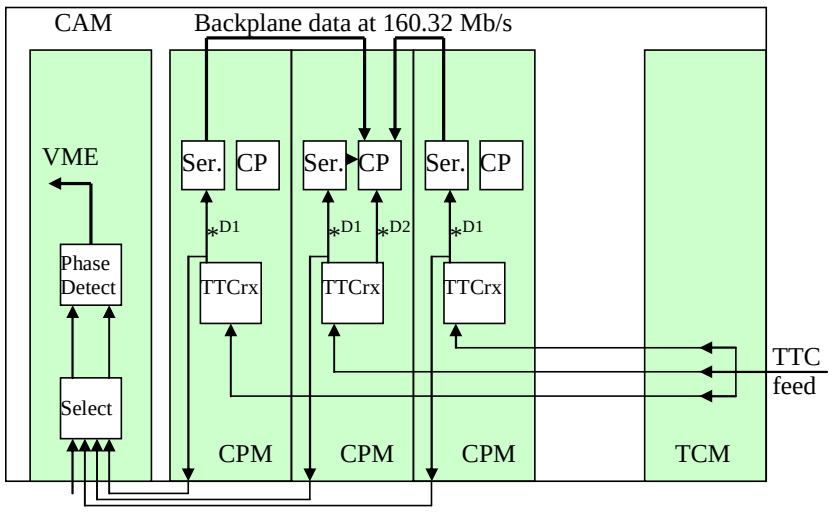
This document describes the specification for the Clock Alignment Module (CAM) to be used within the Processor Crates of the ATLAS Level-1 Calorimeter Trigger system.

Throughout this document 40MHz will be used as a shorthand for the actual TTC clock rate of 40.08 MHz, and likewise for the multiples of this frequency.

## 1.1 Overview

A Cluster Processor Crate contains 14 Cluster Processor Modules (CPMs), with each CPM exchanging data with its immediate neighbours using 160 outgoing and 160 incoming 160 Mb/s links. Each CPM contains 8 Cluster Processor Chips, each receiving data from modules in adjacent slots, left and right, as well as that being generated onboard from the incoming pre-processor data. These 160Mb/s links do not contain any timing information, but rely on the receiving clock being derived from the same source as the transmitting clock, namely the TTC feed. To maximise the timing margins, the phase of the clocks on adjacent modules must be aligned to within sub-nanosecond precision.

Each processor provides an accurate copy of its internal transmit clock for monitoring purposes. The CAM will use this copy to monitor the phase of the clock signal from each processor. Software will select which two clocks are to be compared, measure the phase difference, and adjust the phase of the clock on the source CPM using the programmable delay within its TTCrx.




*D1 = Deskew1 40.08 MHz clock

*D2 = Deskew2 40.08 MHz clock

Although the module is intended for the setting-up and monitoring of the clocks within a CP crate, it can also be used in a JP crate as the module will receive 16 clock inputs.

# 2 Requirements

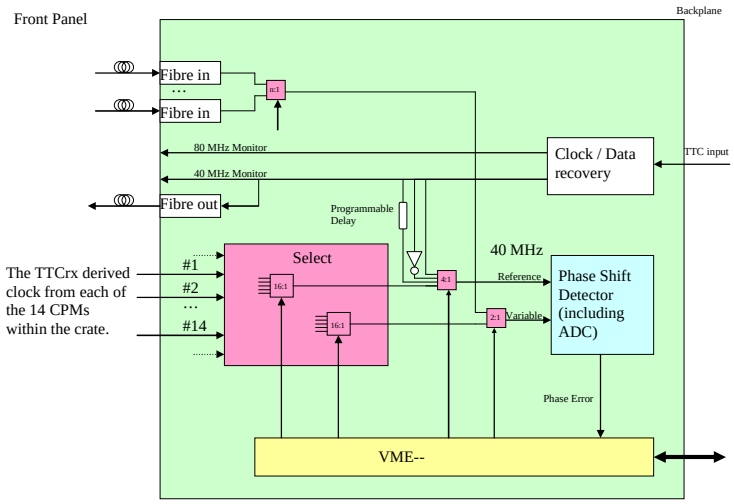
The CAM will be of 9U format i.e. 366mm high by 400mm deep and occupy the single unused ‘CPU/Slave’ slot of each processor crate.

The module will receive, via front panel cable, a clock signal from each of the processors within a crate. Any two of these clocks can be compared to produce a value representing the phase difference between them. A local reference derived from the backplane TTC signal may also be selected for comparison.

The CAM will provide the following functions:

- Receive 16 single-ended clock signals via the front panel using LEMO ‘00’ connectors
- Recover a high-stability local clock from the backplane TTC feed.
- Provide monitoring points for recovered 80MHz and 40MHz clocks.
- Transmit the local TTC clock onto fibre and to receive up to 3 of these clocks from other crates.
- Measure time difference between any two clocks with an accuracy better than 100ps
- VME-- compatible interface
- Front Panel JTAG access for testing and CPLD programming.
- Provide connectors to monitor the incoming busbar voltages.

These functions are illustrated in the diagram below:




The processor clocks are single-ended source terminated signals driven by 3.3V CMOS buffers. These will be suitably received and terminated by the CAM.

The phase detector will be edge-triggered to make it insensitive to mark-space ratios, and have a monotonic phase-voltage transfer function.

The local reference clock will be extracted from the TTC feed using a PECL based circuit. This path will also include a programmable delay to allow the phase of the incoming fibre clocks to be scanned.

Software will measure the phase relationship of the two clocks by sweeping the TTCrx delay on the CPM being ‘synchronised’. Reading the phase error value for each delay increment produces a plot from which will be found the optimum in-phase TTCrx setting.

The fibre-optic links allow the phase of TTC clocks from other crates to be measured and monitored.

# 3 Implementation

## 3.1 Clock Phase Measurement

The design will use PECL or LVPECL logic where appropriate. PECL style logic is fast enough not to obscure the 100ps time resolution of the TTCrx on the CPMs. LVPECL devices use a 3.3V supply and allow regulators to isolate the sensitive logic from the 5V crate supply.

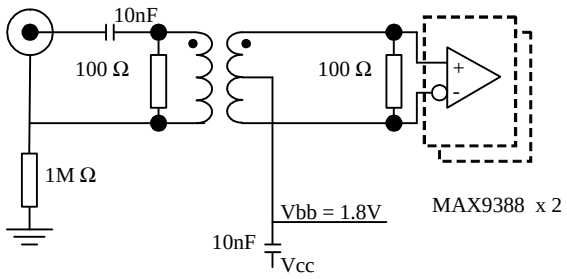
### 3.1.1 Input receivers / input circuitry

The clock monitoring output of a CPM is a single-ended source terminated signal from a 3.3V powered CMOS buffer.

The inputs to this card are AC terminated and then AC coupled into the receiver. With termination at either end, the signal swings at the connector are expected to be about 1.2V. The multiplexers chosen (MAX9388 or MC100EP57)[1] are sensitive enough not to require an extra input amplifier. Maximum input signal is 3 V p-p.

Sensitivity is 200 mV peak-peak swing at 50% duty-cycle ratio.
Because of the AC coupling, a different duty-cycle will require a larger swing due to the 'baseline wander' from the midpoint. For 25% - 75% duty-cycle the required sensitivity is double this figure.

Signal input is via a coaxial LEMO connector type OO, and terminated to 50 Ω as shown in the circuit below.




To avoid connecting together the grounds from different modules, a high-frequency transformer will be used to couple each input into the multiplexers. (Type T1-1T by Mini-circuits). The screen will be grounded via a high resistance to bleed away any static charge that could form on a floating cable. The connectors are insulated from the front panel.
An offset voltage of 50mV will be added across the differential inputs of the multiplexers to prevent them oscillating in the absence of a signal. This bias circuit is shown in Appendix C.

### 3.1.2 Clock selection

The two 16-way selection multiplexers will be constructed from two banks of 4:1 multiplexers with high-gain input stages. These are fed into another multiplexer to select between the processor clocks or other clock sources.

Any of 16 processor clocks or local TTC clock can be compared with any of 16 processor clocks or incoming Fibre clock. The following comparisons may be made:

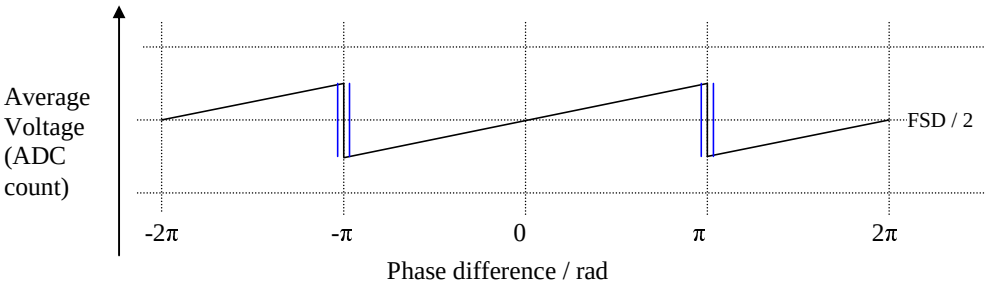
| Clock 1 - Reference | Clock 2 – 'variable' |
|---|---|
| 1 of 16 processor clocks<br>Or<br>Local clock (true , inverted or delayed) | 1 of 16 processor clocks<br>Or<br>1 of 3 Fibre-optic clock signals |

[1] The MAX9388 parts that were originally specified became unavailable so MC100EP57 parts were substituted

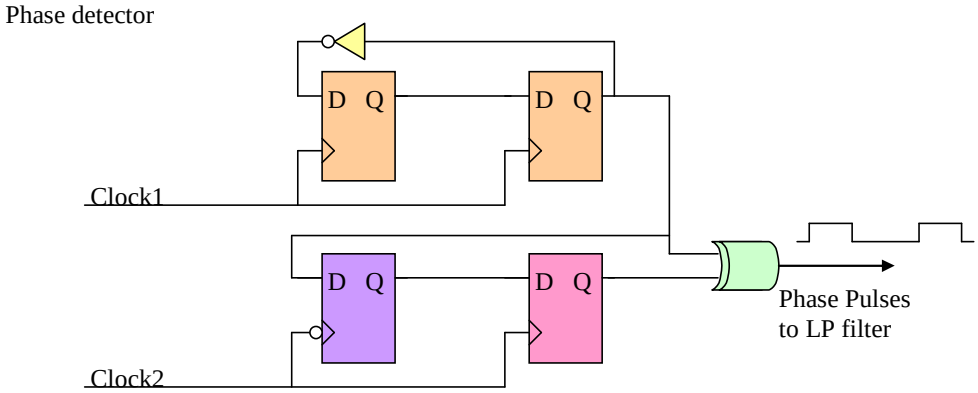
### 3.1.3 Phase shift detector

The clock phase difference is measured using a phase-detector that converts the phase information into a voltage, which is then digitised using an onboard ADC.

The phase shift detector logic produces a pulsed signal with a mark-space ratio dependant upon the phase difference. The pulsed output is fed into a low-pass filter to derive a voltage suitable for feeding the ADC. The characteristics of the phase detector is shown below:




The circuit chosen uses a standard exclusive-or phase detector preceded by D-type flip-flops to give a behaviour which does not have a dead-zone around the zero-phase point. The response around the zero-phase point is linear and unaffected by the mark-space ratio of the inputs. This characteristic is produced by dividing each clock by 4 before feeding into a traditional exclusive-or based phase detector. At the zero-phase point the phase detector receives two inputs in quadrature. Actually one clock signal is not divided by 4, but resampled by the other clock. The resampling is initially done using opposing clock edges to avoid metastable operation at the zero-phase point:




Due to the clock inversion of clock2, the phase wrap-around transition , nominally at π/-π, will depend upon the mark-space ratio of this clock. The wrap-around occurs when the rising edge of clock1 coincides with the falling edge of clock2.

### 3.1.4 Filter and ADC

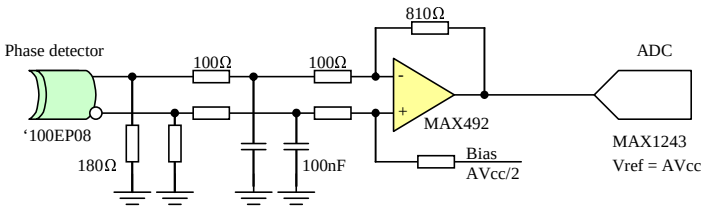
A Low-pass filter is necessary to remove high frequency components of the 20 MHz phase detector pulses. Given the ADC resolution is 10 bits, the attenuation should be greater than 1000.
If a simple RC circuit is used for the low-pass filter, then at 20 MHz Xc = R/1000.
This gives a RC time-constant of 8 μs.

The ADC will have a resolution of at least 10bits. This gives a resolution better than the TTCrx delay settings full-scale range of 8 bits over the clock period of 25 ns. For a 10 bit ADC , $2^{10}$ counts = 25ns , 1 count = 25ps.

The ADC chosen has serial I/O and a conversion time of 20uS. Control and conversion to parallel data is handled by firmware within the VME CPLD.

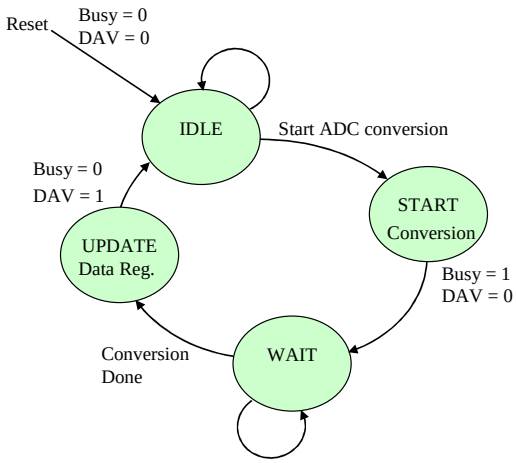
A stable, quiet power supply is provided for the analogue functions. The filter and following analogue circuitry will operate differentially on the phase detector logic to help reject noise from the logic power supply.

The ADC front-end pre-amplifier will take the form of:




Component value calculations are shown in Appendix B.

**ADC control state machine:**



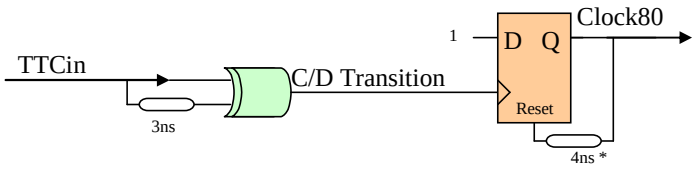

To start a conversion cycle, the StartConversion bit is set to '1' and then, after about 13us, the Data_Available (DAV) status bit will go to '1' indicating that the digitised value can be read from the ADC_Data_Register. During a conversion, the StartConversion bit of the control register will automatically be reset ready for another command, and the DAV status bit will go low until the new data is ready.

## 3.2 Local Reference Clock

### 3.2.1 TTC 80MHz Clock extraction circuit.

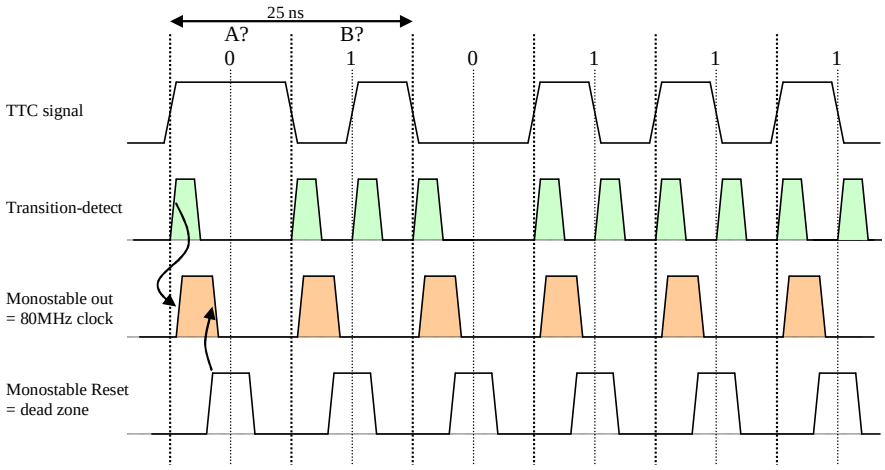
The front end will be built from very fast PECL logic that will extract and separate the 80MHz clock and data embedded in the TTC signal. From these signals a 40MHz clock with the correct phase will generated by examining the recovered Channel A/B data.

The 80MHz clock is recovered from the TTC signal using a transition detector feeding a monostable. The monostable is built using a D-type and delay line. The D-type circuit once triggered has a dead-time centred on the data transition, so will only trigger at a rate of 80MHz.



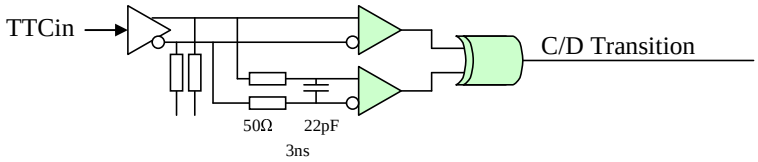

* This includes any transmission delay

Typical waveforms are shown below:



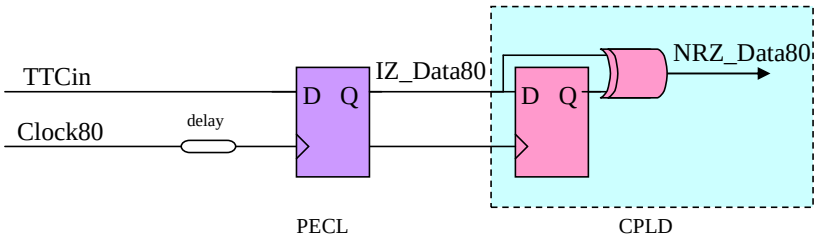

Implementation details

The LVPECL XOR gates have differential inputs. If these are used, the delay element chosen will be an RC circuit wired as follows:

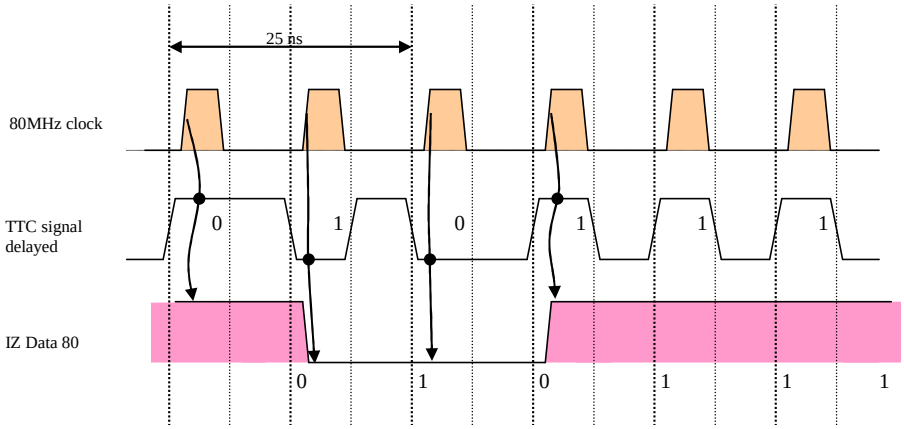



### 3.2.2 Data extraction

The RAW TTC signal is retimed by the recovered 80MHz clock to extract the data. The data is fed into a fast CMOS CPLD which contains the algorithm to identify the A and B channels. A CPLD allows the algorithm to be changed. (There are different algorithms described in the official TTC documentation) A PECL flip-flop samples the raw TTC signal to remove the embedded clock and ease the timing requirements of the CPLD.

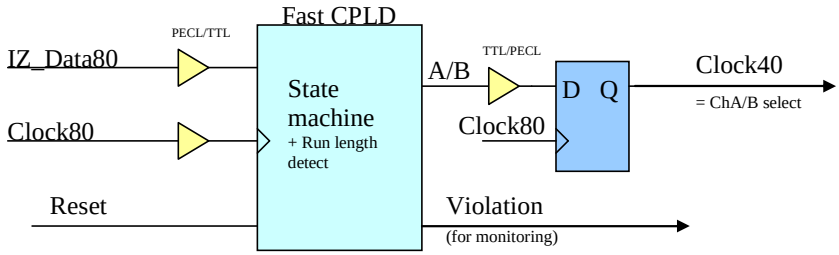



Sampling the TTC signal between a possible data transition and the clock transition produces data with an 'Invert on Zero' format (IZ). If successive samples are the same, then both a clock and data transition have occurred, meaning the data encoded is a '1'. If there has only been one transition, the data encoded is a '0'.




The IZ data is then 'differentiated' to produce the desired 'Non return to Zero' NRZ format.

### 3.2.3 Channel A/B alignment and 40 MHz clock generation



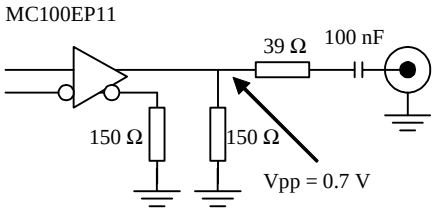

On reset or Power-up the circuit will examine TTC data and make an initial guess on A/B timeslot by assuming TTC system is sending IDLE code, i.e. alternating 1s and 0s.
Logic will monitor the data with respect to the 80MHz clock and delay the A/B signal by one cycle if an illegal sequence of Channel A/B is found.

The TTCrx manual gives conflicting advice on what sequence is illegal. The drawing quotes a length of AB data = (1,0) > 11 as illegal, but the text says A data = 1 > 23 is illegal.
The sequence of AB data = (1,0) will be used initially but can be changed inside the CPLD.

A PECL flip-flop retimes the CPLD signals to give the sub-nanosecond accuracy needed.

### 3.2.4 Onboard Clock monitoring

The TTC derived 80MHz and 40MHz clocks will be available on the front panel (via LEMO 00 connectors)
Circuit detail:




### 3.2.5 TTC Clock delay

The programmable delay chip MC100EP195 will be used to optionally insert an adjustable delay for the onboard TTC derived clock. This part has a delay range of 2.2 – 12.2 ns in 10ps increments using a 10 bit register.

A separate delay of 12.5 ns can be added by selecting an inverted version of the TTC clock.

## 3.3 Bench Test Modes

These modes allow connectivity not covered by JTAG testing to be checked on the test bench before the module is plugged into a crate. It also gives easy access to any high-speed signal during the evaluation of the design. The test modes are enabled using jumpers and require an oscilloscope and signal generator to complete the testing.

### 3.3.1 Clock selection and transmission test.

This mode will drive the clock selection address lines from a 6 bit counter cycling at 1ms. The connectivity of the clock selection circuitry can then be tested by applying an external test clock signal to each input in turn and observing the selected signals on test-points using an oscilloscope. Analogue effects such as crosstalk and signal transmission quality, and the behaviour of the phase-detector circuitry may also be checked.

| MuxTest mode | Test Links PL5 , PL4 | Reference clock select | Variable clock select | Fibre Tx |
|---|---|---|---|---|
| 0 | 0 , 0 | Normal / VME | Normal / VME | Off |
| 1 | 0 , 1 | Counter | Counter | ON |
| 2 | 1 , 0 | 0 | 0 | Off |
| 3 | 1 , 1 | 0 | 1 | Off |

### 3.3.2 ADC Test cycle.

This sets the ADC acquisition and readout to continuously cycle so that the timing of the serial bus can be checked.

| ADCTest mode | Test Links PL3 | ADC access |
|---|---|---|
| 0 | 0 | Normal / VME |
| 1 | 1 | Continuous |

## 3.4 Interfaces

### 3.4.1 Backplane

Backplane connectors will be the 2mm pitch Tyco Z-Pack type of equivalent compatible to IEC 1076-4-101. A 25 x 5 pin connector block is used for the VME connection, and a 22 x 5 pin connector block is used for the TTC feed. Both connector blocks will have upper and lower screens fitted.

A 3 pin Power block and a Guide block are also present. These conform to the published Backplane Specification which is copied in Appendix A.

The J2 VME64 connector is not required, and will not be fitted.

### 3.4.2 Front Panel

Ejectors/injector handles are the standard IEEE type such as those from ELMA as the insertion force is a third of that needed for a CPM.

#### *3.4.2.1 Indicators*

| Function | Colour | Quantity |
|---|---|---|
| Power supplies, Incoming 5V + Onboard 3.3V | Green | 2 |
| VME access | Yellow | 1 |
| L1A received | Yellow | 1 |
| TTC code violation / Error | Red | 1 |

#### *3.4.2.2 Connectors*

| Function | Type | Quantity |
|---|---|---|
| Clock inputs | LEMO coax | 16 |
| Fibre optic transmitter + receiver | SFP socket | 1 |
| Fibre optic receivers | SFP socket | 2 |
| Clock + Voltage monitor | LEMO dual coax | 2 |
| JTAG access – ALTERA Byteblaster pinout | 10 pin IDC | 1 |

**Clock inputs:**

AC coupled and terminated to 50 Ω with a sensitivity of 200mV peak to peak (p-p). Signal amplitude up to 2.4Vp-p. Expected signal swing from CPM is 1.2Vp-p.

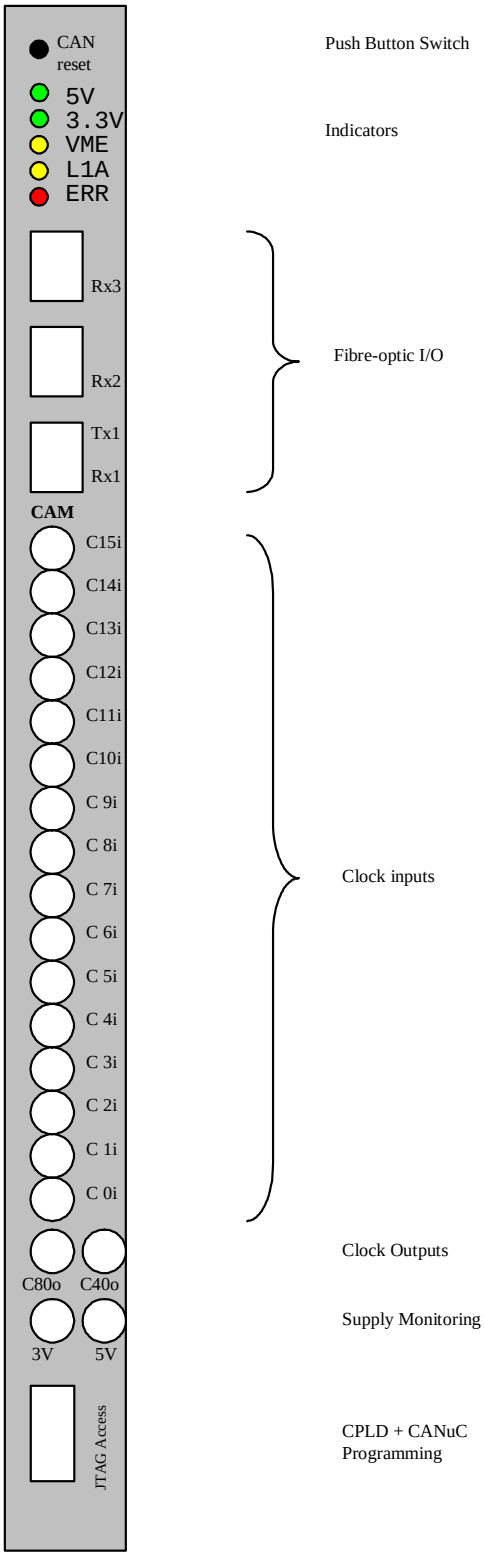
**Clock outputs:**

Driver circuit source impedance is 50 Ω in series with 0.1uF coupling capacitor and will drive 350mVp-p into a 50 Ω load.

**Voltage outputs**

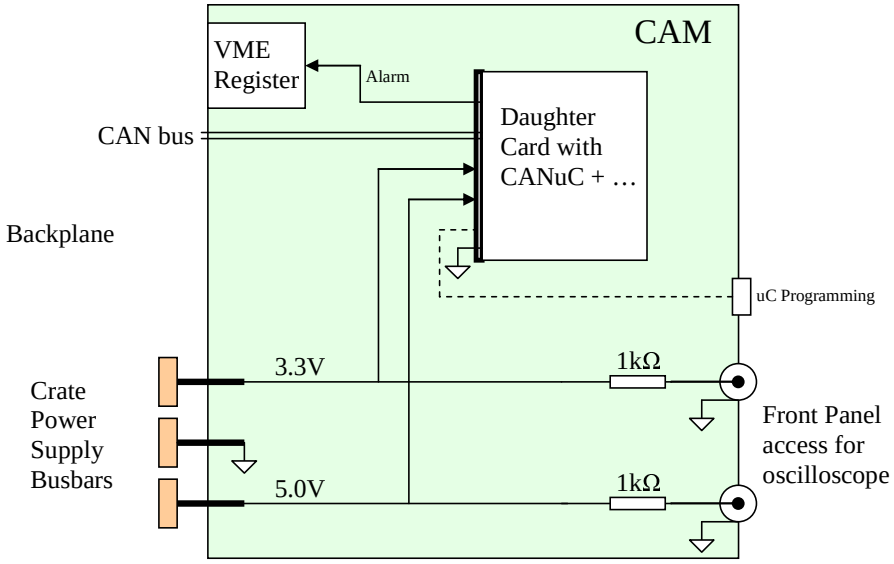
The incoming 5V and 3.3V supplies are passed onto front-panel Lemos via 1k resistors.
A daughtercard with a CANuC may be fitted to monitor these supplies and communicate with the backplane CAN bus. Detail of Daughter card connector and size given in Appendix B.

### *3.4.2.3 Layout*


CAN
reset
5V
3.3V
VME
L1A
ERR
Rx3
Rx2
Tx1
Rx1
CAM
C15i
C14i
C13i
C12i
C11i
C10i
C 9i
C 8i
C 7i
C 6i
C 5i
C 4i
C 3i
C 2i
C 1i
C 0i
C80o
C40o
3V
5V
JTAG Access
Push Button Switch
Indicators
Fibre-optic I/O
Clock inputs
Clock Outputs
Supply Monitoring
CPLD + CANuC
Programming

### 3.4.3 CAN Daughter Card

This holds a CANuC which will monitor the crate busbar voltage, and report any alarm conditions to the DCS via the TCM CANbus.




The ADC of the CANuC has 8 analogue inputs available, 5 of which are used as follows:

| Input | Signal | Full Scale Reading |
|---|---|---|
| AN0 | Crate 5.0V supply | 8.2V |
| AN1 | Crate 3.3V supply | 8.2V |
| AN2 | Onboard 3.3V supply | 8.2V |
| AN3 | Crate 5.0V oscillation amplitude | 400mV sinusoid peak |
| AN4 | Crate 3.3V oscillation amplitude | 400mV sinusoid peak |

The ADC is provided with a very stable reference (4.1V) for accurately measuring DC voltages.

A filter of bandwidth 0.5 to 3 kHz, plus an amplifier and rectifier circuit are used to detect oscillatory signals on the power supply voltage.

### 3.4.4 Power Supplies

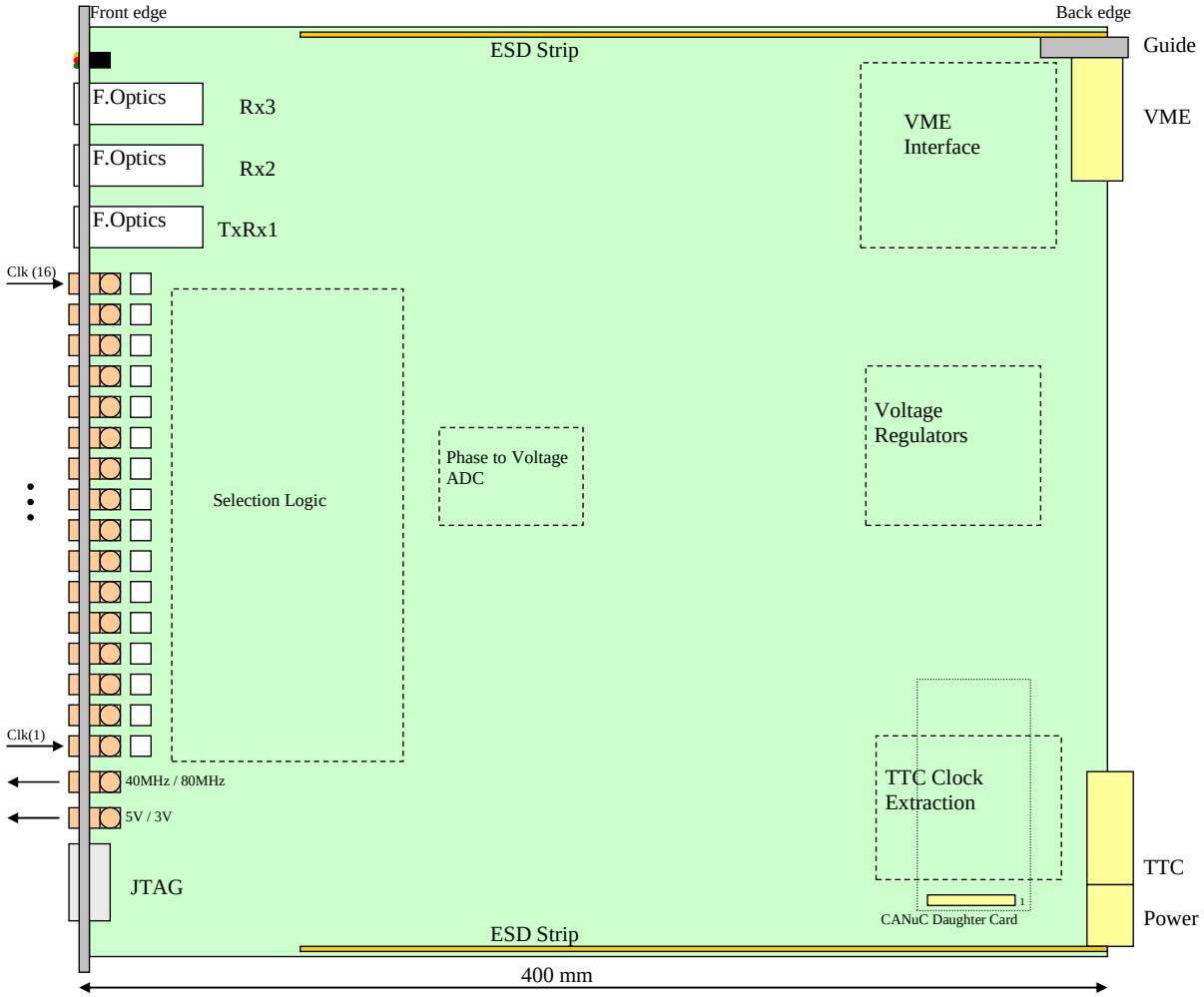
The onboard supplies will be derived from filtering the incoming crate 5V supply, with conversion down to 3.3V using linear regulators and switchers. Values are taken from devices' data sheet for $I_{EE}$ max at 25°C.

Current consumption - estimates

| | |
|---|---|
| Phase detector: | 1.70A. |
| VME interface: | 0.82 A. |
| TTC Clock extraction: | 0.65 A |
| Fibre Optic modules: | 0.33 A |

Power Estimate = Total current x 5V = 17.5W

## 3.5 Module Layout



## 3.6 VME—interface address map

VME base address at 0x0060000
Module will respond to a block of 128 word locations, not all used.

The DS* signal will be received by a buffer having sufficient hysteresis to remove any non-monotonic transitions that may be present on the backplane signal. The VME interface will be robust enough not to generate spurious cycles from glitches on this signal

The IACK* signal on slot2 will be ignored , as will the Geographical address lines, although these may be received by the address decoding CPLD.

### 3.6.1 Register map

Conforms to the L1 Calorimeter Trigger model:

| Type | Function name | Size (16 bit words) | VME address offset from base (Hex) |
|---|---|---|---|
| RO | Module ID A | 1 | 00000 |
| RO | Module ID B | 1 | 00002 |
| RO | Module Status | 1 | 00004 |
| R/W | Module Control | 1 | 00006 |
| R/W | Reference source | 1 | 00008 |
| R/W | TTC delay | 1 | 0000A |
| R/W | Variable source | 1 | 0000C |
| WO | Module Pulse | 1 | 0000E |
| RO | ADC Status | 1 | 00010 |
| R/W | ADC Control | 1 | 00012 |
| RO | ADC Data | 1 | 00014 |

#### *3.6.1.1 Module ID Register A*

A 16-bit register conforming to the LVL1 Calorimeter trigger module ID convention:

Bits 15 - 0: Module Type, CAM = 3380
These bits are set within a PLD.

#### *3.6.1.2 Module ID Register B*

A 16-bit register conforming to the LVL1 Calorimeter trigger module ID convention:

Bits 15-12: Firmware revision No
Bits 11- 8: PCB Module Revision No
Bits 7- 0: Serial Number in the range 0-255.

#### *3.6.1.3 Status Register*

A 16-bit read-only register reserved for module status information.

Bit 15: PS_ALERT from Daughter Card. (Not yet implemented)
Bit 7 - 6: Fibre SFP Module3: RX loss of signal , Module Removed.
Bit 5: Unused – read as zero.
Bit 4 - 3: Fibre SFP Module2: RX loss of signal , Module Removed.
Bit 2: Fibre SFP Module1: TX laser fault.
Bit 1 - 0: Fibre SFP Module1: RX loss of signal , Module Removed.

### 3.6.1.4 Control Register

A 16-bit read-write register containing static (non-pulsed) module controls.

Bits 15-2 Unused.
Bit 1: Set CANuC Programming mode. (Unavailable for Prototype CAM PC3380M/1)
Bit 0: Enable Fibre Transmitter in Module1.

### 3.6.1.5 Reference Source Register

A 6-bit read-write register containing static (non-pulsed) module controls.

Bits 15-6: Unused - read as zero.
Bits 5- 4: Type Selection. 0 = CPM, 1 = TTC, 2 = /TTC, 3 = TTC + ΔT.
Bits 3- 0: CPM/JEM Clock Selection. Processor #.

### 3.6.1.6 TTC Delay Register

A 10-bit read-write register containing ΔT value.

Bits 15-10: Unused - read as zero.
Bits 9- 0: ΔT in steps of 10ps from 2.2ns to 12.2ns

### 3.6.1.7 Variable Source Register

A 6-bit read-write register containing static (non-pulsed) module controls.

Bits 15-6: Unused - read as Zero.
Bits 5-4: Type Selection #. 0 = CPM , 1-3 = Fibre Rx 1 - 3
Bits 3- 0: CPM/JEM Clock Selection. Processor #.

### 3.6.1.8 Module Pulse Register

A 1-bit write only register containing transient or pulsed module controls.

Bits 15: 1 = Clear Bit 15 of module Status Register.
Bits 14- 0: Unused - read as Zero.

### 3.6.1.9 ADC Status Register

A 2-bit read-only register.

Bits 15- 2: Unused - read as Zero.
Bit 1: ADC Data available.
Bit 0: ADC Busy , conversion in progress

### 3.6.1.10 ADC Control Register

A 1-bit read-write register .

Bits 15-1: Unused - read as zero.
Bit 0: Start ADC conversion. Automatically cleared once a conversion has begun.

### 3.6.1.11 ADC Data Register

A 10-bit read-only register containing phase value from latest A/D conversion.

Bits 10-15: Unused - read as zero.
Bit 9 - 0: Phase value. In-phase clocks should give a value around 200h.

# 4 Project Management

## 4.1 Deliverables

The deliverable products of this phase of the project are:

- Specification (this document).
- 2 pre-production CAM followed by 8 production ( 4 CP + 2 JP + 2 spare)
- Firmware for programmable logic.
- Design documentation (schematics, layout information, component data-sheets etc.)

## 4.2 Personnel

The CAM is designed at Birmingham University, although closely coupled with layout effort at RAL. The main personnel for the project are named below, supported by several other members of the Level-1 Calorimeter Trigger Collaboration:

- Project Manager/Engineer: Richard Staley (Birmingham)
- Layout: (RAL Drawing Office)

## 4.3 Design and Verification

Cadence Concept HDL will be used for the schematic design of the module at Birmingham, remotely accessing the central RAL installation of this program. Altera Quartus will be used to create and test the firmware for the CPLDs.

The 80MHz clock extraction circuit and the phase detector and filter will be prototyped on a small PCB before manufacture.

## 4.4 Manufacturing

The PCB layout and routing will be done by the RAL Drawing Office, which also supervise the manufacture and assembly (population) of the module. RAL now has a ‘framework’ agreement with a number of companies who deal with the whole process of PCB manufacture, from component supply through to providing assembled modules. The “1-stop shop” agreement provides that any module failing our acceptance tests will be returned to the manufacturer and corrected at their expense

## 4.5 Test

The assembled modules from the manufacture will be delivered to Birmingham University, where the acceptance tests will be performed on the modules. These tests include visual checks, module power-up and JTAG programming of the two CPLD devices. Any failing module will be returned to the manufacturer for re-work.

Certain functions (clock selection, phase detector and TTC clock recovery) will first be tested on the workbench with the module running the inbuilt test modes using standard test equipment such as signal generators and an oscilloscope. Once these functions are verified then the module will be placed in the 9U crate for testing by software using the VME interface.

The CPM Extender may be used for holding the CAM provided the Ground links SB2 – SB4 and SB7 – SB10 on the Extender are removed.

Using the two prototype modules, the design will be evaluated before more modules are made; the characteristics of the phase detector will be checked, and the jitter of the PECL based clock extraction will be measured and compared to that of a TTCrx source.

## 4.6 Costs

| | NRE costs | Cost each in UKP |
|---|---|---|
| PCB (15 day turn-around) | £500 PCB + 2 x £200 Stencils | £523 (for 1st two ) then £216 |
| Components | | £735 |
| Assembly | | £168 |

# References


1. S.J.Hillier, G.Mahout, R.J.Staley & A.T.Watson, CPM Production Readiness Review document

# Appendix A – Backplane connector layout

The following information is derived from the Backplane PDR document for the CPU slots 1 & 2.

| Pos. | A | B | C | D | E |
|---|---|---|---|---|---|

Guide Pin (0-8mm) (AMP parts 223956-1, 223957-1, or equivalent)

Connector 1 (8-58mm) Type B-25 connector

| | | | | | |
|---|---|---|---|---|---|
| 1 | | <G> | VMED00 | VMED08 | VMED09 |
| 2 | BBSY* | VMED01 | VMED02 | VMED10 | VMED11 |
| 3 | BCLR* | | VMED03 | VMED12 | VMED13 |
| 4 | BG0IN* * | VMED04 | VMED05 | VMED14 | VMED15 |
| 5 | BG0OUT* ** | <G> | VMED06 | VMEA23 | VMEA22 |
| 6 | BG1IN* * | VMED07 | <G> | VMEA21 | VMEA20 |
| 7 | BG1OUT* ** | <G> | VMEDS0* | <G> | <G> |
| 8 | BG2IN* * | VMEWRITE* | <G> | VMEA18 | VMEA19 |
| 9 | BG2OUT* ** | | VMEDTACK* | VMEA16 | VMEA17 |
| 10 | BG3IN* * | VMEA07 | VMEA06 | VMEA14 | VMEA15 |
| 11 | BG3OUT* ** | <G> | VMEA05 | VMEA12 | VMEA13 |
| 12 | BR0* | VMEA04 | VMEA03 | VMEA10 | VMEA11 |
| 13 | BR1* | <G> | VMEA02 | VMEA08 | VMEA09 |
| 14 | BR2* | VMERESET* | VMEA01 | <G> | <G> |
| 15 | BR3* | <G> | | | |
| 16 | IACK* | <G> | | | |
| 17 | IACKIN* | <G> | | | |
| 18 | IACKOUT* | IRQ7* | | | |
| 19 | <G> | IRQ6* | | | |
| 20 | <G> | IRQ5* | | | |
| 21 | <G> | IRQ4* | | | |
| 22 | <G> | IRQ3* | | | |
| 23 | <G> | IRQ2* | | | |
| 24 | <G> | IRQ1* | | | |
| 25 | GEOADD6 | GEOADD5 | GEOADD4 | GEOADD0 | |

* Set low in Position 1 (bus master)
** Implemented only in Position 1

Connector 2 J2 VME64 connector

This will not be fitted

Connector 3 (292-336mm) Type B-22 connector

| | | | | | |
|---|---|---|---|---|---|
| 1-19 | | | | | |
| 20 | <G> | <G> | <G> | <G> | |
| 21 | CAN+ | <G> | TTC+ | <G> | |
| 22 | CAN- | <G> | TTC- | <G> | |

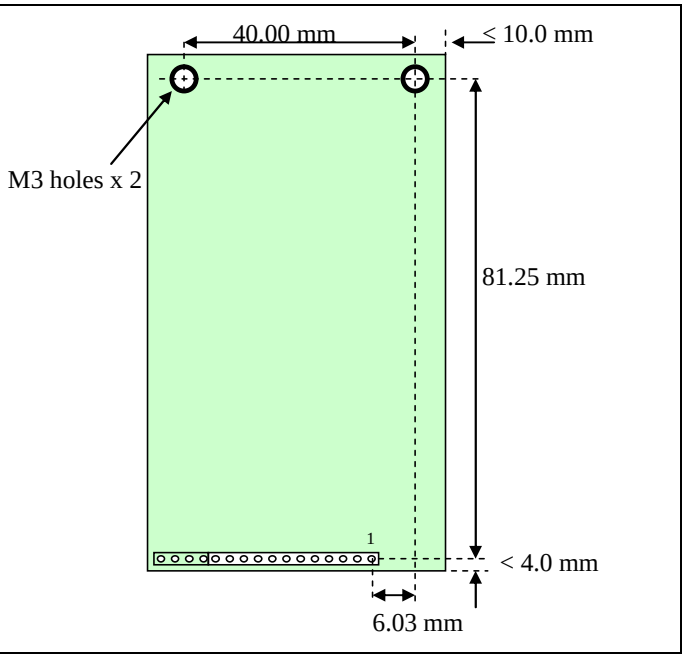
Connector 4 (336-361mm) Type D (N) connector

| | |
|---|---|
| 2 | +3.3V |
| 6 | Power GND |
| 10 | +5.0V |

# Appendix B – Daughtercard connector

Connector Pinout:

| Pos. | Signal (wrt daughter card) |
|---|---|
| 1 | CAN+ (i/o) |
| 2 | CAN- (i/o) |
| 3 | Ground |
| 4 | |
| 5 | 5.0V Supply (in) |
| 6 | 5.0V Supply (in) |
| 7 | RESET* (in) |
| 8 | 3.3V Supply (in) |
| 9 | |
| 10 | Alarm_2 (out) |
| 11 | PS_Alarm (out) |
| 12 | Ground |
| 13 | CAN_Prog* |
| 14 | Ground |
| 15 | RS232_OUT |
| 16 | RS232_IN |
| | |




Note: Prototype CAM has connector with only pins 1 – 12.

# Appendix C – Front-panel connector – JTAG & CANµC

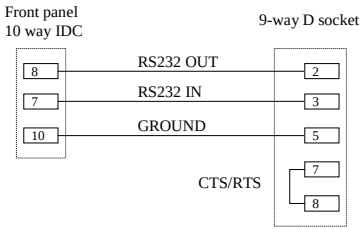
Connector Pinout:

| Pos. | Signal |
|---|---|
| 1 | JTAG_TCK |
| 2 | Ground |
| 3 | JTAG_TDO |
| 4 | 3.3V Supply |
| 5 | JTAG_TMS |
| 6 | |
| 7 | RS232_IN (*) |
| 8 | RS232_OUT (*) |
| 9 | JTAG_TDI |
| 10 | Ground |

### Programming uC

Due to lack of space on the front-panel, the CANuC is programmed using the same front-panel connector that carries the JTAG signals. An adaptor (shown below) is needed to convert this to the standard 9-way D-type connector pinout as used on the other L1Calo modules.

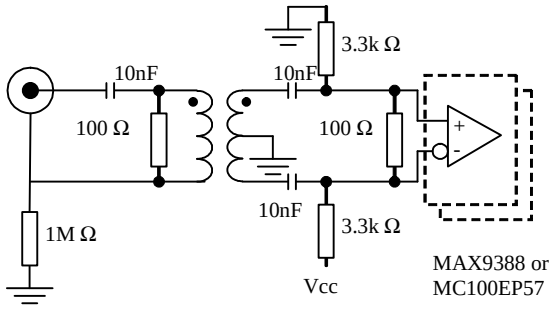
The RS232 signals(*) each have a 10 kΩ inline resistor on the module to protect certain variants of the ALTERA ByteBlaster interface that use these pins for other functions.



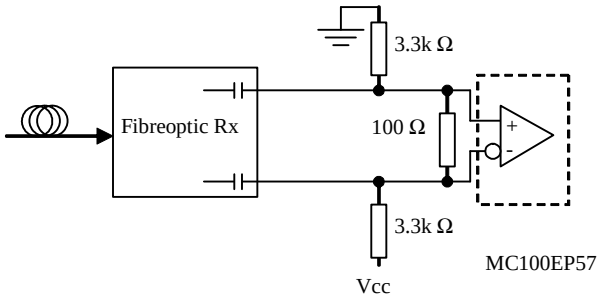

# Appendix D – Changes to prototype module.

The supply filter inductor now a wired ferrite bead instead of a chip inductor.

The differential inputs of the receivers for the 16 processor clocks were biased to the same voltage and thus prone to oscillation in the absence of a signal. The circuit was modified by breaking the transformer DC path and adding a bias network, to offset the inputs by 50mV:




The MAX9388 parts were on a very long lead time, and so were substituted by On-Semi MC100EP57 devices. These are functionally identical, but have a different bias network on their receiver inputs. This difference is important in one area: The fibreoptic receiver outputs are capacitively coupled, but the On-Semi parts have inputs that are pulled to ground. These need to be biased correctly using external resistors, and with a 50mV offset as per the clock inputs:




Four extra pins have been added to daughter card connector to allow programming of CANuC through the front panel.

A reset button for the CANuC has been added to front panel.