DAQ Test Plan

ATLAS Calorimeter Level-1 Trigger- Common Merger Module

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1 Scope

This document defines the Common Merger Module tests and measurements needed with the L1Calo DAQ system. The CMM and other related module specifications are available via the Level-1 trigger module web page, at http://hepwww.rl.ac.uk//Atlas-L1/Modules/Modules.html.

These tests apply to modules which have passed their hardware test programme, meaning that all module circuits and interfaces have been shown to work individually. The DAQ tests are indended to establish that modules work in a realistic realtime and DAQ environment with all parts of the module active concurrently.

All DAQ tests are carried out using the RAL test rig, in a 9U crate with custom backplane, using two CMMs, with a rear cable link available. One TCM is needed to generate timing and CANBus signals, and one CPM and one JEM to provide hit signals on the custom backplane. The test also requires the standard DAQ infrastructure (including 6U crate with CPU and TTC system; PC with DAQ software). Tests in section 3 and 4 require ROD readout. Tests in section 5 requre a full crate of 14 CPMs.

2 Timing tests

These tests are intended to verify the timing window sizes and realtime signal integrity when the module timings are correctly set up. All combinations indicated by section numbers in the following matrix must be tested:

Test	Crate-Summing			System-Summing		
	CP	Jet	Energy	CP	Jet	Energy
Backplane Timing	2.1	2.5	2.4	2.1	2.5	2.4
Cable Timing	n/a	n/a	n/a	2.2	2.2	2.2
CTP hit outputs	n/a	n/a	n/a	2.6	2.6	2.6
Residual Error Rate	2.3	2.3	2.3	2.3	2.3	2.3

2.1 Crate backplane timing window

- Set up a CMM backplane timing scan with CPM in slot 4 and JEM in slot 12 to exercise long and short backplane paths. Select CPM/JEM replay test vectors with hit patterns which populate all 24 hit bits cyclically.
- Perform timing calibrations of the backplane input signals of both CMMs by varying their deskew1 phase in 1ns steps and measuring the parity error rates. Confirm that the error-free window is at least 10ns wide. Record the measurement results in the database.
- Set the optimum combination of deskew1 phase and backplane strobe phase in each CMM.

This test should be performed three times, once each with the cluster-, jet- and energy-summing firmware, although there are not expected to be large timing differences.

Software to do timing scans in the multistep run framework is under development.

2.2 CMM - CMM cable timing window

- Set up a CMM cable timing scan. This test does not need a CPM or JEM, as CMM crate replay test vectors are used. The test hit patterns should populate the crate sum for all 24 hit bits cyclically. Disable all backplane inputs so that backplane parity errors are not counted.
- Perform a timing calibration of the cable input signal of the CMM under test by varying the deskew2 phase and measuring the parity error rates. Confirm that the error-free window is at least 15ns wide. Record the measurement results in the database.
- Set the optimum deskew2 phase and cable strobe phase in the test CMM. Set an equivalent crate-to-system pipeline delay.

2.3 Residual error rate

- Set up CPM in slot 4 and JEM in slot 12, with the same CPM/JEM timings and the same replay test vectors with hit patterns which populate all 24 hit bits cyclically. Leave cable inputs connected as in section 2.2.
- Load the CMM timing values obtained in sections 2.2 and 2.3.
- Measure the residual error rate by running for 1 hour with crate and backplane inputs enabled. Confirm that the error rate is less than 1kHz (normally it should be zero over this period).

2.4 Energy Firmware Timing

- Load Energy summing firmware into both CMMs by setting the GEOADD override bits.. Add a second interconnecting rear cable.
- Repeat tests 2.1 to 2.3.

2.5 Jet Firmware Timing

- Load Jet summing firmware into both CMMs by setting the GEODD override bits. Retain the second interconnecting rear cable.
- Repeat tests 2.1 to 2.3.

2.6 Front Panel Outputs

- Remove rear interconnnect cables, then attach interconnects from the front panel outputs of the CMM under test to the upper two rear inputs of the other CMM.
- Set the geographical addresses to configure both modules for CP system summing.
- Perform a timing measurement of the cable input signal of the non-test CMM by varying the its deskew2 phase and measuring the parity error rates. Confirm that the error-free window is at least 15ns wide. Record the measurement results in the database against the module under test.
- Repeat this test for Energy and Jet firmware sets by modifying the GEOADD override register.

3 Firmware Algorithms and DAQ and RoI Readout

These tests verify that the correct algorithms are present, and are being correctly selected by the Geographical address logic.

3.1 CP readout and Algorithms

This test verifies that the entire structure of the module is operating as far as the readout is concerned. A ROD is required.

- Set up the system to run with CP firmware, with the module under test performing system-level summing. Connect the rear input from the second CMM. Set up five-slice readout, with test vectors from the JEM and CPM populating the 24 input bits cyclically.
- Load the backplane and cable timing settings obtained in section 2.
- Perform a DAQ Timing scan to set the DAQ and RoI readout pointers. Save the pointer offsets to the Database. Load the DAQ pointers to obtain the nominal DAQ and RoI readout.
- Inject L1A signals at a rate of around 1kHz. Check that the DAQ and RoI data transferred over the G-Link are correct by comparing with the online simulation.

3.2 Jet and Energy readout and Algorithms

- Set up the system in turn to run with the Energy and then with the Jet firmware.
- Connect the two rear cables.
- Perform the timing setup and readout checks as in section 3.1 for each version of the firmware.

4 Link Stability

This test verifies that the module is capable of operating at the speed extremes as far as the readout is concerned. A ROD is required.

- Set up the system to run with CP firmware, with the module under test performing system-level summing. Connect the rear input to the second CP-CMM. Set up test vectors from a JEM or CPM populating the 24 input bits of both modules cyclically.
- Load the backplane and cable timing settings obtained above
- Load the DAQ pointers to obtain the nominal DAQ and RoI readout.
- Run sequentially with 1, 2, 3, 4 and 5 timeslices at representative trigger rates of 1kHz and 100kHz, including readout at 8MHz burst rate.
- For each readout frequency, check that the DAQ and RoI G-Links remain active, and that the correct length of data is transferred with valid DAV gaps. This test is done by checking the 9U ROD readout status bits.
- Analyse a sample of data to confirm that contents still agree with simulation.
- Run the system for an hour or more to check that there are no low-rate errors.
- Repeat this test with Energy-summing and Jet-summing firmware versions.

5 CANbus Test

Using the CANbus test software on a laptop connected to the TCM, verify that CANbus messages are being sent and received correctly between TCM and CMM. Verify that the voltage and temperature values from the CMM have the correct values. Raise the board temperature by a few degrees with a hand-held heater to verify that the temperature sensors are working correctly.

6 Combined System Test

A full CP system will be assembled at RAL for CPM preproduction checks. When this system is complete, tests in sections 1-4 above should be repeated.