Project Specification

Project Name: ATLAS Calorimeter First Level Trigger-Common Merger Module

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1 Scope

The Atlas Level-1 Calorimeter Trigger consists of three subsystems:

- the Pre-processor, which accepts shaped analogue pulses from the ATLAS calorimeters, digitises and synchronises them, identifies the bunch-crossing from which each pulse originated, scales the digital values to yield transverse energy (E_T), and prepares and transmits the data to the following stages;
- the Cluster Processor (CP) subsystem, which identifies and counts isolated e/γ and τ candidates;
- the Jet/Energy Processor (JEP) subsystem, which identifies and counts energetic jets and computes the missing, total, and jet transverse energies.

The CP and JEP subsystems identify trigger features by using low-latency algorithms running in FPGAs in Cluster Processing Modules (CPMs) and Jet/Energy Modules (JEMs). Each module transmits its results over a backplane to a Common Merger Module (CMM) which merges the information for all modules in the crate. These sums are passed by cable link to a further CMM where the results from all crates are added and transmitted to the Central Trigger Processor. The architectures of the CP and JEP subsystems are designed to be sufficiently similar that a common backplane is used. This also permits the use of a common design of merger module hardware. The positions of the CMMs in the CP an JEP crates are illustrated in Figure 1

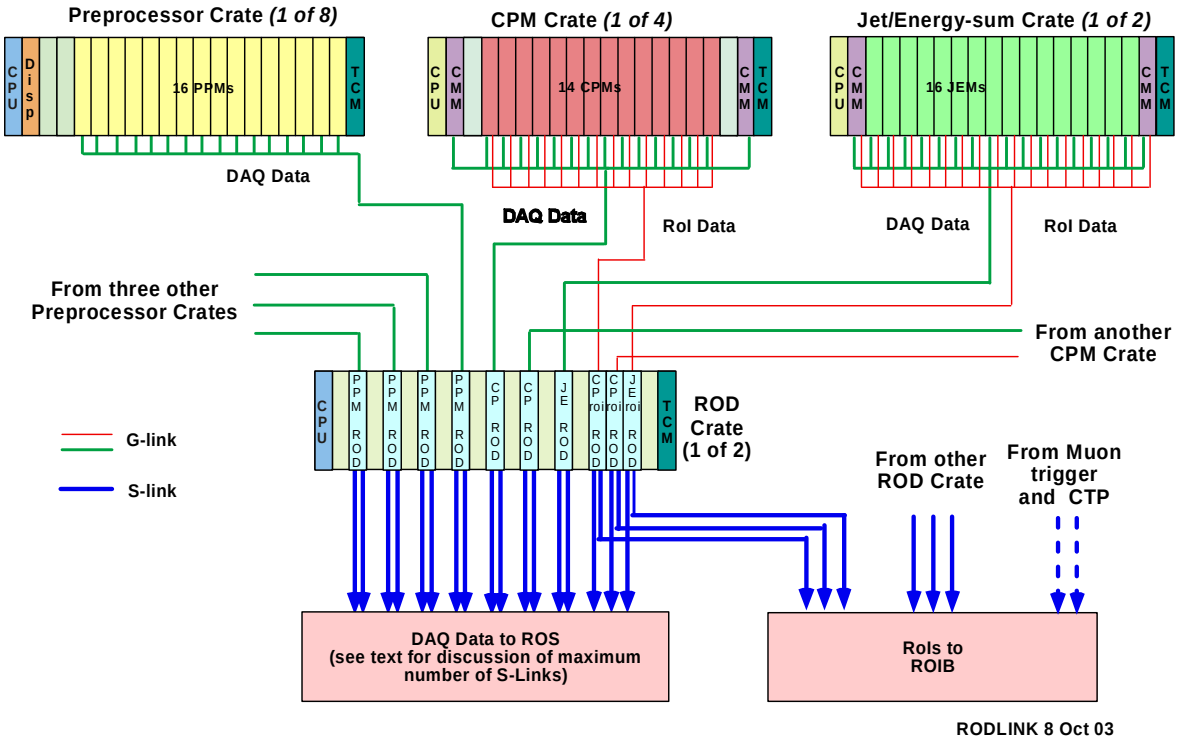

Figure 1: Overview of Calorimeter trigger crates, illustrating positions of CMMs.

The purpose of this document is to specify the Common Merger Module, leading to construction of CMM production modules. Data transfer has been demonstrated from Cluster Processor Modules and Jet/Energy Modules to the CMM prototypes, with correct merging of hit counts and energy sums. Testing includes real-time data transfer from

CMMs to the Central Trigger Processor (CTP), event data to data read-out drivers (D-RODs), and Region-of-Interest data to RoI read-out drivers (R-RODs).

2 Related projects and documents

[2.1] ATLAS TDR at http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html
[2.2] G-link documentation at http://literature.agilent.com/litweb/pdf/5966-1183E.pdf
[2.3] ROD document via http://hepwww.rl.ac.uk//Atlas-L1/Modules/Modules.html
[2.4] TTC documents at http://www.cern.ch/TTC/intro.html
[2.5] I2C Bus specification at http://www.semiconductors.philips.com/acrobat_download/literature/9398/39340011.pdf
[2.6] Latency Envelope definitions, at https://edms.cern.ch/document/107364/2
[2.7] TCM document via http://hepwww.rl.ac.uk//Atlas-L1/Modules/Modules.html
[2.8] CPM specification via http://hepwww.rl.ac.uk//Atlas-L1/Modules/Modules.html
[2.9] Reduced VME specification via http://hepwww.rl.ac.uk//Atlas-L1/TIN/TIN.htm
[2.10] JEM specification via http://hepwww.rl.ac.uk//Atlas-L1/Modules/Modules.html
[2.11] Common CP and JE Crate backplane specification via http://hepwww.rl.ac.uk//Atlas-L1/Modules/Components.html
[2.12] Central Trigger Processor documentation via http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/LEVEL1/ctpttc/L1CTP.html
[2.13] Use of TTC system and Busy network, at http://hepwww.ph.qmul.ac.uk/l1calo/doc/pdf/TTCBusy.pdf
[2.14] MB90F590 series microcontroller datasheet and reference manuals, at http://www.fme.gsdc.de/pdf/ds90590-ds07-13704-5e.pdf and http://www.fme.gsdc.de/pdf/hm90590-cm44-10105-4e.pdf

3 Technical Aspects

The module is 9U to meet the IEEE1101.10 standard crate specification, and incorporates a plug-in TTCrx daughter module.

Five prototype modules have been built to demonstrate correct data summing and read-out, and have been used for the combined system tests. When production modules are manufactured, 21 are needed (8 for the CP system, 4 for the JEP system, 5 for test systems plus 4 spares).

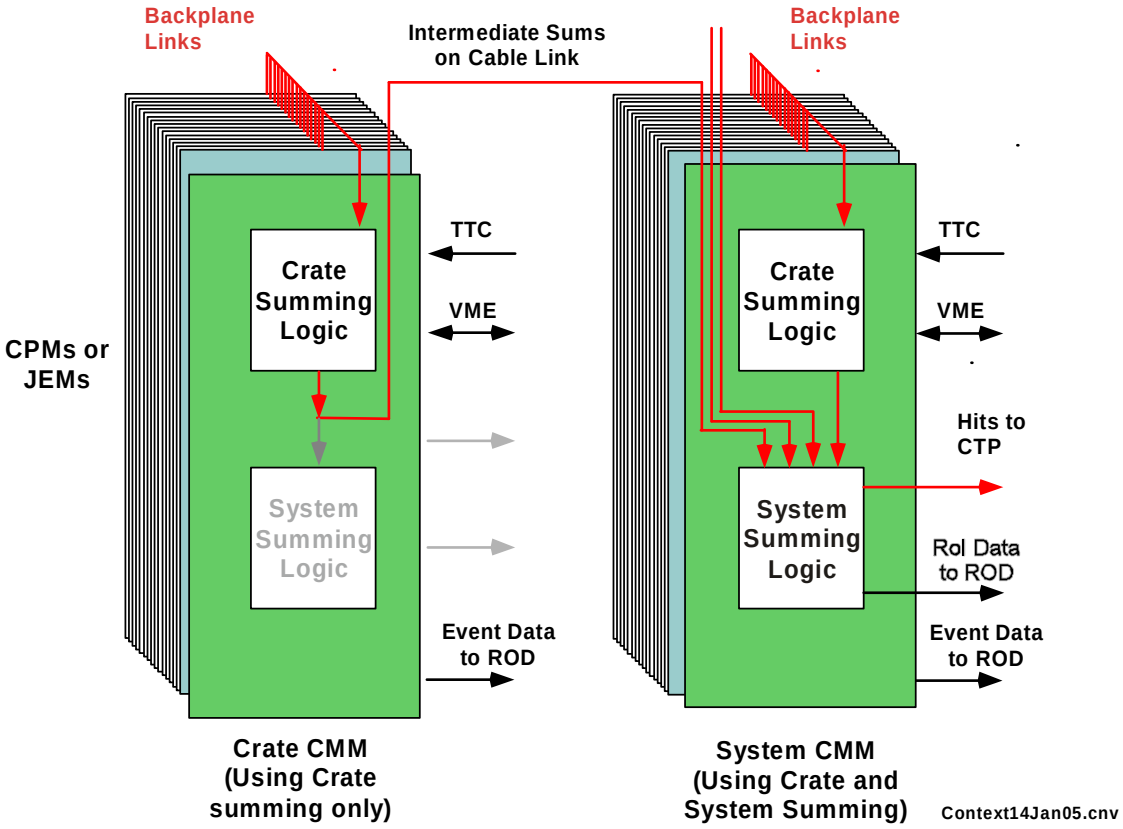

Figure 2: Context diagram of CMM showing backplane, TCM, CPMs or JEMs, CTP

3.1 Requirements and Specifications

The CP has 16 threshold sets (i.e. combinations of cluster and isolation thresholds), eight reserved for electron/photon triggers and eight programmable to function either as e/γ or as τ/hadron triggers. For each threshold set, the 'hits' above threshold must be summed to a maximum of seven over the entire detector. One CMM per crate handles the first eight threshold sets, and a second CMM per crate handles the other eight. Two CMMs act as "System CMMs", one each for e/γ and τ hits. These modules form their own intermediate sums as above, add the intermediate sums received from other modules by cable link, and send the results to the Central Trigger Processor.

Similarly, in the JEP there are eight jet threshold sets, each of which can have a programmable jet-window size. For each threshold set, the 'hits' must be summed to a maximum of seven over the entire detector excluding the forward calorimeters (although a programmable option to include the forward calorimeters in the overall jet trigger might be desirable.) This jet hit summing is done by one CMM per JEP crate. A more limited

counting capability is required for jet-like hits in the forward calorimeters, and this is done in the same CMM.

A second CMM in JEP crates sums the two components of transverse energy as well as the total transverse energy. The final sums of transverse energy in the entire detector, including forward calorimetry, must be compared to eight missing transverse-energy thresholds and four total transverse-energy thresholds.

Two of the CMMs again act as "System CMMs", one each for jet hits and energy summing. These modules first form their own intermediate sums as above, then add these to the intermediate sums received from other modules by cable link, and send the results to the Central Trigger Processor. Extra logic in the jet system CMM calculates the total jet transverse energy (E_{TJ}). An energy 'RoI' is generated and sent to the Level-2 RoI Builder via the RoI Readout Driver (R-ROD).

A common hardware CMM design is used to perform all these functions, with different FPGA logic as required. Each hardware module includes all the logic to perform both crate and system-level processing, as shown in figure 2 below.

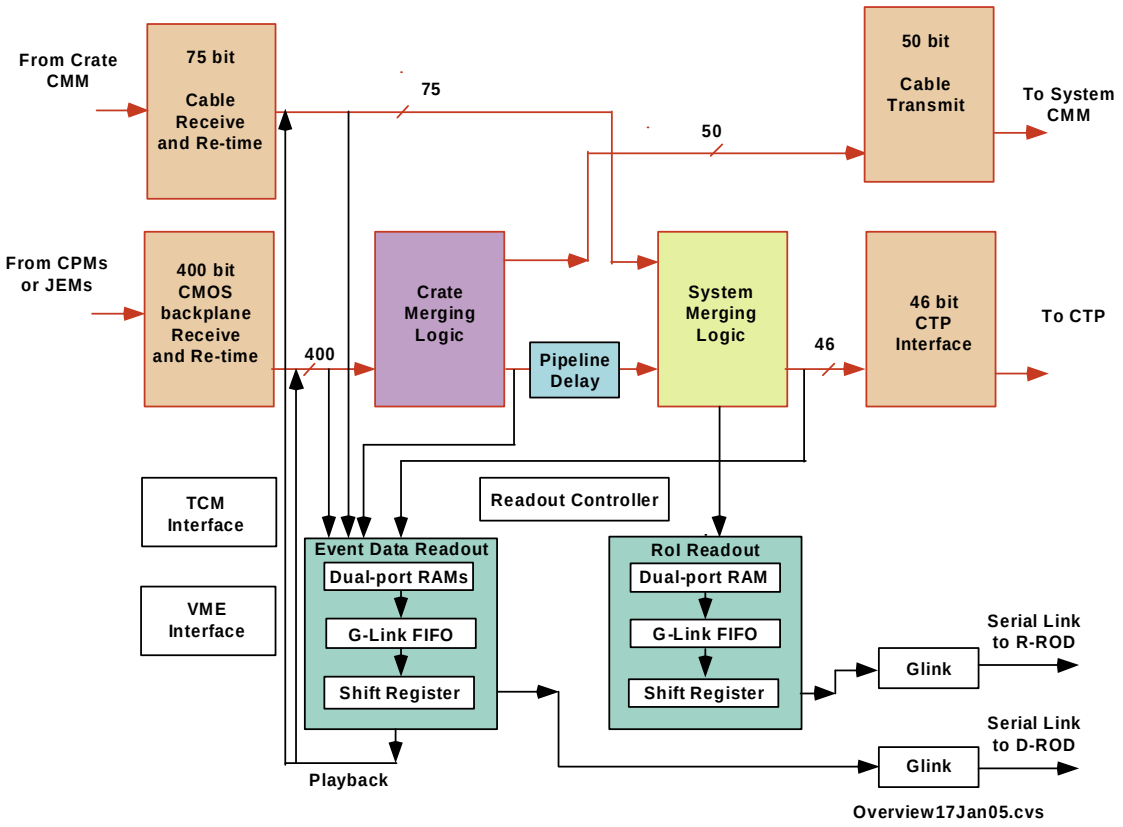

Figure 3: Overview of Common Merger Module

3.2 Functional Requirements

3.2.1 CPM hit counting:

Crate summation (Figure 4)

(a) Receive 350 backplane signals at 40 MHz, composed of eight 3-bit hit counts plus 1 parity bit from each of 14 CPMs.
(b) Form eight separate 3-bit sums, one for each threshold.
(c) Transmit 25 bits of summed data, composed of eight 3-bit hit counts plus 1 parity bit, on 40 MHz cable links to the System CMM
(d) Receive TTC signals from the TCM and derive LHC clock, broadcast commands, and L1 Accept.
(e) On receipt of L1A, collect a programmable number (up to 5) of time-slices of input and output data and transmit to a D-ROD via G-Link

System summation (Figure 5)

(f) Receive 75 bits of summed data from three Crate CMMs at 40 MHz on cable links
(g) Check the received parity.
(h) Receive 24 bits from local crate summation logic, delayed to match cable data timing.
(i) Form eight final three-bit sums
(j) Transmit 24-bit final sums with parity to CTP over cable links
(k) On receipt of L1A, collect a programmable number (up to 5) of time-slices system summation results and transmit to a D-ROD via G-Link

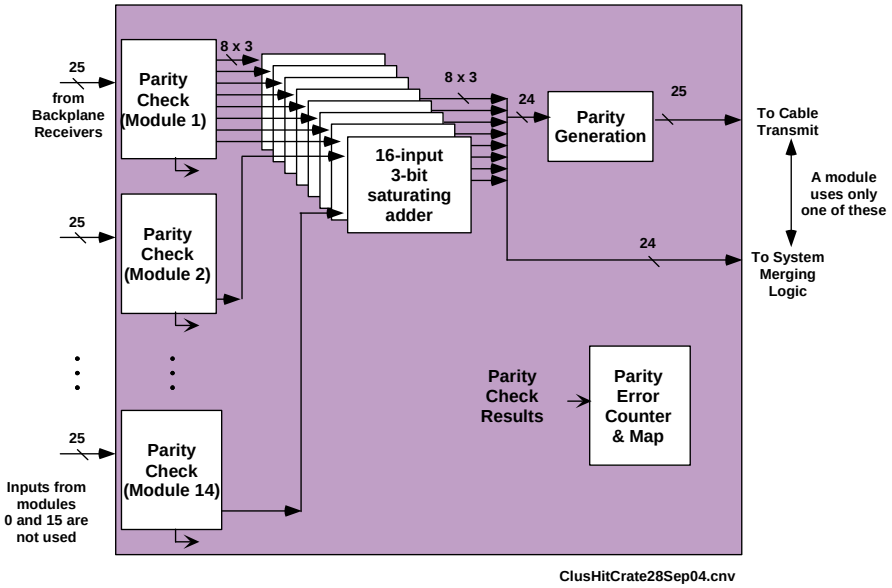

Figure 4: Cluster summation at Crate Level

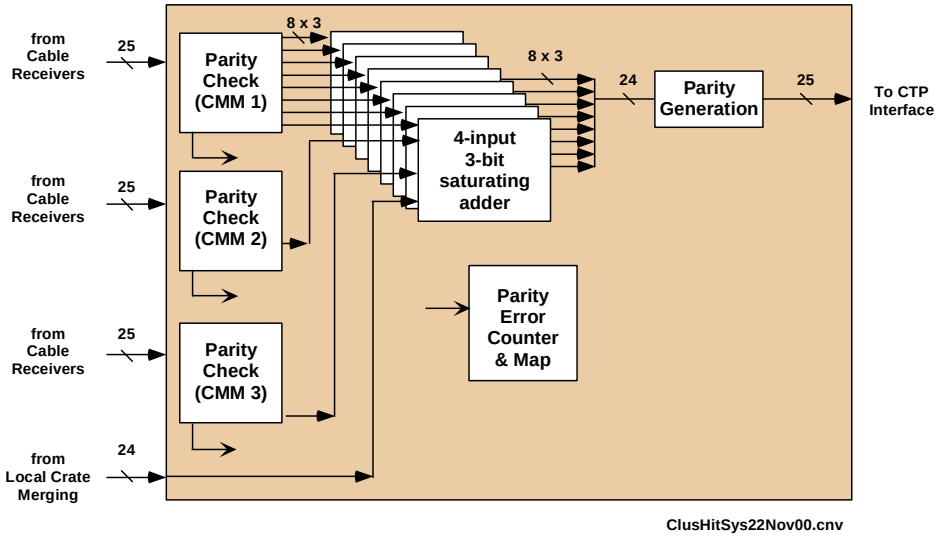

Figure 5: Cluster summation at System Level

3.2.2 JEM hit counting and jet energy estimation:

Crate summation (Figure 6)

(a) Receive 400 backplane signals at 40 MHz, composed of eight 3-bit hit counts plus 1 parity bit from each of 16 JEMs.
(b) Form eight separate 3-bit sums, one for each of eight thresholds in the main jet trigger (normally covering $|\eta| \leq 3.2$, i.e. barrel and end-cap calorimeters)
(c) Transmit 25 bits of summed data, composed of eight 3-bit hit counts plus 1 parity bit, on 40 MHz cable links to the System CMM
(d) Form eight separate 2-bit sums, one for each of four thresholds in forward and backward regions.
(e) Transmit 17 bits of forward summed data, composed of eight 2-bit hit counts plus 1 parity bit, on 40 MHz cable links to the System CMM
(f) Receive TTC signals from the TCM and derive LHC clock, broadcast commands, and L1 Accept.
(g) On receipt of L1A, collect a programmable number (up to 5) of time-slices of input and output data and transmit to a D-ROD via G-Link

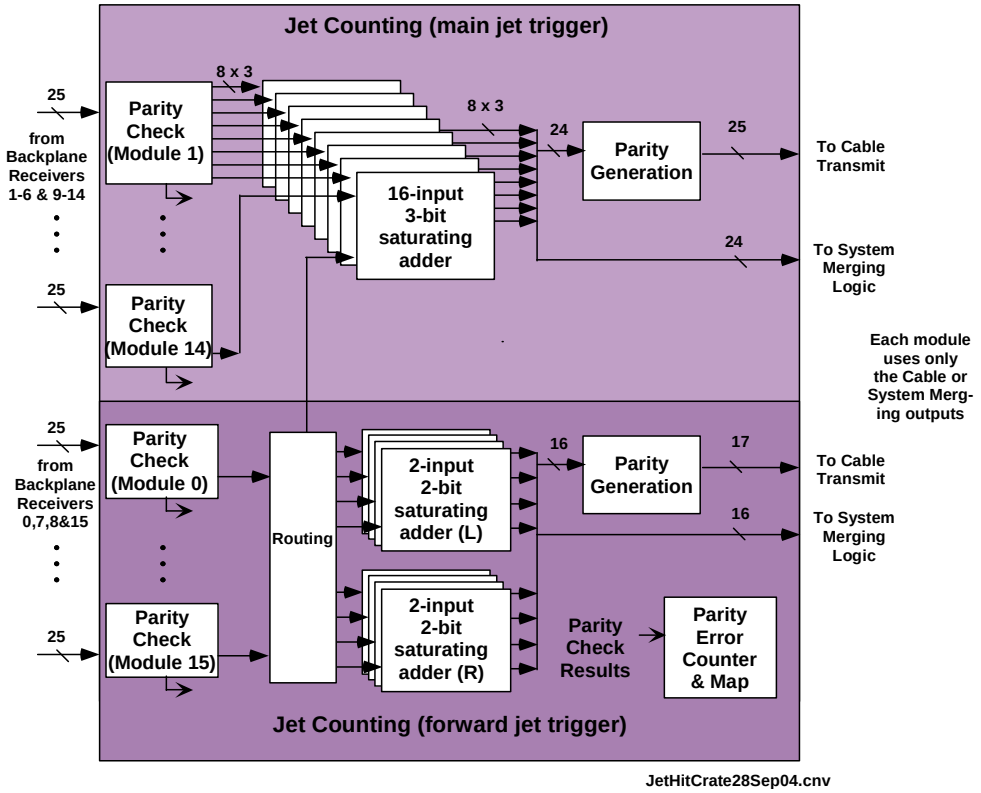

Figure 6: Jet Hit summation at Crate level

System summation (Figure 7)

(h) Receive 42 bits of summed data from a Crate CMM at 40 MHz on cable links.
(i) Check the received parity
(l) Receive 40 bits from local crate summation logic, delayed to match cable data timing.
(j) Form eight final three-bit main jet sums and eight final two-bit forward sums.
(k) Form jet E_T estimator (E_{TJ}), sum and threshold to 4-bit E_{TJ} hits.
(l) Transmit final sums and E_{TJ} hits with parity to CTP over cable links
(m) On receipt of L1A, collect a programmable number (up to 5) of time-slices of system summation results and transmit to a D-ROD via G-Link

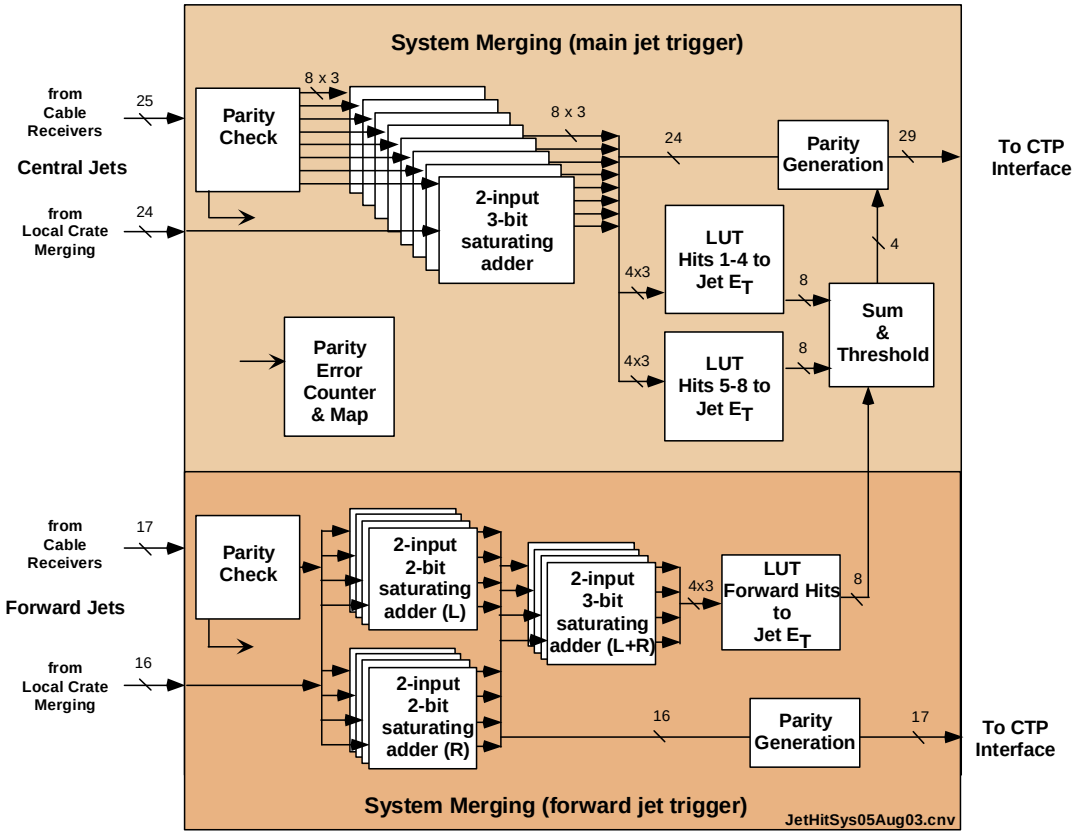

Figure 7: Jet Hit summation at System level

3.2.3 JEM Energy summing:

Crate summation (Figure 8)

(a) Receive 400 backplane signals at 40 MHz, composed of 8-bit compressed-scale E_X E_Y and E_T values plus 1 parity bit from each of 16 JEMs.
(b) Add the three energy components separately, as 15 bit twos-complement sums for the energy components E_X and E_Y, and as a14 bit unsigned sum for E_T, in each case with separate overflow bits.
(c) Transmit 50 bits of summed data, composed of two 15-bit and one 14-bit numbers, 3 overflow bits and 3 parity bits on a 40 MHz cable link to a System CMM.
(d) Receive TTC signals from the TCM and derive LHC clock, broadcast commands, and L1 Accept.
(e) On receipt of L1A, collect a programmable number (up to 5) of time-slices of input and output data and transmit to D-ROD via G-Link.

System summation (Figure 9)

(f) Receive 50 bits of summed data from a Crate CMM at 40 MHz on cable links.
(g) Check received parity
(h) Add the external and internal E_T energy components to produce the total transverse energy, and apply the E_T thresholds to form the sum-E_T hits.
(i) Vector sum the signed external and internal E_X and E_Y energy components to produce the total missing energy, and apply the missing-E_T thresholds to form the missing-E_T hits.
(j) Transmit sum-E_T and missing-E_T hits with parity to the CTP over cable links.

(k) On receipt of L1A, collect a programmable number (up to 5) of time-slices of system energy summation results and transmit to a D-ROD via G-Link, and collect Energy RoI data and transmit to R-ROD.

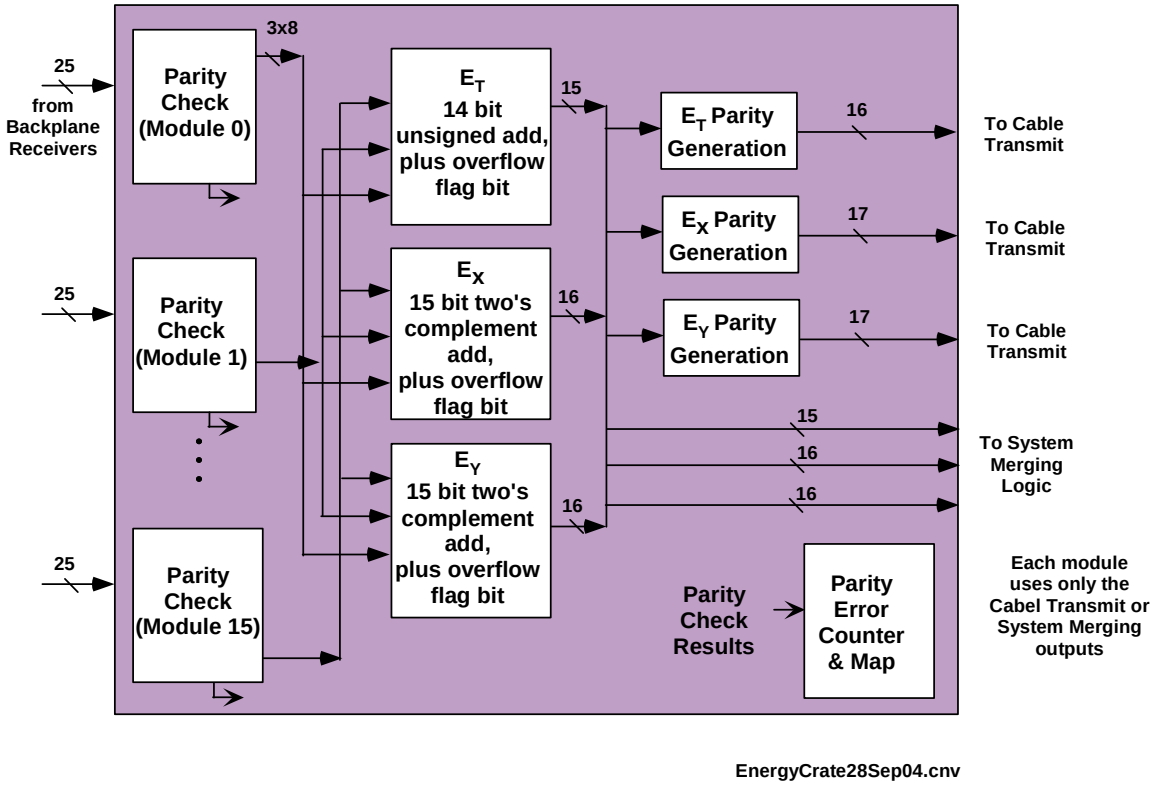

Figure 8: Energy summation at Crate Level

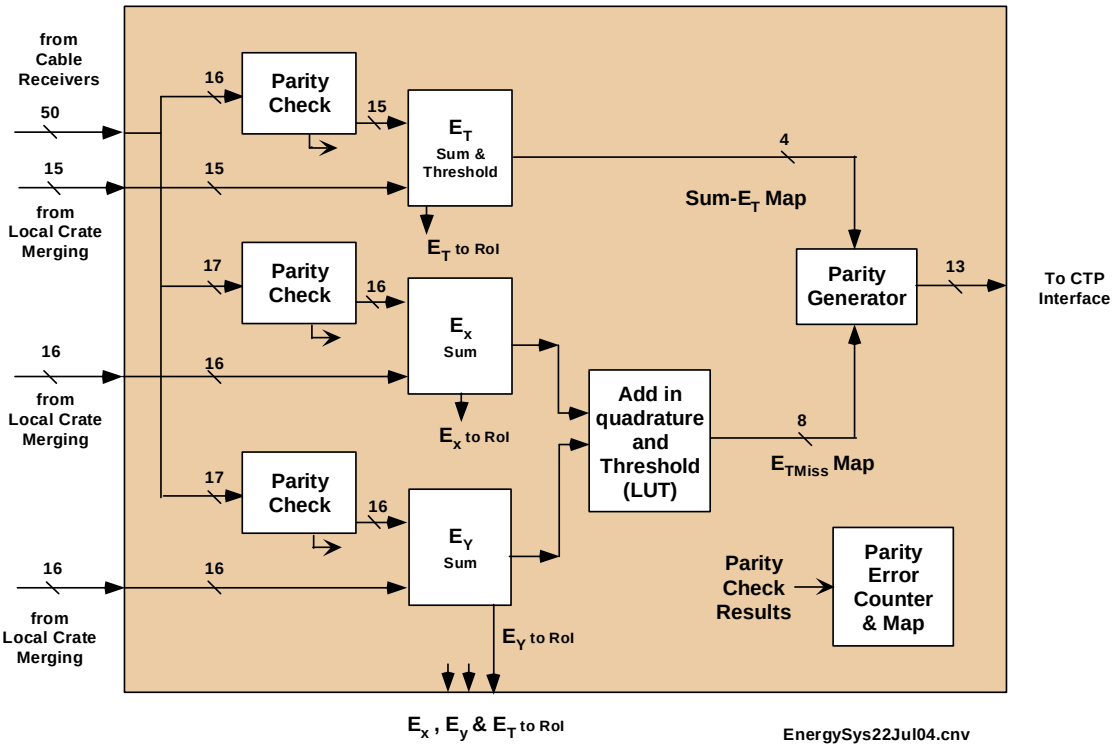

Figure 9: Energy summation at System Level

3.3 Error Rate Requirements

Internal trigger errors must generate less than 1% of the maximum ATLAS level-1 trigger rate. With the exception of energy data from the JEMs, the majority of the 400 input data bits to each CMM from JEMs or CPMs are zero, and a change in any one of these bits might generate a trigger. In the case of Energy data, the encoding scheme handles small energies and some data bits may often be non-zero. The most demanding assumption is again that any change to data bits may generate a trigger.

The upper limit to the acceptable backplane input bit error rate is given by requiring that the twelve CMMs together receive no more than 1 kHz of modified bits over the 40 MHz backplane:

$$BER \times 12 \times 400 \times 40 \times 10^{6} < 10^{3} \Rightarrow BER < 5 \times 10^{-9}$$

It is straightforward to verify that this is met by counting the rate of observed parity errors on the backplane. Observing no errors from one module for one second already surpasses the requirement by a factor 100.

The module should also minimise the effect of any errors that do occur by setting the corresponding input data to zero.

3.4 Latency Requirements

The overall latency for the level-1 trigger should not exceed 2.0 μs. Detectors are required to accept up to 2.5 μs, thus providing some tolerance if performance targets cannot be met. The overall latency envelopes for the trigger system are defined in [2.6], summing to 2.054 μs but not yet including the chain of LTP modules. In the test beam, the measured overall latency leads to the almost identical value of 82 bunch crossing times.

The latency of merger modules is not identified separately, but should be kept in the region of 5 or 6 bunch crossings if the envelope is to be maintained as measured in the test beam.

3.5 Functional Details

3.5.1 Nomenclature

All merger modules are physically identical, and capable of performing crate and system-level summation for the cluster, jet or energy subsystems. The inter-crate cabling, however, defines four CMMs in which system-level summation is performed as well as crate-level summation, the necessary signals being carried by cable links from other CMMs in which only crate-level summation is actually needed. The term "System CMM" is used to identify those CMMs performing the final stage of summation prior to sending results to the CTP. The term "Crate CMM" is used to identify CMMs providing only crate-level summation.

3.5.2 Backplane and cable interfaces

New data are received from the backplane and (on System CMMs) from the cable link(s) on each 40 MHz clock cycle. The backplane data from each source module (JEM or CPM) are transmitted using single-ended back-terminated 2.5V CMOS levels. The signals consist of 24 data bits plus one parity bit. Data from Crate-CMMs are sent to System-CMMs by balanced cable using differential LVDS levels. The timing skew between the

earliest and latest data bits arriving from any one CPM, JEM, or remote CMM must not exceed 10 ns. Odd parity is used with both backplane and cable data, so that all-zero data are accompanied by a nonzero parity bit. On each cycle, the data are clocked onto the module using one of four 160 MHz clock phases, which can be chosen separately for each originating CPM, JEM or remote CMM. The parity is recalculated and compared with the received parity. If there is a parity mismatch, the received data for the clock cycle in question are set to zero, the parity-error counters are incremented, and the parity error indicator forwarded to the following logic, from where it will eventually enter the DAQ readout.

3.5.3 Module Timing considerations

The module timing is derived from the TTC signals distributed on the backplane by the Timing Control Module [2.7]. The backplane input synchronisation logic and crate-summing FPGA timing is derived from the TTC CLOCK40Des1 phase-adjustable clock. The system-summing FPGA must accept incoming remote sub-sums, and it and the cable input synchronising logic use the TTC CLOCK40Des2 phase-adjustable clock. The pipeline delay element between these two logic blocks compensates for the cable delay from the Crate CMM. Compensation for cable lengths of up to 5 metres (25 ns propagation time) may be needed, so the delay should be adjustable up to 50 ns. If shorter cabling is possible, it should be possible to reduce this pipeline delay to zero. The delay is implemented within the system-summing FPGA.

Timing calibration of backplane and cable inputs are performed under software control using test data supplied by CPMs and JEMs.

The overall latency of the module from receipt of backplane signals to transmission of hits to the CTP must be as low as possible, and must fall within the latency envelope for the trigger.

3.5.4 Cluster Hit Counting

The received data consist of eight 3-bit hit counts per CPM, formatted as in Figure 10. The CMM adds the 3-bit hit-counts separately for each threshold, with any overflow setting the output hit count to 7. This process forms the eight 3-bit sums constituting the intermediate sum data. In Crate-CMMs, an odd parity bit is generated and sent with the intermediate sums over cable link via the rear transition module (see Appendix C).

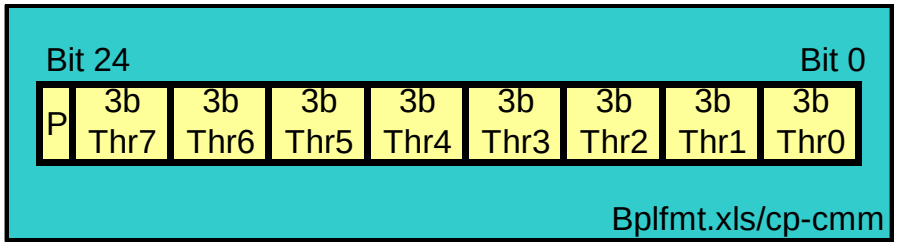

Figure 10: Format of Backplane CPM - CMM data

System CMMs receive intermediate sums by cable link from other crates, formatted as in Figure 11. These are added to the on-board intermediate sum data from their own crate to form eight final 3-bit sums, again with overflow setting the output value to 7. These data are sent over parallel links to the CTP, as in Figure 12.

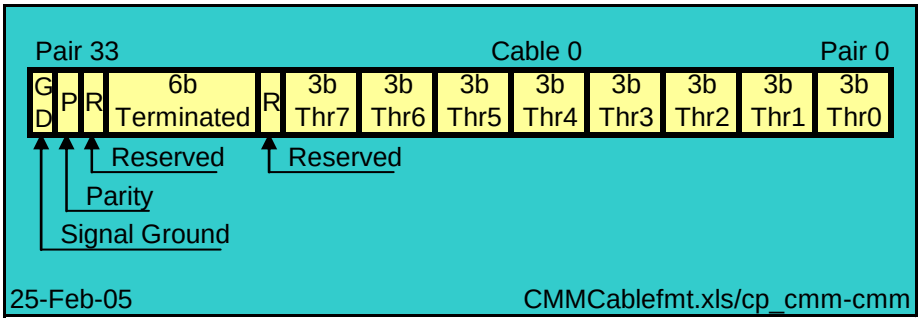

Figure 11: Format of cable input data from remote cluster CMM.

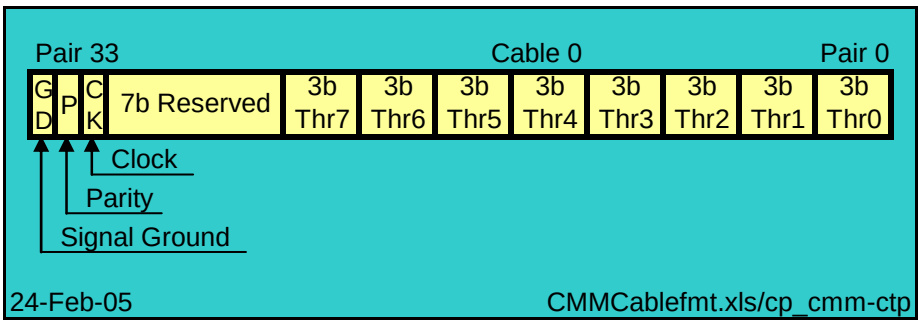

Figure 12: Format of cable data from cluster CMM to CTP

3.5.5 Jet Hit Counting

The jet counting process is similar to the cluster counting process, but with the added requirement to count forward jets and to estimate the total jet transverse energy. This requires different processing of data from JEMs 0, 7, 8 and 15, which handle forward calorimetry, and extra processing on the system-summing CMM.

For barrel and end-cap JEMs 1-6 and 9-14, the received data consist of eight 3-bit main jet hit counts per JEM, as shown in the upper half of Figure 13 (formatted like the CPM data). For end-cap and forward JEMs 0, 7, 8 and 15, the received data consist of some bits carrying main jet hit counts for the same eight thresholds, and the remaining bits carrying hit counts for four separate forward calorimeter thresholds, as shown in the lower half of the figure. In the present design, the 24 bits are composed of 8*2 bits for main jet thresholds, plus 4*2 bits for forward thresholds. Although the use of the bits is defined, it is a requirement that the JEM and CMM FPGA configuration be structured such that they can readily be modified (i.e. the FPGAs reprogrammed) to work with different mixtures of bits depending on the physics requirements. The routing block in Figure 6 illustrates the region of CMM code which would require adaptation to carry different mixtures of input signals to the appropriate processing elements.

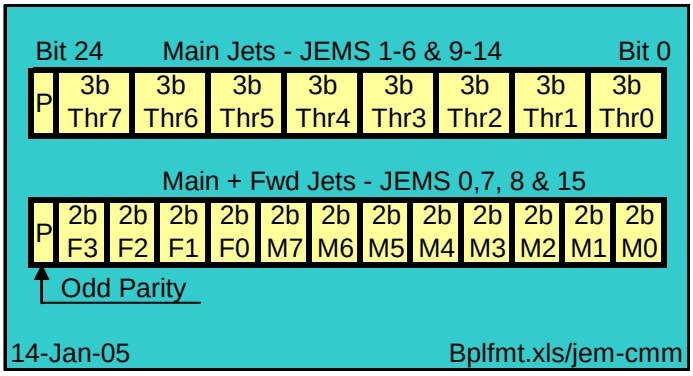

Figure 13: Format of Backplane JEM - CMM jet data.

The hit-counts are added separately for each of the eight thresholds of the main jet trigger. This sum includes the main jet hit counts from all JEMs. An arithmetic overflow should set the corresponding resulting hit sum to 7. The hit-counts for the forward jet trigger from JEMs 0+8 and 7+15 are added separately for each threshold, with any overflow setting the resulting hit sum to 3. This process forms the eight 3-bit sums for the main jet trigger and eight 2-bit forward sums which together constitute the intermediate sum data.

In the crate CMM, an odd parity bit is generated and sent with the intermediate sums over cable link.

The system CMM receives intermediate sums by cable link, formatted as in Figure 14. These are added to the on-board intermediate sum data from its own crate to form eight 3-bit overall jet-trigger sums and eight 2-bit forward jet-trigger sums, with overflow setting the scale maximum as above. These data are sent over parallel links to the CTP.

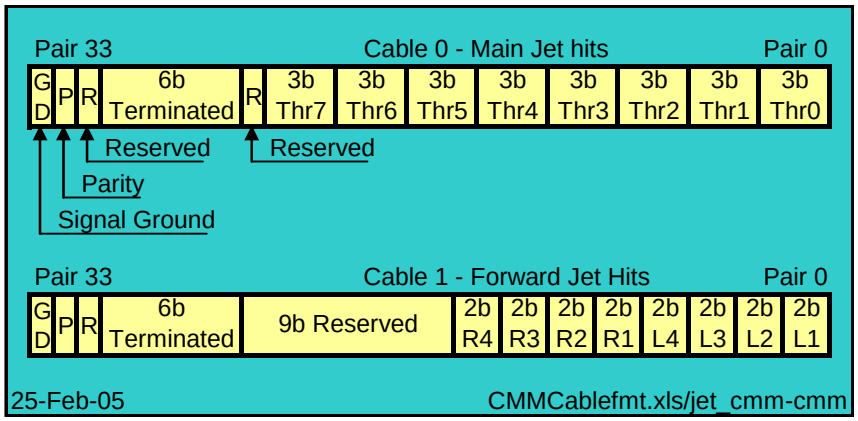

Figure 14: Format of cable input data from remote Jet CMM

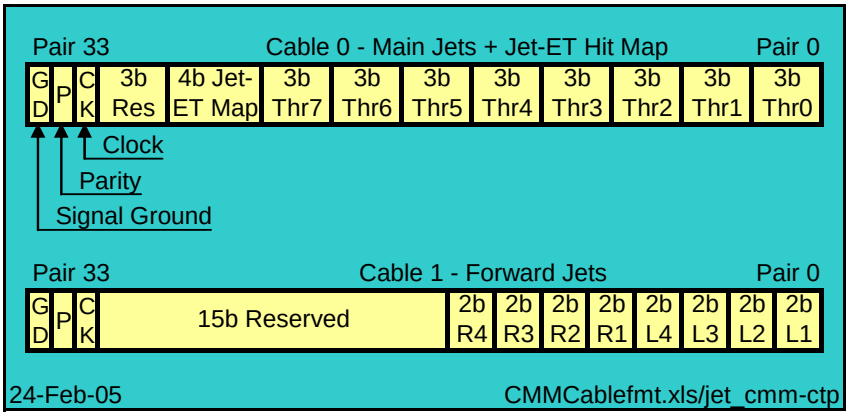

Figure 15: Format of cable data from Jet CMM to CTP

3.5.6 Jet Transverse Energy Estimation

The total jet transverse energy is calculated using a simple multiplicity-based estimator. The inputs to the algorithm are the numbers of jets passing each of the main and forward jet thresholds, and the values of those thresholds. As the counts are rounded down to 7 (3 for forward jets), and the maximum incoming calorimeter information is limited to 255 GeV per tower, the estimator may be low for events with high jet multiplicity or high jet energies.

To understand the estimator, consider an event containing n jets passing the threshold E_T > x GeV and m jets passing E_T > y GeV, with n > m and y > x. There are n – m jets in the E_T range x GeV ≤ E_T ≤ y GeV. These jets have a total E_T of at least (n – m)x GeV and at most (n – m)y GeV. A number of possible estimators of the total jet E_T can be constructed in this way, such as lower limits on jet E_T (assuming each jet lies exactly at the lower end of the range, upper limits, or indeed both together.

The hardware implementation of the E_{TJ} calculation uses lookup tables to convert groups of jet counts to transverse energies. The energies are summed and thresholds applied to yield the four-bit E_{TJ} hit map.

3.5.7 Energy Summing

3.5.7.1 Compressed Energy Scale

A compressed energy scale is used for energy transmission from JEM to CMM. The baseline format consists of a 2-bit scale and a 6-bit magnitude, as shown in Figure 16. The conversion in the JEMs from a linear scale to the compressed scale is made in a LUT, and other transfer functions could be used. This can be accommodated in the CMM if the reverse transformation is applied to the incoming data on receipt.

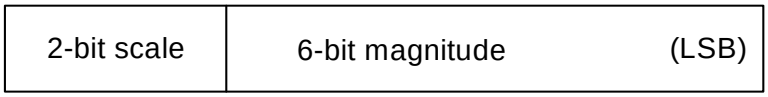

Figure 16: Quad-Linear energy scale

The magnitude value must be multiplied by a scale factor to obtain the energy value, as indicated in the following table:

Scale bits	Scale Factor	Full Scale
00	1	63
01	4	252
10	16	1008
11	64	4032

3.5.7.2 The Energy-Summing process

On each 40 MHz clock cycle, quad-linear unsigned E_X, E_Y and E_T energy data are presented over the backplane from each JEM. The data are clocked onto the CMM using one of four 40 MHz clock phases. Parity (odd) is checked. The trigger phi-quad architecture puts module boundaries on a detector x-z or y-z plane, so all modules in the same quadrant share the same E_X and E_Y sign, as shown in Figure 17.

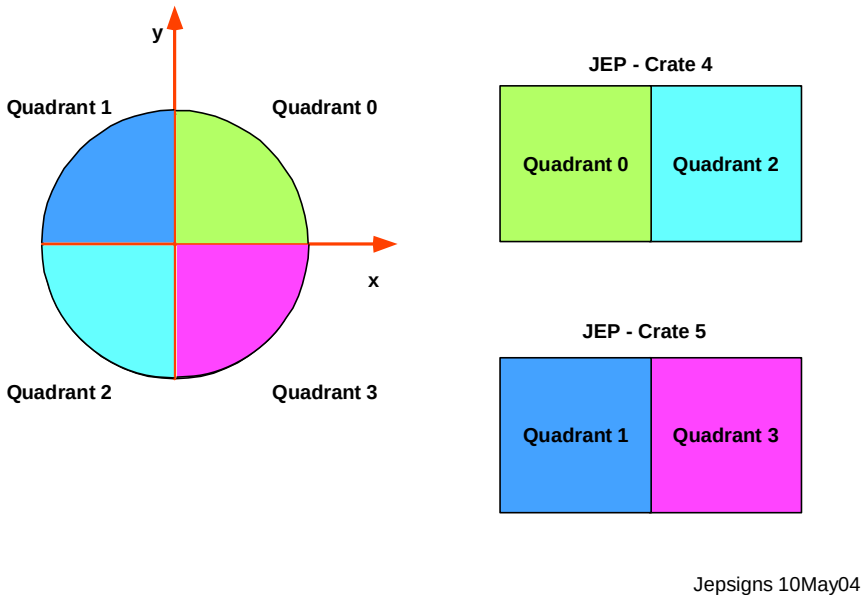

Figure 17: Quadrant organisation in the JEP

Unsigned arithmetic is used to add the 8 inputs from each half crate. The diagonally opposing half crate sums are added to produce the 14-bit unsigned E_T (up to 16383 GeV), and subtracted to produce 15-bit twos-complement signed intermediate sums (± 16383). Identical arithmetic is used in crate-level summation in both crates, so the calculations done are:

$$Crate4: E_X(4) = E_X(0) - E_X(2), \quad E_Y(4) = E_Y(0) - E_Y(2), \quad E_T(4) = E_T(0) + E_T(2)$$
$$Crate5: E_X(5) = E_X(1) - E_X(3), \quad E_Y(5) = E_Y(1) - E_Y(3), \quad E_T(5) = E_T(1) + E_T(3)$$

The subtraction is done using twos-complement arithmetic. The results are in the local coordinates of quadrant 0 (x, y positive) and quadrant 1 (x negative, y positive) respectively, so the system totals are calculated thus:

$$System: E_X = E_X(4) - E_X(5), \qquad E_Y = E_Y(4) + E_Y(5), \qquad E_T = E_T(4) + E_T(5)$$

Each JEM can encode up to 4032 GeV in its 8-bit output fields. Overflow bits O_X, O_Y and O_T for are set in the crate-summing logic if any JEM input is saturated or if an E_X, E_Y or E_T sum exceeds the 14-bit magnitude. No further overflows occur in system-summing logic, but any crate-summing overflows are propagated in into the system DAQ and RoI

output. In the interests of minimum latency, the overflows are indicated by separate overflow bits in the E_X, E_Y and E_T data, while the data summing process goes on in parallel using whatever input data is presented. When one of the overflow bits is set, the sign of the corresponding summed data is correct, but the magnitude will not be saturated and should be ignored except for module checking purposes.

In Crate-CMMs, an odd parity bit is generated and sent with the three intermediate sums over cable link in the format shown in Figure 18, with the E_X and E_Y values are transmitted in twos-complement format, while the E_T value is an unsigned positive integer.

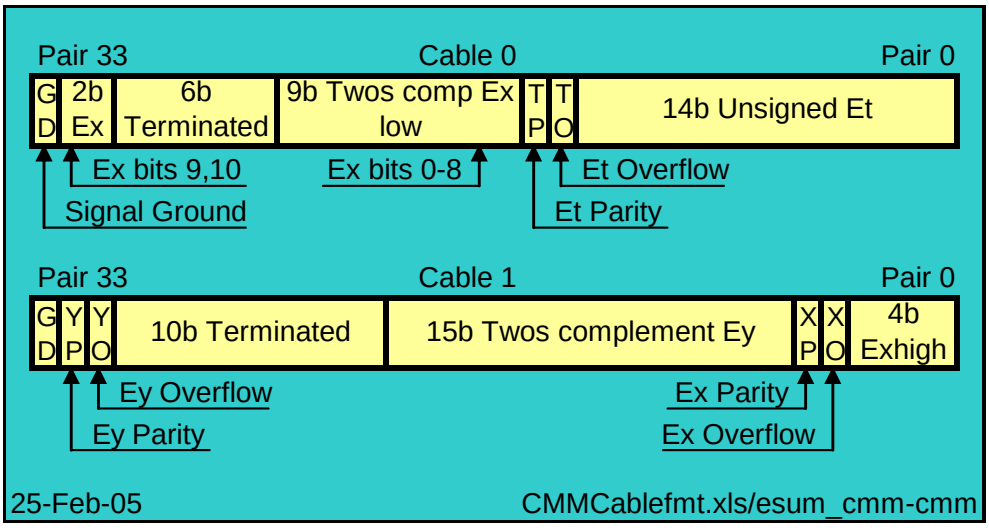

Figure 18: Format of cable input data from remote Energy CMM.

System-CMMs receive these data from a remote CMM. The incoming data are re-timed, the parity (odd) is checked, and the sums are added to the on-board intermediate sum data to produce twos-complement E_X, E_Y and unsigned E_T. The most significant bits are kept to provide the sign bits required for RoI readout, but are not needed with the final E_X and E_Y as the following algorithm needs only the magnitude to calculate $\sqrt{\left(E_X^2 + E_Y^2\right)}$. The E_T value is compared in a lookup table to the four thresholds to give the final E_T hit map, with threshold values of up to 2047 GeV in 4 GeV steps.

3.5.7.3 Computation of Missing- E_T hits

The summed E_X and E_Y values are calculated as 11-bit values. As illustrated in Figure 20, a common range is chosen for E_X and E_Y depending on the highest set bit in the two values. Six-bit truncated values are also chosen, depending on the range. These E_X and E_Y values together form a 12-bit address (4096 locations) which is used to access a lookup table. Each LUT location contains a 32-bit value made up from four 8-bit fields. One of these 8-bit fields is chosen, corresponding to the energy range. The lookup table content is pre-loaded to give the same result as squaring the incoming E_X and E_Y, adding the squares, and comparing to eight squared thresholds to give the map of E_{TMiss} thresholds passed. As illustrated, the precision of the thresholding diminishes with increasing range. The Sum-E_T and Missing-E_T data are sent to the CTP, formatted as shown in Figure 21. In both cases, the data are sent as a hit map.

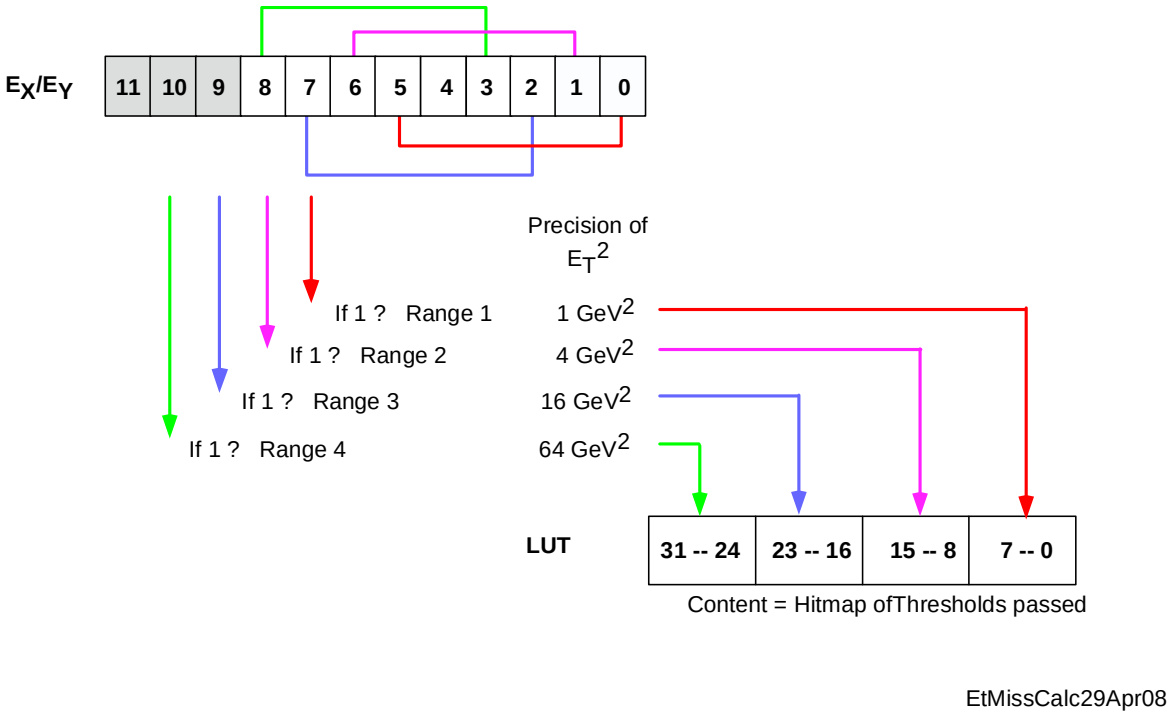

Figure 19

Figure 20: Implementation of E_{TMiss} threshold calculation.

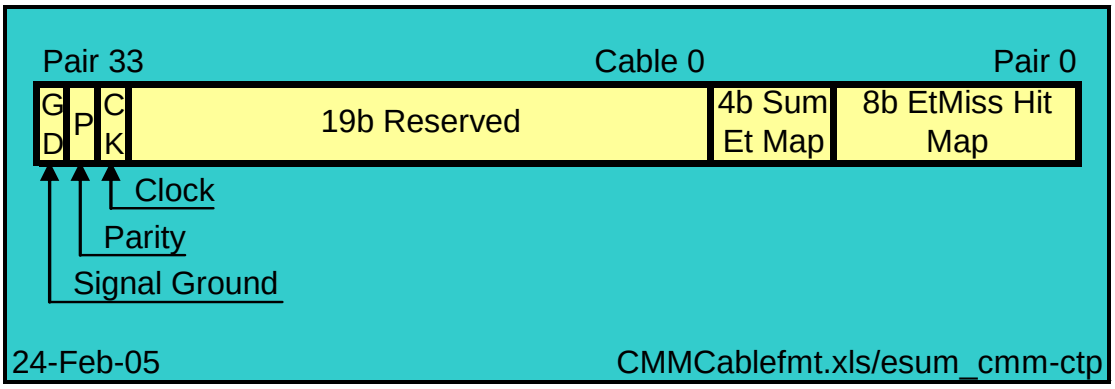

Figure 21: Format of cable data from Energy-summing CMM to CTP

3.5.8 Input Signal control

Backplane signals from individual CPM or JEM modules may be disabled using a mask register. When a bit is set, all data from the corresponding module are ignored, the parity check is not performed, and data entering the algorithm (hits or energies) are set to zero. A similar control allows incoming cable link data to be disabled.

3.5.9 Playback Capability

A facility is included in the readout logic to play back data from the scrolling memory into the real-time data path (refer to Figure 3). To operate in this mode, the playback mode bit is set in the control register, and the dual-port RAM is pre-loaded by computer with the desired data values. In playback mode, data arriving from CPMs or JEMs is ignored, and

data is taken instead from the dual-port RAM. All other functions of the module operate as normal. In particular, by appropriate adjustment of the readout offset, the event data readout can contain a copy of the data injected into the real-time path.

The sequencing of the input controls for backplane inputs is as follows:

1. Incoming data is received. In playback mode, the playback data is introduced;
2. The channel disable mask is applied;
3. If not in replay mode, data is copied to the readout/playback memory. In replay mode, the data is not re-recorded.
4. Parity checking is applied.
5. Resulting data enters the algorithm

The same ordering (but without the replay option) applies to cable inputs from remote crate-summing modules.

3.5.10 TTC Data Synchronisation

If data is being played back from multiple CMMs, their scrolling memories must be synchronised after loading. This is achieved using the TTC command word "01mmmmxx" (see [2.13]), which resets the scrolling memory write pointers to zero and the read pointers to their offset values. Bits "mmmm" and "xx" may take any value during this command. As the values for TTC commands may change, all TTC command outputs are routed to a programmable device from which the synchronisation signal is derived.

3.5.11 Error Handling

All input data, both from the backplane and (on the System-CMMs) over cable links, are accompanied by an odd parity bit, generated at the rate of 1 bit per source module. After re-timing, the incoming data parity is checked. If a parity error is detected, the following actions are performed:

1. A bit in the parity error latch for the corresponding channel is set to 1. This identifies which input is giving errors. A VME command is required to clear the register.
2. The parity error counter (PEC) register is incremented for any clock cycle where there is at least 1 parity error. This estimates the error rate.
3. The PE bit is set in the module status register whenever the PEC register is nonzero.
4. The parity check result (PCR) for this clock cycle is formed from the 'OR' of all parity checks for the current bunch crossing.
5. The PEC and PCR bits are included in the DAQ and RoI data. The module does not generate any other external error signal, so data monitoring or regular hardware scanning must detect an error condition.

A single VME command is provided to clear all parity error registers on the module.

3.5.12 Rate Metering

The CMM measures the rate of trigger hits as they arrive from the CPMs and JEMs and during the hit summing process. The rate meter function has components at Module, Crate, and System level.

The Module and Crate rate meters count a selectable OR of hits for all the thresholds coming from each individual module or crate. The System rate meters count hits for each threshold separately over the whole system.

A rate normalisation counter counts 40.08MHz clock cycles, providing a reference value for the other counters.

All CMM firmware versions include the same group of registers at the same addresses. Some of the registers and some of the bits are not used in some firmware versions, and return zero on VME read. Unused VME-read-write registers and bits accept VME write cycles but ignore written data. It is expected that the counters will be read often enough to avoid overflow, but counters should saturate at 0xFFFFFFFF so that overflow can be detected. All counters are read-only from VME.

In normal use, software will cycle round all CMMs roughly once every 5 seconds. Software should first inhibit counting by setting the Rate Counter Inhibit bit in the Control Mode Register, and then read all counters. Counters should then be cleared using the Reset Rate Counters bit in the Control Pulse Register, and then the counting inhibit removed. This guarantees that all the counters in a CMM are live for the same period. The software must normalise readings CMM-by-CMM by dividing by the Rate Normalisation Counter for the CMM concerned, or reject the reading if any of the counters has saturated.

3.5.12.1 CP Subsystem Rate Metering

This uses only Module Hit Counters 1-14 and not 0 and 15. Only the bottom eight bits of the Rate Masks are used. Only System Hit Counters 0-7 are used.

Starting from the parity-checked CMM input from each CPM, the eight 3-bit hit counts are ORed to produce eight 1-bit signals, one for each electron or tau threshold. Bits for a particular hit threshold are set to zero if disabled in the Module Rate Mask register. The resulting 8 bits are ORed to produce a single signal for the CPM concerned. This is counted in one of the fourteen Module Rate Counters. The input from particular a CPM will not count if it fails parity checks or if it is disabled in the Backplane Disable Register.

Similar logic is used to count the parity-checked 3-bit summed hits from the local crate and from the three remote crates. The four Crate Rate Counters are incremented in this logic.

For each of the eight threshold hit counts sent from the System CP-CMM to the CTP, the 3 bits are ORed to produce a1-bit signal. The eight signals, one per threshold, are counted in eight of the System Rate Counters 0-7.

3.5.12.2 Jet Rate Metering

This uses Crate Hit Counters 0 and 1, and not 2 and 3.

Starting from the parity-checked CMM input from each JEM except numbers 0, 6, 7 and 15, the eight 3-bit hit counts are ORed to produce eight 1-bit signals, one for each main jet threshold. These signals are ORed to produce a single signal for the JEM concerned.

For JEMs 0, 6, 7, and 15, parity-checked inputs are ORed to produce 12 signals, one for each main jet threshold hit count and one for each forward jet threshold hit count. The 12 signals are ORed to produce one signal for the JEMs concerned. The 16 signals, one from each JEM, are counted in the 16 Module Rate Counters.

In both cases, he input from particular a JEM will not count if it fails parity checks or if it is disabled in the Backplane Disable Register, and inputs for a particular hit threshold will not count if disabled in the Module Rate Mask register.

Similar logic is used to count the summed hits from the local crate and the remote crate. Two of the Crate rate Counters are incremented in this logic.

For each of the eight 3-bit main jet hit counts sent from the System Jet-CMM to the CTP, the 3 bits are ORed to produce a1-bit signal. For each of the four 2-bit forward jet hit

counts, the four bits (two from the left end, two from the right end) are ORed to produce a 1-bit signal. These signals are counted in the twelve System Rate Counters.

3.5.12.3 Energy Rate Metering

This version counts threshold hits in the system FPGA only, as hot trigger towers will be identified in the CP and JET crate counts. The Module Rate Counters, Crate Rate Counters, and Rate Masks are not used.

The 12 bits sent to the CTP (8 missing-ET hits, 4 sum-ET hits) are counted in the twelve System Hit Counters.

3.5.13 Event Data Readout

3.5.13.1 General Principles

The CMM responds to an L1A by providing data readout to the data acquisition system and, for some CMMs, to the Level-2 Trigger via the RoI Builder. The two mechanisms differ only in fine detail, and each uses a dual-port memory, G-Link FIFO and Shift register, as shown in Figure 3.

On each 40 MHz clock cycle, copies of the input hits and parity from the backplane, intermediate input sums, intermediate output sums and final hit counts are stored in the dual-port memories. These data are overwritten when the memory pointers wrap round 256 clock cycles later.

When an L1A occurs, the readout logic on the CMM copies data from the dual-port RAM to the G-Link FIFO before it can be overwritten. The read pointers used in the copy are staggered, so that all data originating from the same bunch crossing in the LHC machine are written at the same relative position in the G-Link FIFO.

Assuming that the G-Link is not busy, the data are then read from the G-Link FIFO and loaded into shift registers, one for each of the 20 G-Link data pins. These data are shifted serially into the G-Link, followed by a longitudinal odd-parity bit on G-Link pin. The data are transmitted by the G-Link, received at the ROD, reformatted into S-Link ROD fragments, and sent to the DAQ or RoI Builder.

3.5.13.2 Handling Multiple Time Slices

Data from a programmable number of clock cycles (i.e. several “time slices”) may be copied from the Dual-port RAM into the G-Link FIFO. The G-Link transmission begins as the G-Link DAV signal is asserted by the CMM. If several time slices are to be sent, the CMM loads each successive time slice into the shift register, sending the data to the G-Link without a pause while maintaining the DAV signal active, and with each timeslice followed by an odd parity bit on each G-Link data line.

The CMM maintains a counter for the bunch-crossing number, which is reset by the BCReset signal from the TTCrx. When an L1A is received, this BCN is copied to a BCN FIFO. The readout controller inserts the BCN data into the shift register, with the same BCN used for every slice of a multi-slice event.

After all timeslices for one event have been sent, the readout logic de-asserts the G-Link DAV signal, and the G-Link goes idle. This creates a “DAV Gap” which the ROD recognises as the end of the data for the event concerned. DAV must remain inactive for enough clock cycles for the ROD to complete the current event processing and prepare for

the next event. The duration of the DAV Gap should be a firmware parameter whose value can be set when the ROD firmware has been completed.

If the BC or time slice FIFOs overflow, the DAQ FO bit is latched in the status register; the control logic also informs the ROD via a status bit (FO) in the data stream. The bit remains set until the G-Link FIFO is empty, ensuring that all potentially affected events are labelled as such. A second status bit, the Recorded FIFO Overflow, RFO, is set at the same time, but remains set until cleared by the Clear Errors control bit. FO and RFO are both read via the Status Register. The FIFO overflow condition should not occur if the system is in-step and operating correctly.

3.5.13.3 Slice Readout for e/γ and τ-counting CMMs

The 35-bit format used for e/γ and τ CMM readout is illustrated in Figure 22, and includes some empty bit fields for maximum compatibility with the Jet-counting CMM. G-Link bits 0-11 carry copies of the incoming backplane data from CPMs 1-11, with parity and one bit each of the bunch-crossing number for the L1A. G-Link bits 12 and 13 carry copies of the incoming backplane data from CPMs 12 and 13 with parity. Bits 14-16 carry sub-sums from the three remote CMMs, with the FIFO Overflow bit also carried on bit 14. G-link bits 17 and 18 carry the local sub-sums and the total hit counts. G-link bit 19 is all zeros. All G-Link pins carry an odd-parity bit after the last data bit of each slice (i.e. the value of the added parity bit is chosen so that each pin carries an odd number of set bits, including the parity bit itself).

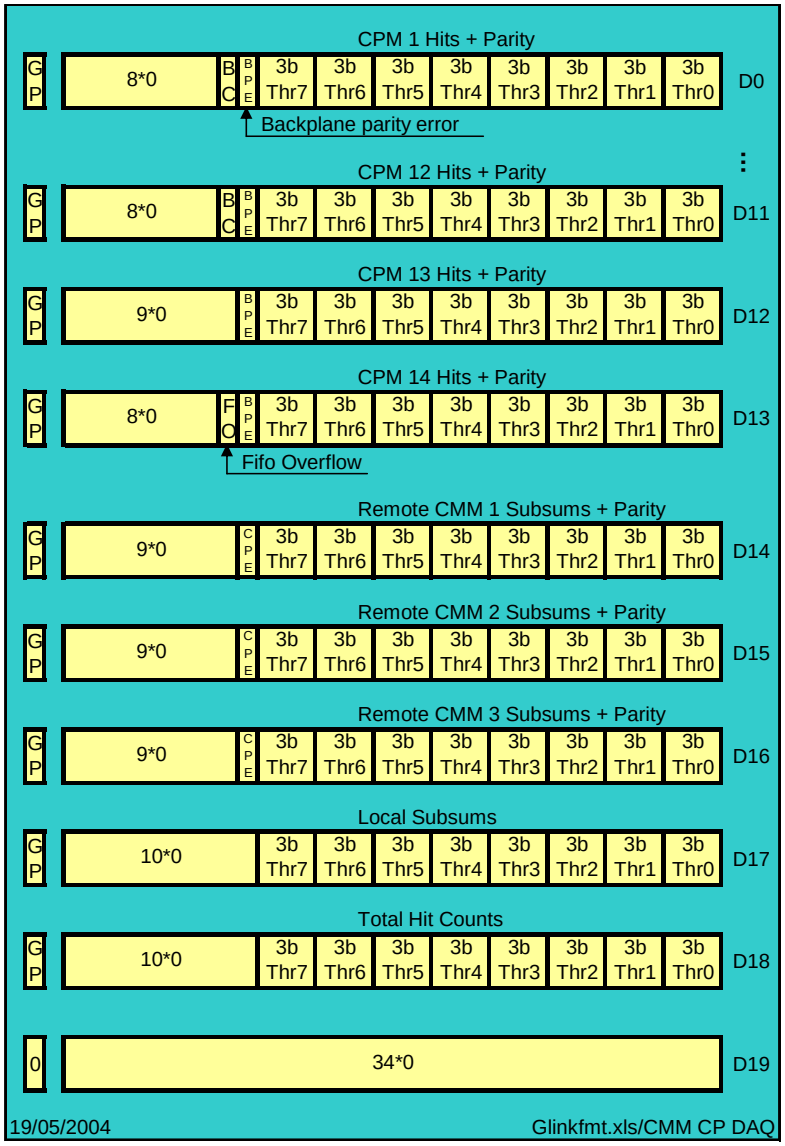

Figure 22: Serial readout format from Cluster-merging CMM

3.5.13.4 Slice Readout for Jet-merging CMMs

The 35-bit format used to read out main jet trigger and forward (Left and Right) jet hit-counts from Jet CMMs is illustrated Figure 23. G-Link bits 0-15 carry copies of the backplane data from JEMs 0-15, and bits 0-11 also carry one bit each of the bunch counter number corresponding to the L1A. G-Link bit 14 also carries the FIFO overflow bit. G-link bit 16 carries the remote main jet count sub-sums and the four Jet-ET hit bits, and G-Link bit 17 carries the local main jet sub-sums and also part of the total forward jet counts. G-Link bit 18 carries total main jet counts and the remaining total forward jet counts. G-link bit 19 carries the remote and local forward jet sub-sums. All G-Link bits carry an odd-parity indicator after the last data bit of each slice.

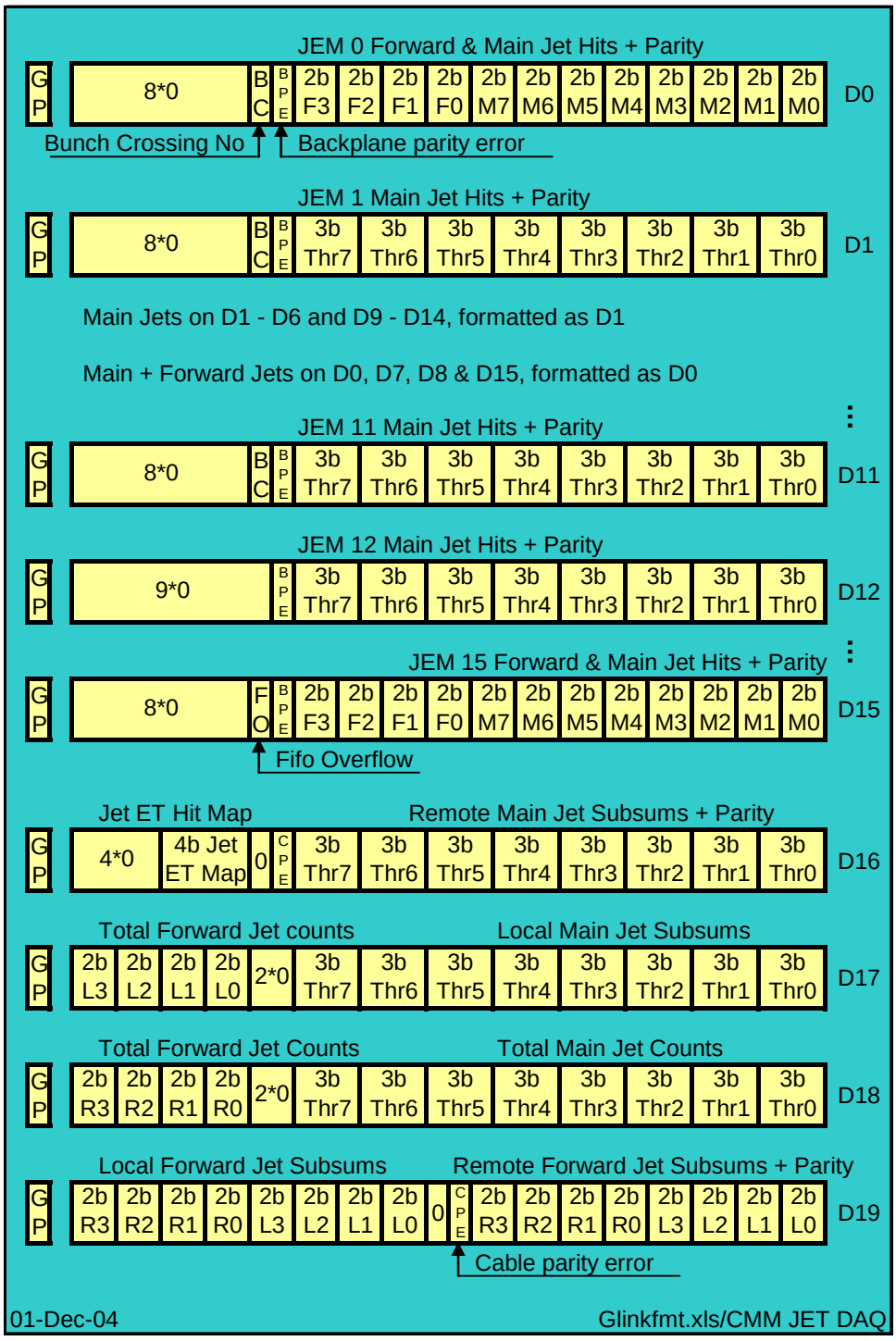

Figure 23: Serial readout format from Jet-merging CMM

3.5.13.5 Slice Readout for Energy- merging CMMs

The format used for energy-merging CMM readout is illustrated in Figure 24. G-Link bits 0-15 of energy-merging CMMs carry copies of the compressed scale E_X, E_Y, E_T and parity received over the backplane from JEMs 1-16. G-link bits 16 and 17 carry the remote energy sub-sums and the E_T and E_{TMiss} hits. These are not coded, allowing access to individual bit values. G-Link bits 18 and 19 carry the module energy sub-sums, 12-bit bunch counter and the DAQ FIFO overflow bit. All G-Link bits carry an odd-parity indicator after the last data bit of the last slice.

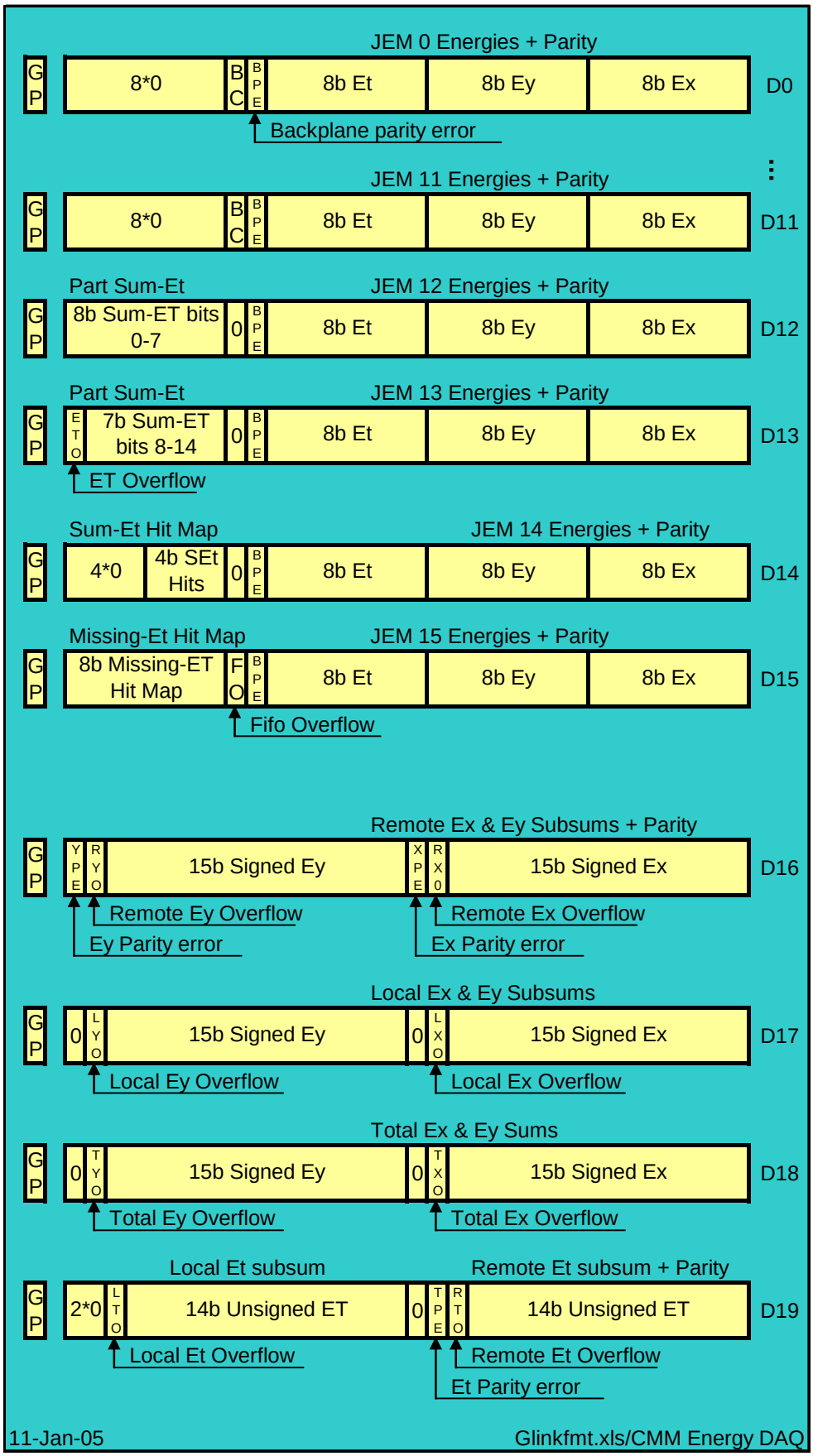

Figure 24: Serial readout format from Energy-merging CMM

3.5.14 RoI Readout

RoI information is generated in the System CMMs performing energy summing and Jet summing (all other RoI information required by the Level-2 Trigger is generated in CPMs and JEMs). RoI data is generated and stored in FIFOs in the system-summing FPGAs for every 40 MHz clock.

On receipt of the L1A signal, the readout logic on the CMM copies and reformats the RoI data into the RoI readout FIFOs. When the RoI G-Link to the R-ROD becomes available; the controller transmits the stored RoI data to the R-ROD. The control logic also informs the ROD via a status bit in the time slice data stream if the BC and time slice FIFOs have overflowed (see 3.2.8. above). A single slice of RoI data is always read on receipt of L1A, regardless of the number of time slices of event data.

The format of Energy RoI data is identical to that for one slice of Energy-merging readout corresponding to the L1A as shown in Figure 24. From this, the ROD uses only the Total E_X, E_Y, E_T (G-Link pins D18, 12-13) and Sum- E_T and missing- E_T threshold data (pins D14, D15) to build the RoI datum for Level-2, and the Bunch Crossing number (one pin on each of D0 to D11) for checking purposes.

The format of the jet-E_T Hit RoI data is similarly identical to that for one slice of jet readout as shown in Figure 23. From this, the ROD uses only the jet-E_T hit data (4 bits on pin D16) to build the RoI datum for Level-2, and the Bunch Crossing number for checking purposes.

3.5.15 G-Link Clocking and Stability

Prototype CMMs have obtained the G-Link 40 MHz clock from the TTC system. However, the G-Link is sensitive to the clock quality, and particularly to the level of clock jitter. In production CMMs, the G-Link should be driven from a low-jitter crystal clock. Implementing this requires the G-Link FIFO to be fully asynchronous, and also requires that the ROD be capable of receiving G-Link transmission from asynchronously-clocked G-Links.

Tracks from the crystal source to the G-Link must be carefully laid out and impedance controlled. The high-speed G-Link signal will be sent optically to guarantee interference-free reception.

4 PCB Layout

The module layout is shown in Figure 25. As far as possible, front panel components are positioned in lines with corresponding items in the CPM.

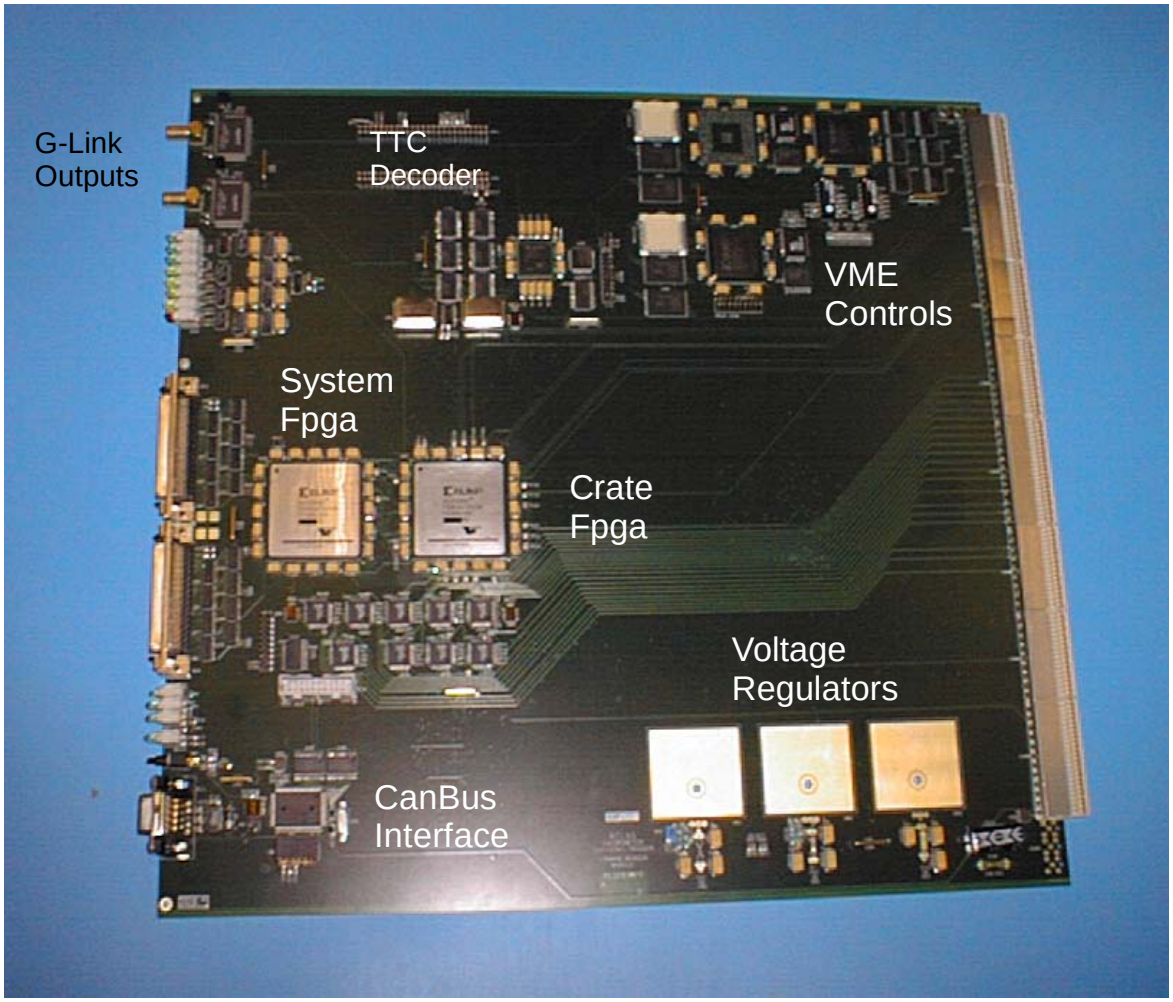

Figure 25: CMM layout.

5 Implementation

All logic described in section 3.5 is implemented in FPGAs. Two XCV1000E-6FG860 FPGA devices are used in the real-time signal path, one each for crate-level and system-level summation to minimise the latency. The XCV1000E, XCV16000E & XCV2000E devices all use the same FG860 footprint, so upgrades are possible without changes to the PCB.

All CMMs include a System-ACE device with a standard Compact Flash card holding the FPGA configuration versions for hit- and energy-summing functions. Appropriate FPGA configurations are selected and loaded automatically on power-up, based on backplane pin configuration as specified in Table 1, or by VME command. This scheme effectively assigns crate numbers 0-3 to the CP system and 4-5 to the JEP system, leaving crate numbers 6 and 7 unused. Crate number logic in the backplane is inverted, so the table includes the crate numbers and GEOADD pin values.

Crate	GEOADD(6:4)	GEOADD(0)	Module Function
0-2	111,110,101	0 (Left)	τ Crate-CMM
3	100	0	τ System-CMM
0-2	111,110,101	1 (Right)	e/γ Crate-CMM
3	100	1	e/γ System-CMM
4	011	0	Energy Crate-CMM
4	011	1	Jet Crate-CMM
5	010	0	Energy System-CMM
5	010	1	Jet System-CMM
6-7	001,000	Any	Reserved

Table 1: Determination of Module functions from Geographical VME Addresses

5.1 VME Interface

The module uses a subset of the VME standard, referred to as "VME--" and defined in [2.9]. The subset provides only the signal lines necessary to execute A24, D16 cycles from a single crate master without interrupts or arbitration. All cycles are A24, D16. VME interfacing is implemented by an FPGA, with essential reset signals in a CPLD. All address decoding and slow control registers are implemented in these devices.

Geographical addressing is implemented using signal levels as defined in the backplane specification, see [2.11]. The module self-configures as a Crate or System CMM with algorithms for the Cluster or Jet/Energy system, based on the value read from the pins defined in the common backplane specification, according to Table 1.

5.2 TTCrx Daughter Module

This module interfaces with the TTC system and provides all the clocks and control signals for the merger module.

The TTCrx chip includes an I2C interface to its internal registers [2.4]. The CMM provides a VME-- to I2C interface which enables these registers to be accessed from VME--. This interface is implemented in an XCV100E Xilinx FPGA, which always acts as the I2C bus master. The only other device on the I2C bus is the TTCrx chip itself, which always acts as a slave.

The VME--I2C interface is implemented using two VME-- registers: TTCrx Control and TTCrx Status. Each access to the TTCrx Control register initiates two I2C accesses to the TTCrx chip - the first to write to the TTCrx Pointer register, and the second to read/write the TTCrx Data register. The results of an I2C access can be read in the VME-- TTCrx Status Register.

Full details of the CMM VME-- registers are given the programming model, see 5.8, and details of the TTCrx I2C registers and protocol are given in the TTCrx chip specification [2.4]. A full description of I2C-bus protocol, of which only a subset is used here, is given in the I2C-bus specification [2.5].

5.3 CANBus Interface

The Common Merger Module uses a Fujitsu MB90F591 microcontroller [2.14] as an interface to the Controlled Area Network Bus (CANBus) in the processing crate. The architecture is used throughout the calorimeter trigger, and allows the module to pass voltage and temperature information via the Timing Control Module to the ATLAS Detector Control System (DCS). The Common Merger Module has eight parameters to be monitored, comprising the three voltages generated on-board (see 5.6), three FPGA temperatures, and two G-Link temperatures. The microcontroller can be programmed from the front panel and reset both from the front panel and via VME.

The temperatures of the three FPGAs on the module, the 'system', 'crate', and 'I2C' devices, are obtained using a MAX1668 Serial Master Bus chip (SMBus) controlled by the microcontroller. There are three connections between the microcontroller and this device, namely clock, data and an alert. The Alert pin is connected to interrupt input INT0 (p76) on the microcontroller. If an FPGA temperature exceeds a pre-determined temperature value, an exception routine deals with the problem.

The voltage levels are measured using the 10-bit Analogue to Digital Converter in the microcontroller. Channels 0, 1 and 2 are connected respectively to the 1V5, 2V5 and 3V3 supplies, with the reference voltage connected to the +5V supply. The temperatures of the two HP G-Link (DAQ and ROI) chips are obtained using two LM35D temperature sensors bonded to the heat sinks. The outputs from the temperature sensors are connected to channels 3 and 4 of the 10-bit Analogue to Digital Converter.

Port 7 of the microcontroller is connected to the geographical address input pins from the backplane. From this input, delays are calculated to prevent two microcontrollers on the same bus transmitting at the same time, thus preventing bus contention.

Port 8 is connected to a fixed pull-up, pull-down resistor network which is a fixed code for the CMM module type. The details of this code can be found in addressing scheme for the TTC and Busy network [2.13]. For the CMM the value is set to 0x04.

Port 1 of the microcontroller is connected via a buffer to the VME data bus. This is used for a software version code which can be read by VME when required. The enable signal for this buffer is controlled by the VME CPLD. Port 2 is connected to buffered signals from the VME CPLD. These control signals enable access to software version register (default) or other registers within the microcontroller.

5.4 Inputs and Outputs

5.4.1 Front Panel Monitoring (LEDs)

The LEDs are located at the top (status indicators) and bottom (power indicators) of the front panel, positioned to match the CPM layout. Colours and behaviour follow a common convention throughout the calorimeter trigger. Fast signals are stretched so that they light the LEDs for long enough to be seen. Green signals indicate normal static conditions, yellow indicate transient operating conditions, and red indicate errors.

Description	Signal name	Colour	Panel Label	
			Module V1-2	Module fromV3
+5 Volts		Green	5.0	5.0 (2 LEDs parallel)
Internally generated +3.3V		Green	3.3	3.3
Internally generated +2.5V		Green	2.5	2.5
Internally generated +1.8V		Green	1.8	1.8
System clock is active	SYSCLK	Green	CK	CLK
System ACE Status	ASTST	Green	ASTAT	AST
System ACE Error	AERR	Red	AERR	AER
Configuration Done	ALL_DONE	Green	DONE	DONE
TTC Ready	TTC_READY	Green	TR	TTC
DAQ G-Link ready	GDAQ_LNKRDY	Green	DR	DLR
RoI G-Link ready	GROI_LNKRDY	Green	RR	RLR
DAQ G-Link active	GDAQ_DAV	Yellow	DD	DDV
RoI G-Link active	GROI_DAV	Yellow	DR	RDV
VME access in progress	Board_Select	Yellow	BS	BSEL
DAQ FIFO empty	EFIFO_Busy	Yellow	FE	EF
Level-1 accept	L1Accept	Yellow	LA	L1A
Crate Trigger Hits	CrateTrigHit	Yellow	CH	CHT
System Trigger Hit	SysTrigHit	Yellow	SH	SHT
Parity Error		Red	PE	PER
DAQ FIFO Full (Overflow)		Red	FF	FF
CAN Transmit		Yellow	-	CTX
CAN Receive		Yellow	-	CRX

Table 2: Front Panel Led Indicators

The trigger hit LEDs are divided into two groups, one indicating activity at the local crate level and one indicating system-level activity (used only on System CMMs). In the CP and JEP crates, a light is lit when any of the corresponding threshold counts exceeds 0.

5.4.2 Rear Panel Input and Outputs

The rear connector to the module carries signals from the backplane and also signals that pass though the backplane to other CMM modules.

5.4.2.1 Signals from the Backplane

1) High-speed hit and energy data from CPMs or JEMs
2) VME--
3) Encoded TTC signal (includes 40 MHz clock and L1)
4) CANBus monitoring bus.

Details of the CMM backplane connections and signal names are specified in the common Processor Backplane Specification [2.11] and are reproduced in Appendix A. For example, the incoming data bits from CPM or JEM in crate station 14 are labelled P14_0 to P14_24. The bits are used as follows:

- For data from CPMs: Threshold 1(2:0) -> PX_2 to PX_0;
  Threshold 2(2:0) -> PX_5 to PX_3
  ….etc to Threshold 8(2:0) -> PX_23 to PX_21;
  Parity PX_24
- For jet data from JEMs, the same arrangement;
- For energy data from JEMs: E_X(7:0) -> PX_7 to PX_0;
  E_Y(7:0) -> PX_15 to PX_8;

E_T(7:0) ->	PX_23 to PX_16;
Parity	PX_24

All signal and clock traces to or from the backplane carrying signals at or above 40 MHz must have controlled impedance matching that of the backplane. Particular care is needed in receiving the input hit and energy data, which is sent single-ended from back-terminated CMOS devices on the processor modules.

5.4.2.2 Signals passing through the Backplane

Pins passing through the backplane carry the 40 MHz parallel signals to or from other CMMs.

A passive transition module is required at the rear of the backplane to adapt the backplane pin layout for connection to up to three cables carrying differential signals between Crate- and System-CMMs, using three 3M 10168-6000EC 68-pin connectors (standard 68-pin SCSI-3 connectors on the prototype modules),. The cables conform to the CERN IS 23 specification (including halogen free), and are round and shielded, and of 100Ω nominal impedance. (standard SCSI-3 Cables for the prototype modules). Track impedances on the CMM and the transition module match the cable impedance. Each cable carries 27 signal pairs, including two pairs (labelled "R" in figures 11, 12 14 and 15) reserved for future expansion. These are connected to pins in the same FPGA as the committed 25 pairs. The remaining pairs are used for cable ground via the grounding network (see section 5.5). The signals are carried differentially, with CMM pins M_0+, M_0- to M_26+, M_26- used only for input. The remaining two groups of 50 pins (M_27+, M_27-) to (M_53+,M_53-) and (M_54+, M_54-) to (M_81+,M_81-) used for input or for output according to module firmware configuration. The pinout details appear in Appendix E, F and G. Identical transition modules are used at both ends of cable links. The transition module is shown in Figure 26 and the overall system cabling is illustrated in Figure 27.

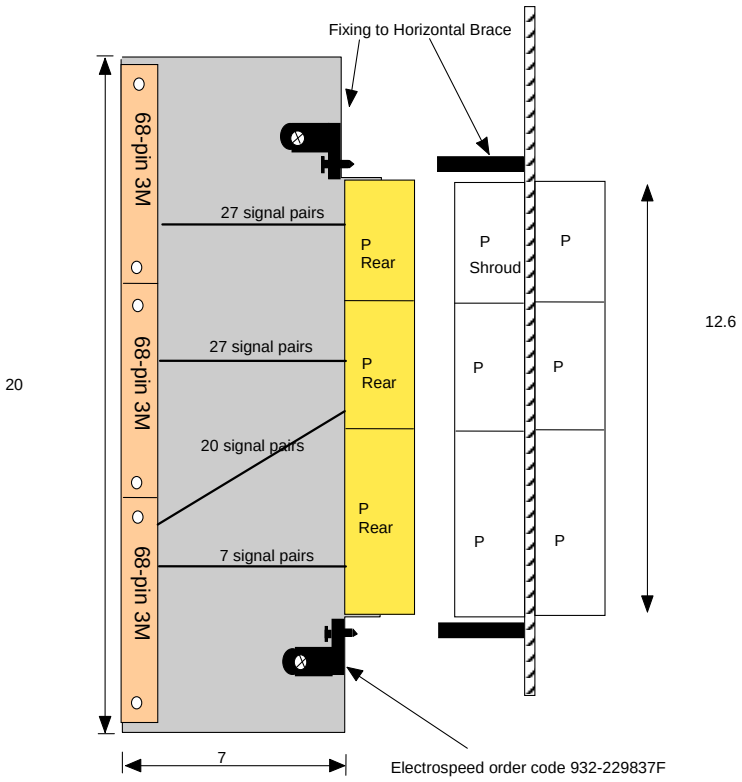

Figure 26: Rear Transition Module

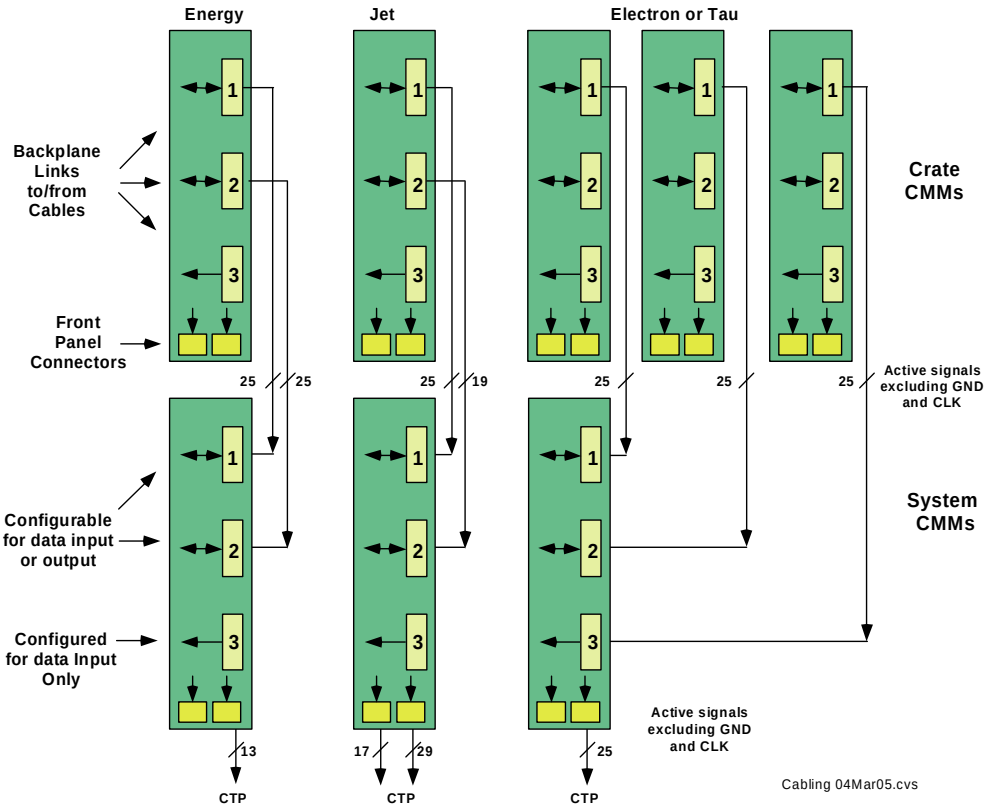

Figure 27: Interconnection scheme for CMMs (transition modules omitted for clarity).

5.4.3 Front Panel Outputs

The front panel provides two 3M 10168-6000EC 68-pin IDC connectors as used on the CTP_IN module (standard 68-pin SCSI-3 connectors were used on the prototype modules). Each connector carries up to 33 differential signals to the CTP, depending on the module firmware configuration. The remaining pair is used to provide an optional signal ground connection to the CTP (see section 5.5). The cables conform to the CERN IS 23 specification (including halogen free), and are round and shielded, and of 100Ω nominal impedance. The first connector carries all CP and Energy hits and the main JEP hits, while the second connector is used only for the forward jet counts from the JEP system, as shown in Figure 27. Any spare I/O pins in the FPGA hosting the system summation algorithms are connected to unused pins on this connector to provide for possible future expansion. All PCB traces match the cable impedance. The pinout for these connectors is included as Appendix B, and matches the pinout of the CTP_IN module.

The front panel also houses two Small Form-factor Pluggable Multimode 850 nm optical transceivers with LC connectors (Infineon V23818-M305-B57) for G-Link RoI and Slice readout (electrical Lemo-00 connectors in the prototypes). These devices are economical and their active parts are plug-in and therefore replaceable. Only the transmitting half of the transceiver is used.

The front panel also has two Lemo-00 connectors providing copies of the 40 MHz clocks used by the two main FPGAs

5.5 Cable Grounding Scheme

The cable-grounding scheme follows that developed for the high-speed Pre-processor to CPM and JEM links. Dedicated cable pairs (labelled GND in the pinouts) from CMM to CTP and between CMMs are joined together for each cable to form a cable signal ground point. Provision is made on the module to connect each of these via a separate resistor, filter, or solder link, to a common low-impedance connection to module signal ground. In the case of links between CMMs, the filter components are placed on the transition module, while for the links to the CTP they are placed on each CMM. The scheme is shown in Figure 28.

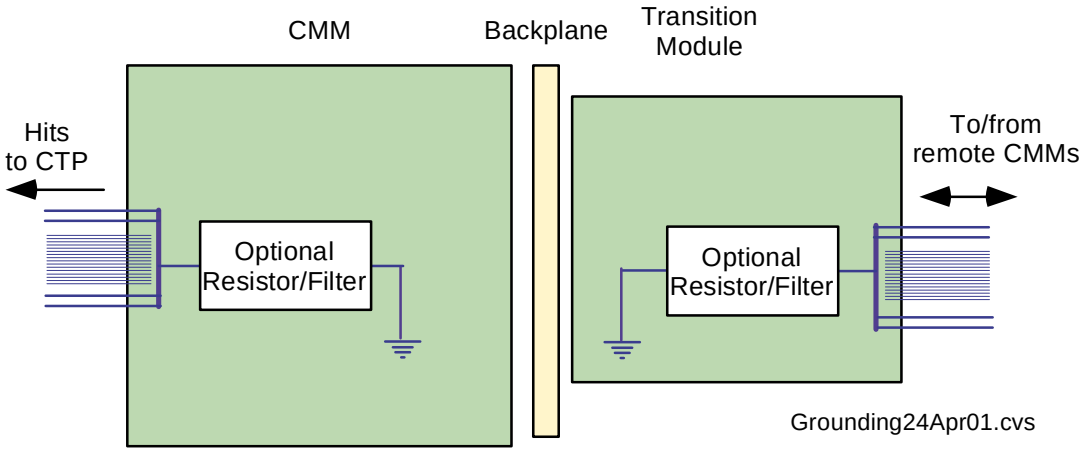

Figure 28: Grounding scheme for CMM cables.

5.6 Power Requirements

The crate backplane provides +3.3V and +5V supplies. However, the 3.3V supply is reserved exclusively for power-sensitive components such as the LVDS transceivers, and is not used on the CMM. Supplies of +1.8V, +2.5V and +3.3V for other devices are generated on-board from the +5V supply. The total current drawn at +5V may be up to 10A.

5.7 Instrument Access points

5.7.1 Test and Set-up Points

1. Logic analyser probe points are provided on various data paths to aid in debugging the module.
2. Oscilloscope test points are provided for important signals including L1A, G-Link DAV.
3. JTAG boundary scan port
4. A single In-System-Programming (ISP) port is included for configuring FPGAs. All FPGAs are linked to this port. FPGA configurations are normally memory resident, but loading from VME or ISP is possible for testing.

5.7.2 Ground Points

Ground points are provided for scope probe grounding in exposed areas of the motherboard.

5.8 Programming Model

5.8.1 Guidelines

These are to aid the software control of the module.

1. The computer can read all registers; hence there are no 'write only' registers. The register bits generally have the same meaning for reads as for writes.
   1.1 All Status Registers shall be read-only registers.
   1.2 All Control Registers shall be Read/Write registers.
   1.3 Reading back a register generally returns the last value written.
   1.4 Attempts to write to read-only registers or undefined portions of registers result in the non-modifiable fields being left unchanged.
2. It is illegal for the computer to read or write a value that the CMM module itself is able to modify at the same time.
3. If the computer reads a register (e.g. a counter) which the CMM module is modifying, a well-defined value is returned, for example by synchronising the data capture to the 40 MHz clock.
4. When the address space occupied by the CMM module is accessed, it always responds with a handshake to avoid a bus error.
5. The power-up condition of all registers is all zeros, unless otherwise stated.

5.8.2 Notation

The names of the registers and bit fields within them are written in *italic*. The names of the signal lines are *underlined italic*. Bit-fields are labelled Input to Card and Output from Card rather than Write and Read to make it clear whether it is the card or the computer which is doing the writing.

In this document, a byte is always an 8-bit field, a word is always 16 bits and a long-word is always 32 bits.

Setting a bit-field means writing a 1 to it, clearing it means writing a 0.

RO means that the computer can only read the value of this register; writing has no effect either to the value or the state of the module.

RW means that the computer can affect the state of the module by writing to this register.

5.8.3 VME Access Modes

The CMM module is addressed using an A24 address bus. The reduced VMEbus does not carry AM codes, and should respond assuming a standard D16 cycle has been issued

5.8.4 VME Register Map

The memory map and detailed assignment of bits may change during the design phase to accommodate requirements not foreseen at the time of writing this document.

The following registers are used in all types of CMM

Byte Address (hex)	Register type	Register Name	Size in bytes	Description
00000	RO	ModuleIdA	2	Module ID Register A
00002	RO	ModuleIdB	2	Module ID Register B
00004	RW	ControlModeReg	2	Control Mode Register
00006	RW	ControlPulseReg	2	Control Pulse Register
00008	RO	StatusReg	2	Status Register
0000A	RO	FifoStatusReg	2	FIFO Status Register
0000C	RO	BpEReg	2	Backplane Parity Error Register
0000E	RO	CEReg	2	Cable Link Parity Error Register
00010	RW	BpDisReg	2	Backplane Link Disable Register
00012	RW	CDisReg	2	Cable Link Disable Register
00014	RO	PCReg	2	Parity Count Register
00016	RW	BpTimingRegA	2	Backplane Timing Register A
00018	RW	BpTimingRegB	2	Backplane Timing Register B
0001A	RW	CTimingReg	2	Cable Link Timing Register
0001C	RW	PipeDelay	2	Pipeline Delay Register
0001E	RW	DaqSliceReg	2	DAQ Slice Register
00020	RW	DaqOffsetBpData	2	DAQ addr offset, backplane data
00022	RW	DaqOffsetCrtReslts	2	DAQ addr offset, crate results
00024	RW	DaqOffsetCblData	2	DAQ addr offset, cable data
00026	RW	DaqOffsetSysReslts	2	DAQ addr offset, system results
00028	RW	RoiOffsetBpData	2	RoI addr offset, backplane data
0002A	RW	RoiOffsetCrtReslts	2	RoI addr offset, crate results
0002C	RW	RoiOffsetCblData	2	RoI address offset, cable data
0002E	RW	RoiOffsetSysReslts	2	RoI address offset, system results
00030	RO	FfAddrCrtDaq	2	FIFO address pointers, crate DAQ
00032	RO	FfAddrSysDaq	2	FIFO address pointers, system DAQ
00034	RO	FfAddrCrtRoi	2	FIFO address pointers, crate RoI
00036	RO	FfAddrSysRoi	2	FIFO address pointers, system RoI
00040	RW	TtcrxControl	2	TTCrx Control Register
00042	RO	TtcrxStatus	2	TTCrx Status Register
00050	RO	CmmCId	2	Crate FPGA firmware version
00052	RO	CmmSId	2	System FPGA firmware version
00054	RO	I2cId	2	I2C FPGA firmware version
00056	RO	VmeId	2	VME CPLD firmware version

00058	RO	SystemAceVMEIf	2	System Ace VME Interface
0005C	RW	CanAccessA	2	CAN Access Register A
0005E	RW	CanAccessB	2	CAN Access Register B
00060	RW	SumEtThr1Reg	2	Sum-ET Threshold 1
00062	RW	SumEtThr2Reg	2	Sum-ET Threshold 2
00064	RW	SumEtThr3Reg	2	Sum-ET Threshold 3
00066	RW	SumEThr4Reg	2	Sum-ET Threshold 4
00068	RW	JetEtThr1Reg	2	Jet-ET Threshold 1
0006A	RW	JetEtThr2Reg	2	Jet-ET Threshold 2
0006C	RW	JetEtThr3Reg	2	Jet-ET Threshold 3
0006E	RW	JetEThr4Reg	2	Jet-ET Threshold 4
00070	RO	ModuleRateCounters	16*4	Module Rate Counters
000B0	RO	CrateRateCounters	4*4	Crate Rate Counters
000C0	RO	SystemRateCounters	12*4	System Rate Counters
00100	RO	NormalisationRate	1*4	Normalisation Rate Counter
00104	RW	ModuleRateMask	2	Module Rate Mask Register
00106	RW	CrateRateMask	2	Crate Rate Mask Register
001FA	RW	TtcI2Cid	2	TtcI2cId Register
001FC	RO	TtcBrcst	2	TtcBrcst Register
001FE	RO	TtcDq	2	TTC DQ Register
00200	RO	TtcDump	32	TTC Dump RAM
01000	RW	DprCrtFpgaIput	16384	DPR Access: Crate FPGA Input Data
05000	RW	DprCrtFpgaOput	2048	DPR Access: Crate FPGA Output Data
05800	RW	DprSysFpgaIput	3072	DPR Access: System FPGA Input Data
06400	RW	DprSysFpgaOput	2048	DPR Access: System FPGA Output Data
06C00	RW	FifoCrtFpgaIput	16384	FIFO Access: Crate FPGA Input Data
0AC00	RW	FifoCrtFpgaOput	2048	FIFO Access: Crate FPGA Output
0B400	RW	FifoSysFpgaIput	3072	FIFO Access: Sys FPGA Input Data
0C000	RW	FifoSysFpgaOput	2048	FIFO Access: Sys FPGA Output Data
0C800	RW	DprRoi	3072	DPR Access: RoI Data
0D400	RW	FifoRoi	3072	FIFO Access: RoI Data
0E000	RW	DprMainJetEtLut	8192	Main Jet-ET LUT
010000	RW	DprFwdJetEtLut	8192	Forward Jet-ET LUT
012000	RW	MissEtLut	16384	Missing-ET LUT

5.8.4.1 Module ID Register A

All bit fields are outputs from card

Bit	Descriptive Name	Signal name
0-15	*ModuleID*	*RALNo*

Module ID Number
A unique 8-bit number for each module type, set to 2417 for the CMM.

5.8.4.2 Module ID Register B

All bit fields are outputs from card

Bit	Descriptive Name	Signal name
0-7	Module Serial number	SerNo
8-11	Hardware Revision Number	RevNo
12-15	*null*	

Module Serial Number
A unique 8-bit number for each module, starting at 1 and set by solder jumpers.

Revision Number
Four-bit revision number starting at 1 and set by solder jumpers.

5.8.4.3 Control Mode Register

All bit fields are inputs to card.

Bit	Descriptive Name	Signal name
0 (LSB)	*Enable Playback Mode*	*ENPBK*
1-4	*GEOADD Bypass*	*GEOBP*
5	*TTC Clock enable*	
6	*TTC Protect*	
7	*LaserDisable_RoI*	
8	*Laser_Disable_DAQ*	
9	*Rate Counter Inhibit*	
10–15	*null*	

Enable Playback Mode
Bit 0
Writing a 1 to this bit causes the crate FPGA Input Data dual port memory to be used as a data playback memory. In this mode, input from CMMs or JEMs is ignored, and data from the memory enters the crate-summing algorithm. Data from the module continues to be written into other memories in this mode.

Geoadd Bypass
Bit 1-4
On power-up, these bits are set to the value obtained from the geographical addressing pins GEOADD(0) (bit 1) and GEOADD(6:4) (bits 4-2) and used to establish the module

function as in Table 1. If the Geoadd bypass bits are subsequently changed and the Crate- or System- FPGA reload bits set (Control Pulse Register), the module adopts an alternative function as if the VME GEOADD bits had been set on power up to the value in the bypass register. This feature is for testing groups of modules. Bypassing the Geographical address in this fashion changes only the firmware to be downloaded. VME and TTC address decoding is performed using the VME GEOADD bits and so is not altered by changes made here.

TTC Clock Enable
Bit 5
When this bit is set, the CMM uses the TTC clocks. When this bit is cleared, the CMM uses the on-board 40 MHz oscillator. Trying to set this bit when the TTC is not ready has no effect (the bit remains cleared).

TTC Clock Protect
Bit 6
This bit controls the TTC Decoder protection scheme described in the TTCDec specification, which determines the clock behaviour when the TTC clock is lost. When this bit is cleared (Debug mode), the TTCDec automatically switches to use a crystal clock if the TTC signal is lost. When the bit is set (Protected mode), the TTCDec does not switch automatically. This prevents a TTC problem being concealed by the automatic switchover.

Laser_Disable_RoI
Bit 7
When this bit is set, the laser used to drive the RoI G-Link is turned off to reduce power consumption. The bit is initially off (laser enabled).

Laser_Disable_DAQ
Bit 8
When this bit is set, the laser used to drive the DAQ G-Link is turned off to reduce power consumption. The bit is initially off (laser enabled).

Rate Meter Inhibit
Bit 9
When this bit is set, incrementing of the rate meter counters and the normalization counter is inhibited.

5.8.4.4 Control Pulse Register

All bit fields are inputs to card. All bits read back as zero, and writing a zero to a bit has no effect.

Bit	Descriptive Name	Signal name
0 (LSB)	*Reset Module*	*BOARD_RESET*
1	*Reset TTC*	TTC_RESET
2	*Reset RoI G-link*	GROI_RESET
3	*Reset DAQ G-link*	GDAQ_RESET
4	*Reset CAN controller*	VMECANRESET
5	*Reset I2C controller*	I2C_RESET
6	*Null*	
7	*null*	
8	*Reset DLL*	DLL_RESET
9	*Clear Errors*	CLRE
10	*Reset Rate Meter Counters*	
11-15	*null*	

Reset Module
Bit 0
Writing a 1 to this bit resets the module to the power-on state. This includes restoring the module geographical address to that obtained from the backplane, and reloading the FPGAs accordingly.

Reset TTC
Bit 1
Writing a 1 to this bit resets the TTC daughter board to the power on state.

Reset RoI G-link
Bit 2
Writing a 1 to this bit resets the RoI G-link to the power on state.

Reset DAQ G-link
Bit 3
Writing a 1 to this bit resets the DAQ G-link to the power on state.

Reset CAN controller
Bit 4
Writing a 1 to this bit resets the CAN microprocessor to the power on state.

Reset I2C controller
Bit 5
Writing a 1 to this bit resets the I2C interface controller to the power on state.

Reset DLL
Bit 8
Writing a 1 to this bit resets to the power-on state the Delay-Locked Loops (DLLs) used for clock management within the Crate and System FPGAs.

Clear Errors
Bit 9
Writing a 1 to this bit resets to zero the Backplane Parity Error Register, the Cable Parity Error Register, the Parity Count Register, and the FIFO Overflow and Recorded FIFO Overflow bits.

Reload Crate-summing FPGA
Bit 10
Writing a 1 to this bit reloads the Crate-summing FPGA with firmware corresponding to the module geographical address specified in the Geoadd Bypass field in the Control Mode Register.

Reload System-summing FPGA
Bit 11
Writing a 1 to this bit reloads the System-summing FPGA with firmware corresponding to the module geographical address specified in the Geoadd Bypass field in the Control Mode Register.

Reset Rate Counters
Bit 12
Writing a 1 to this bit sets all rate meter counters and the normalisation counter to zero.

5.8.4.5 Status Register

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0 (LSB)	Combined Parity Error	
1	FPGA Load Complete	
2	DAQ FIFO Overflow	DAQFO
3	*Null*	
4	I2C FPGA loaded	DONE_I2C
5	Crate FPGA loaded	DONE_CMM
6	System FPGA loaded	DONE_CMMS
7	TTC Ready	TTC_READY
8	Crate FPGA DLL locked	CMM_LCK_DLL
9	System FPGA DLL locked	CMMS_LCK_DLL
10	DAQ G-Link Ready	GDAQ_LINKRDY
11	RoI G-Link Ready	GROI_LINKRDY
12	Recorded FIFO Overflow	
13-15	*Null*	

Combined Parity Error
Bit 0
When this bit is set, a parity error has been detected on one or more of the incoming backplane or cable links since the last error reset. The bit is cleared by the error-reset bit in the Control Pulse Register.

FPGA load complete
Bit 1
This bit is set if all FPGA configurations have loaded successfully.

DAQ FIFO Overflow
Bit 2
This bit is set if any of the readout FIFOs on the module have overflowed. It is cleared by the error-reset bit in the Control Pulse Register.

I2C FPGA loaded
Bit 4
This bit is set if the I2C controller FPGA has been configured correctly.

Crate FPGA loaded
Bit 5
This bit is set if the Crate FPGA has been configured correctly.

System FPGA loaded
Bit 6
This bit is set if the System FPGA has been configured correctly.

TTC Ready
Bit 7
This bit is set when the TTCrx is ready.

Crate FPGA DLL locked
Bit 8
This bit is set when the DLL in the Crate FPGA has successfully locked on to the 40 MHz clock.

System FPGA DLL locked
Bit 9
This bit is set when the DLL in the System FPGA has successfully locked on to the 40 MHz clock.

DAQ G-Link Ready
Bit 10
This bit is set when the DAQ G-link is ready.

RoI G-Link Ready
Bit 11
This bit is set when the RoI G-link is ready.

5.8.4.6 FIFO Status Register

All bit fields are outputs from card.

Bit(s)	Descriptive Name	Signal Name
0	*Crate DAQ FIFO empty*	CMM_DAQ_EF
1	*System DAQ FIFO empty*	CMMS_DAQ_EF
2	*Crate RoI FIFO empty*	CMM_ROI_EF
3	*System RoI FIFO empty*	CMMS_ROI_EF
4	*Crate DAQ FIFO full*	CMM_DAQ_FF
5	*System DAQ FIFO full*	CMMS_DAQ_FF
6	*Crate RoI FIFO full*	CMM_ROI_FF
7	*System RoI FIFO full*	CMMS_ROI_FF
8–15	*null*	

FIFO Status Register
Bits 0–7
Empty and full flags for all of the readout FIFOs on the module.

5.8.4.7 Backplane Parity Error Register

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0-15	*Backplane Parity Error*	*BPERR*

Backplane Parity Error
Bits 0-15
When a bit in this field is set to 1, a parity error has been detected in the data from the corresponding backplane slot since the parity system was last reset.

5.8.4.8 Cable Link Parity Error Register

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0-2	*Cable Parity Error*	*CPERR*
3	*Crate Data Parity Error*	

Cable Link Parity Error
Bits 0-2
When a bit in this field is set to 1, a parity error has been detected in the corresponding cable link since the parity system was last reset.

Crate Data Parity Error
Bit 3
When this bit is set to 1, a parity error has been detected in the data from the crate FPGA since the parity system was last reset.

5.8.4.9 Backplane Link Disable Register

All bit fields are inputs to card.

Bit	Descriptive Name	Signal name
0 - 15	*Disable Backplane Link*	*BPLDisable*

Disable Backplane Link
Bit 0-15
When a bit is set in this field, the input from the corresponding backplane slot (CPM or JEM) is ignored, and zeros enter the crate summing logic. Data recorded in the input memories have value zero but correct (odd) parity.

5.8.4.10 Cable Link Disable Register

All bit fields are inputs to card.

Bit	Descriptive Name	Signal name
0 - 2	*Disable Cable Link*	*CLDisable*

Disable Cable Link
Bit 0-15
When a bit in this field is set, the corresponding cable input from a remote CMM is ignored. Incoming data for the link(s) is set to zero.

5.8.4.11 Parity Count Register

All bit fields are outputs from card. Power-up condition initially sets all bits to 0, but counts errors until all enabled links are transmitting valid data. Error conditions on disabled links are ignored.

Bit	Descriptive Name	Signal name
0-15	*Counted Parity Errors*	*PECOUNT*

Counted Parity Errors
Bits 0-15
This register contains the number of parity errors summed over all channels (cable and backplane) since the parity system was last reset. It is incremented by 1 in each clock tick for which at least 1 parity error was detected, and overflows to 0xFFFF.

5.8.4.12 Backplane Timing Register A

All bit fields are inputs to card.

Bit	Descriptive Name	Signal name
0 - 15	*Backplane Timing Select*	*BPTSel*

Backplane Timing Select
Bits 0-15
This register consists of 8 groups of two bits. Each pair of bits selects one of four possible phases of the 40 MHz clock to latch incoming backplane link data from slots numbered 0-7.

5.8.4.13 Backplane Timing Register B

All bit fields are inputs to card.

Bit	Descriptive Name	Signal name
0 - 15	*Backplane Timing Select*	*BPTSel*

Backplane Timing Select
Bits 0-15
This register consists of 8 groups of two bits. Each pair of bits selects one of four possible phases of the 40 MHz clock to latch incoming backplane link data from slots numbered 8-15.

5.8.4.14 Cable Link Timing Register

All bit fields are inputs to card.

Bit	Descriptive Name	Signal name
0 - 5	*Subsum Timing Select*	*STSel*

Subsum Timing Select
Bits 0-5
This register consists of 3 groups of two bits. Each pair of bits selects one of four possible phases of the 40 MHz clock to latch incoming sub-sum cable link data.

5.8.4.15 Pipeline Delay Register

All bit fields are inputs to card.

Bit	Descriptive Name	Signal name
0 - 3	*Pipeline Latency*	*PL*

Pipeline Latency
Bits 0-5
This 4-bit register sets the pipeline delay in 25ns clock cycles between local intermediate sums and crate summing. The delay should be set equal to the cable delay between CMMs.

5.8.4.16 DAQ Slice Register

All bits are input to card.

Bit	Descriptive Name	Signal name
0 - 2	*ReadoutSlices*	*RSlices*

Readout Slices
Bits 0-2
This register contains the number of time slices of sampled input, intermediate and output data to be read out in response to a Level-1 Accept. During data acquisition this value should normally be limited to 5, as this is the maximum value supported in the ROD data format.

5.8.4.17 DAQ addr offset, backplane data

Bits 0-7
This register contains the offset between the read- and write-address counters of the Dual-Port RAM used in the DAQ readout path to capture the incoming backplane data. When the write address counter reaches zero, the read address counter is loaded with the value contained here.

5.8.4.18 DAQ addr offset, crate results

Bits 0-7
This register contains the offset between the read- and write-address counters of the Dual-Port RAM used in the DAQ readout path to capture the results from the Crate FPGA. When the write address counter reaches zero, the read address counter is loaded with the value contained here.

5.8.4.19 DAQ addr offset, cable data

Bits 0-7
This register contains the offset between the read- and write-address counters of the Dual-Port RAM used in the DAQ readout path to capture the data incoming via cable from

remote CMMs. When the write address counter reaches zero, the read address counter is loaded with the value contained here.

5.8.4.20 DAQ addr offset, system results

Bits 0-7

This register contains the offset between the read- and write-address counters of the Dual-Port RAM used in the DAQ readout path to capture the results from the System CMM. When the write address counter reaches zero, the read address counter is loaded with the value contained here.

5.8.4.21 RoI addr offset, backplane data

Bits 0-7

This register contains the offset between the read- and write-address counters of the Dual-Port RAM used in the RoI readout path to capture the incoming backplane data. When the write address counter reaches zero, the read address counter is loaded with the value contained here.

5.8.4.22 RoI addr offset, crate results

Bits 0-7

This register contains the offset between the read- and write-address counters of the Dual-Port RAM used in the RoI readout path to capture the results from the Crate FPGA. When the write address counter reaches zero, the read address counter is loaded with the value contained here.

5.8.4.23 RoI address offset, cable data

Bits 0-7

This register contains the offset between the read- and write-address counters of the Dual-Port RAM used in the RoI readout path to capture the data incoming via cable from remote CMMs. When the write address counter reaches zero, the read address counter is loaded with the value contained here.

5.8.4.24 RoI address offset, system results

Bits 0-7

This register contains the offset between the read- and write-address counters of the Dual-Port RAM used in the RoI readout path to capture the results from the System CMM. When the write address counter reaches zero, the read address counter is loaded with the value contained here.

5.8.4.25 FIFO address pointers, crate DAQ

Bits 0-15

This register provides read-only access to the internal FIFO address counters of the Crate FPGA DAQ readout path. Bits 0-7 = read counter; bits 8-15 = write counter.

5.8.4.26 FIFO address pointers, system DAQ

Bits 0-15

This register provides read-only access to the internal FIFO address counters of the System FPGA DAQ readout path. Bits 0-7 = read counter; bits 8-15 = write counter.

5.8.4.27 FIFO address pointers, crate RoI

Bits 0-15

This register provides read-only access to the internal FIFO address counters of the Crate FPGA RoI readout path. Bits 0-7 = read counter; bits 8-15 = write counter.

5.8.4.28 FIFO address pointers, system RoI

Bits 0-15

This register provides read-only access to the internal FIFO address counters of the System FPGA RoI readout path. Bits 0-7 = read counter; bits 8-15 = write counter.

5.8.4.29 TTCrx Control Register

This register and the following TTCrx Status Register provide access to the 20 user-accessible internal registers of the TTCrx chip. Refer to the TTCrx Reference Manual version 3 page 13ff for programming details.

All bit fields are inputs to card. Power-up condition initially sets all bits to 0. A TTCrx I/O operation takes place whenever this register is changed, unless the I2C bus is busy (see TTC Status register below). An I2C operation is aborted if the reset bit is set.

Bit	Descriptive Name	Signal name	
0-7	*Data to TTCrx*	*TTCWDATA*	
8-12	*TTC Register Number*	*RRCREGNO*	
13	*Write*	*TTCWRITE*	0 = read, 1 = write
14	*Unused*		
15	*Reset TTCrx Controller*	*TTCCRESET*	

Data to TTCrx

Bits 0-7

This 8-bit field contains data to be written to the TTCrx chip.

TTC Register Number

Bits 8-12

Specify the TTCrx register number to be read or written

Write

Bit 13

When set to 1, defines the operation as a write to TTCrx. When set to 0, the operation is a read.

Reset TTCrx Controller

Bit 15

When set to 1, resets the TTC controller logic and aborts any I2C operation in progress.

The TTC registers and offsets are listed in Table 3. All registers are 8 bits wide.

Offset	Name	Function
0	FineDelay1	Deskew clock 1 delay, in steps of 104 ps from 0 to 25 μs.
2	FineDelay2	Deskew clock 2 delay, in steps of 104 ps from 0 to 25 μs.
4	CoarseDelay	Bits <3:0>: Tick delay to bunch counter reset Bits <7:4>: Tick delay to user broadcast commands
6	Control	Access to the TTCrx control register
8	SingleErrLow	Low 8 bits of the single-bit error counter
A	SingleErrHigh	High 8 bits of the single-bit error counter
C	DoubleErr	Low 8 bits of the double-bit error counter
E	SEUErr	Error count register.
10	IDLow	Bits <7:0> of the TTCrx address.
12	IDHigh	Bits <13:8> of the TTCrx address and mastermode A bits <1:0>.
14	I2CID	Bits <6:0> of the I2C Bus address and mastermode B bits <1:0>.
16	Config1,	Configuration register
18	Config2,	Configuration register 2
1A	Config3	Configuration register 3.
1C	Status	Receiver status register
1E	BC Low	Bits <7:0> of the 16-bit bunch counter.
20	BC High	Bits <15:8> of the 16-bit bunch counter.
22	EvCountLow	Bits <7:0> of the 24-bit event counter.
24	EvCountMid	Bits <15:8> of the 24-bit event counter.
26	EvCountHigh	Bits <23:16> of the 24-bit event counter.

Table 3: TTCrx ASIC internal registers

5.8.4.30 TTCrx Status Register

All bit fields are outputs from card. Power-up condition initially sets all bits to 0.

Bit	Descriptive Name	Signal name
0-7	*Data from TTCrx*	*TTCRDATA*
8-12	*Unused*	
13	*I2C Busy*	*I2CBUSY*
14	*I2C Error*	*I2CERR*
15	*Unused*	

Data from TTCrx
Bits 0-7
This 8-bit field contains data read from the TTCrx chip.

I2C Busy
Bit 8
When set to 1, indicates that an I2C transaction is underway

I2C Error
Bits 9
When set to 1, indicates that an I2C error has occurred

5.8.4.31 Crate FPGA firmware version

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0-1	*FPGA Firmware Type*	*Ftype*
2-3	*FPGA Firmware Level*	
4-7	*null*	
8-15	*FPGA Code Revision*	

FPGA Firmware type
Bits 0-1
This 2-bit field contains the FPGA firmware type, i.e. the type of data being summed:

Bitfield 0-1 Value	Module Function
0	CP summing
1	Jet Summing
2	Energy Summing
3	Reserved

FPGA Firmware level
Bits 2-3
This 2-bit field contains the FPGA firmware level, i.e. crate or system-level summing:

Bitfield 2-3 Value	Summing Level
0	Crate summing
1	System Summing
2-3	Reserved

FPGA Code Revision
Bit 8-15
This 8-bit field contains the crate FPGA code version number. The first version is numbered 1.

5.8.4.32 System FPGA firmware version

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0-1	*FPGA Firmware type*	*Ftype*
2-3	*FPGA Firmware level*	
4-7	*null*	
8-15	*FPGA Code Revision*	

FPGA Firmware type
Bits 0-1
This 2-bit field contains the FPGA Firmware type (as defined in section 5.8.4.31 above)

FPGA Firmware level
Bits 2-3
This 2-bit field contains the FPGA Firmware level (as defined in section 5.8.4.31 above)

FPGA Code Revision
Bit 8-15
This 8-bit field contains the system FPGA code version number. The first version is numbered 1.

5.8.4.33 I2C FPGA firmware version

This register contains the version number of the I2C FPGA controlling the TTCrx chip. This is a 16-bit value. The first version is number 1.

5.8.4.34 VME CPLD firmware version

This register contains the version number of the FPGA providing the interface to VME¨. This is a 16-bit value; the first version is number 1.

5.8.4.35 System Ace VME Interface

This register is reserved for VME control of the System Ace device.

5.8.4.36 CAN Access Register A

Two registers providing access to the microprocessor controlling the CAN bus.

5.8.4.37 CAN Access Register B

Bit	Descriptive Name	Signal name
0 - 3	*Can Interrupt Request*	*CAN_IRQ[0:3]*
4-15	*null*	

CAN Interrupt Request

Bits 0-3

Writing a 1 to one of these bits causes an interrupt request to the CANBus processor at the corresponding priority. Writing a zero has no effect. These bits always read as zero.

5.8.4.38 Sum-E_T Threshold 1

Bits 0-15

This register contains the 16-bit threshold for Sum-E_T hit 1.

5.8.4.39 Sum-E_T Threshold 2

Bits 0-15

This register contains the 16-bit threshold for Sum-E_T hit 2.

5.8.4.40 Sum-E_T Threshold 3

This register contains the 16-bit threshold for Sum-E_T hit 3.

5.8.4.41 Sum-E_T Threshold 4

Bits 0-15

This register contains the 16-bit threshold for Sum-E_T hit 4.

5.8.4.42 Jet-E_T Threshold 1

Bits 0-15

This register contains the 16-bit threshold for Jet-E_T hit 1.

5.8.4.43 Jet-E_T Threshold 2

Bits 0-15

This register contains the 16-bit threshold for Jet-E_T hit 2.

5.8.4.44 Jet-E_T Threshold 3

This register contains the 16-bit threshold for Jet-E_T hit 3.

5.8.4.45 Jet-E_T Threshold 4

Bits 0-15

This register contains the 16-bit threshold for Jet-E_T hit 4.

5.8.4.46 Module Rate Counters

This bank of addresses contains sixteen 32-bit module rate meter counters. For each counter, the 16 LSBs appear first, followed by the 16 MSBs at the next 16-bit address. Thus counter zero has 16 LSBs at address 0x1600C0 and 16 MSBs at 0x1600C2.

5.8.4.47 Crate Rate Counters

This bank of addresses contains four 32-bit crate rate counters, mapped in the same way as the module rate counters.

5.8.4.48 System Rate Counters

This bank of addresses contains the twelve 32-bit System rate counters, mapped in the same way as the module rate counters.

5.8.4.49 Normalisation Rate Counter

This register contains the normalisation rate counter, mapped with the 16 LSBs at the specified address, and the 16 MSBs at the next higher address.

5.8.4.50 Module Rate Mask Register

This register contains the module rate threshold mask. Hits for thresholds are ignored if the corresponding bit is set to one. Bits 0-7 are used in the CP subsystem and bits 0-11 in the Jet subsystem. The register is not used in the Energy subsystem.

5.8.4.51 Crate Rate Mask Register

This register contains the crate rate threshold mask. Hits for thresholds are ignored if the corresponding bit is set to one. Bits 0-7 are used in the CP subsystem and bits 0-11 in the Jet subsystem. The register is not used in the Energy subsystem.

5.8.4.52 TtcI2cId Register

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0-5	*TTCrx I2C ID*	*TtcI2cId*
6-15	*Unused*	

TtcI2cId
Bits 0-5
This register contains the TTC base ID used by the I2C FPGA to communicate with the TTCrx, which is set up as the module resets. It matches the content of the TTCrx base address register I2C_ID (0:5), and should always contain the value 4.

5.8.4.53 TtcBrcst Register

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0-1	*Null*	
2-5	*TTC BRCST data (2: 5)*	*TTCBRCST (2: 5)*
6-7	*TTC BRCST data (6:7)*	*TTCBRCST (6: 7)*
8-15	*Unused*	

null
Bits 0-1
These bits read as zero.

TTC BRCST data (2:5)
Bits 2-5
The most recent value of BRCST data bits (2:5) output from the TTCrx (that were qualified by the TTC strobe BRCSTSTR1).

TTC BRCST data (6:7)
Bits 6-7
The most recent value of BRCST data bits (6:7) output from the TTCrx (that were qualified by the TTC strobe BRCSTSTR2).

5.8.4.54 TTC DQ Register

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0-3	*TTC DQ*	*TTCDQ*
4-15	*Unused*	

TTC DQ
Bits 0-3
The most recent DQ value output from the TTCrx (that was qualified by the TTC strobe DOUTSTR).

5.8.4.55 TTC Dump RAM

All bit fields are outputs from card.

Bit	Descriptive Name	Signal name
0-7	*TTC Dump Data*	*TTCDump*
8-15	*Unused*	

TTC Dump Data
Bits 0-7
A block of RAM 16 words deep that captures data from TTC Error and Configuration Dumps. Data from the TTC are mapped to the RAM using DQ as the address.

5.8.4.56 DPR Access: Crate FPGA Input Data

This address space is mapped to the scrolling dual-port RAM within the Crate FPGA that records the input data received from the CPMs or JEMs. The data consist of 16 groups of 256 25-bit values, organised as shown below. In CP versions of the CMM only channels 1-14 contain nonzero data.

Byte Offset (Hex)	Contents
0 - 1FE	256 16-bit words, data for channel 0 bits <0:15>
200 - 3FE	256 16-bit words, data for channel 0 bits <16:25>
400 - 7FE	Data for channel 1
…	…
3C00 - 3FFE	Data for channel 15

Bit 25 of the data for each channel contain the parity error flag resulting from the check of the corresponding incoming data. The error bits are set to 0 if there was no parity error.

5.8.4.57 DPR Access: Crate FPGA Output Data

This address space is mapped to the scrolling dual-port RAM within the Crate FPGA that records the data output from that device. The format of these data varies between CMM firmware versions. They are organised as follows:

Byte Offset (Hex)	Contents, CP CMM	Contents, Energy-Sum CMM	Contents, Jet-Counting CMM
0 - 1FE	256 16-bit words, data bits <0:15>	256 16-bit words of E_X data	256 16-bit words of main jet data <0:15>
200 - 3FE	256 16-bit words, data bits <16:23>	256 16-bit words, E_Y	256 16-bit words, main jet data <16:23>
400 - 5FE	*Unused*	256 16-bit words, E_T	256 16-bit words, forward jet data

These data are local to the module, so there are no parity indicators.

5.8.4.58 DPR Access: System FPGA Input Data

This address space is mapped to the scrolling dual-port RAM within the System FPGA that records the input data received from remote CMMs.(Data from the local Crate FPGA are recorded there before transmission and are not re-recorded here). The format of these data varies between CMM versions. They are organised as follows:

Byte Offset (Hex)	Contents, CP CMM	Contents, Energy-Sum CMM	Contents, Jet-Counting CMM
0 - 1FE	256 16-bit words of data from remote CMM 1, bits <0:15>	256 16-bit words of E_X <0:15> data from remote CMM	256 16-bit words, main jet data <0:15> from remote CMM
200 - 3FE	256 16-bit words, remote CMM 1 <16:25>	256 16-bit words, E_Y <0:15>	256 16-bit words, bits 0:8 = main jet<16:24>
400 - 5FE	remote CMM 2, bits <0:15>	256 16-bit words, bit 0 = E_X <16>, bit 1 = E_Y <16>	256 16-bit words, forward jet data<0:15>
600 - 7FE	remote CMM 2, bits <16:24>	256 16-bit words, E_T<0:15>	256 16-bit words, bit 0 = f/wd jet<16>
800 - 9FE	remote CMM 3, bits <0:15>	*RAM not present*	*RAM not present*
A00 - BFE	remote CMM 3, bits <16:24>	*RAM not present*	*RAM not present*

The data for each cable contain a parity error flag resulting from the check of the corresponding incoming data, on the following bit numbers: CP-CMM: bit 24; E_X and E_Y: bit 16; E_T: bit 15; main jets: bit 24; forward jets: bit 16.

5.8.4.59 DPR Access: System FPGA Output Data

This address space is mapped to the scrolling dual-port RAM within the System FPGA that records the output data. The format of the data is as follows:

Byte Offset (Hex)	Contents, CP CMM	Contents, Energy-Sum CMM	Contents, Jet-Counting CMM
0 - 1FE	256 16-bit words of CP data <0:15>	256 16-bit words, E_X <0:15>	256 16-bit words, main jet counts <0:15>
200 - 3FE	256 16-bit words of CP data <16:24>	256 16-bit words, E_Y <0:15>	256 16-bit words, main jet counts <16:23>
400 - 5FE	*RAM not present*	256 16-bit words, bit 0 = E_X <16>, bit 1 = E_Y <16> bits 4:7 = $E_T$hits, bits 8:15 = E_T^{MISS} hits	256 16-bit words, forward jet counts L and R
600 - 7FE	*RAM not present*	256 16-bit words, Sum-E_T <0:15>	256 16-bit words, 4-bit Jet E_T hits <0:3>

5.8.4.60 FIFO Access: Crate FPGA Input Data

This address space is mapped to the FIFO within the Crate FPGA DAQ logic that buffers the input data. The data in this FIFO are organised identically to the data in the Crate FPGA Input DPR (see 5.8.4.56).

5.8.4.61 FIFO Access: Crate FPGA Output

This address space is mapped to the FIFO within the Crate FPGA DAQ logic that buffers the output data. The data in this FIFO are organised identically to the data in the Crate FPGA Output DPR (see 5.8.4.57).

5.8.4.62 FIFO Access: Sys FPGA Input Data

This address space is mapped to the FIFO within the System FPGA DAQ logic that buffers the input data. The data in this FIFO are organised identically to the data in the System FPGA Input DPR (see 5.8.4.58).

5.8.4.63 FIFO Access: Sys FPGA Output Data

This address space is mapped to the FIFO within the System FPGA DAQ logic that buffers the output data. The data in this FIFO are organised identically to the data in the System FPGA Output DPR (see 5.8.4.59).

5.8.4.64 DPR Access: RoI Data

This address space is mapped to the scrolling dual-port RAM within the System FPGA that records the RoI data. The format of the data is as follows:

Byte Offset (Hex)	Contents, CP CMM	Contents, Energy-Sum CMM	Contents, Jet-Counting CMM
0 - 1FE	*RAM not present*	256 16-bit words, E_X <0:15>	256 16-bit words of Jet E_T hits
200 – 3FE	*RAM not present*	256 16-bit words, E_Y <0:15>	*unused*
400 – 5FE	*RAM not present*	256 16-bit words, bit 0 = E_X <16>, bit 1 = E_Y <16> bits 4:7 = $E_T$hits, bits 8:15 = E_T^{MISS} hits	*RAM not present*
600 – 7FE	*RAM not present*	256 16-bit words, E_T	*RAM not present*

5.8.4.65 FIFO Access: RoI Data

This address space is mapped to the FIFO within the System FPGA that buffers the RoI data. The format of the data is identical to that in the RoI DPR (see 5.8.4.64 above).

5.8.4.66 Main Jet-ET LUT

This address space is mapped to the LUT within the System FPGA that converts main Jet hit counts to energies before thresholds are applied. The lower and upper bytes of each 16-bit word access the LUTs for jet thresholds 1-4 and 5-8 respectively

5.8.4.67 Forward Jet-ET LUT

This address space is mapped to the LUT within the System FPGA that converts forward Jet hit counts to energies before thresholds are applied. .The lower byte of each 16-bit word accesses the LUTs. The upper byte is ignored on write and reads back as zero.

5.8.4.68 Missing-ET LUT

This address space is mapped to the LUT within the System FPGA that converts missing-ET values to hits (see Figure 20). The lower 4096 (x2000) locations map LUT 0 (the lowest energy range) to the low byte and LUT 1 to the high byte. The higher 4096 locations map LUT 2 to the low byte and LUT 3 to the high byte, as follows:

Byte Offset	VME bits 8-15	VME bits 0-7
0x0 - 0x1FFE	LUT 1	LUT 0 (low energy)
0x2000 - 0x3FFE	LUT 3	LUT 2

5.9 Connector Definitions.

These are as defined for merger module positions in the common backplane specification.

5.10 Manufacturing

An outside manufacturer will carry out PCB manufacture and assembly. The module requires a 12-layer PCB, with Nickel-Gold finish and 60 ohm track impedances. The large FPGAs have 1.00 mm BGA pitch, the overall module having approximately 4000 nets.

5.11 Testing

5.11.1 Test Strategy

Testing is done in stages:

1. Test the CMM internal data transfer using LabView environment
2. System tests with software provided by the customer in the customer's environment

A test plan is provided at the PRR stage

5.11.2 Test equipment

(1) Powered 9U crate with custom backplane
(2) A24 D16 VME interface
(3) Computer to run software
(4) Data Source and Sink modules
(5) Logic analyser
(6) Oscilloscope
(7) TTC system (TTCvi, TTCvx, TTCrx)
(8) VME Extender

5.11.3 Software

A test engineer from the System Support Group will develop the LabView test software.

The test software for other tests is required from the customer.

5.12 Installation

The CMM module is designed for a 9U crate with a reduced VME backplane. The module is provided with a front panel containing sockets and monitoring LEDs. The module must be single-width to meet space constraints.

5.13 Maintenance and further orders

This is a prototype module built to full production specifications. Production modules have an expected life span of up to 20 years. A total of 21 production merger modules are required (see section 3).

6 Project Management

6.1 Personnel

		RAL Ext.	RAL Location
Customer:	C. N. P. Gee	6244	R1, 1.39
Project Manager:	V. Perera	5692	R68, 2.31
Project Engineer	I.P.Brawn	6816	R68, 2.23

6.2 Deliverables

6.2.1 To the Customer:

1. Initially two pre-production modules, and following acceptance 18 more production CMM Modules, with firmware needed to operate the module for crate- and system-summing in Cluster Processing crates. Firmware for jet hit counting and energy summing will be developed by the Stockholm and Mainz groups, based on the cluster crate summing code developed at RAL, with appropriate agreements to protect IPR where necessary.
2. Test Plan

6.2.2 From the Customer:

Specification document in MS Word format, Test Software, Powered crate with custom backplane and a software platform to allow the test software to drive the CMM Module.

6.3 Firmware Responsibilities

Master versions of the CP and Energy-summing firmware are held at RAL with the module hardware designs, in a Unix server system which is backed-up every night. Firmware versions, problem reports and updates are listed on the RAL ESDG web and conform to the RAL ISO 9000 QA system. An evaluation is underway of a tool for firmware version management. All designs will be moved to a common repository if or when agreement is reached.

Responsibility for the firmware components is as follows:

6.3.1 CP hit counting:

This is wholly the responsibility of RAL, together with all firmware in the module outside the crate and system FPGAs for all module versions. RAL is also responsible for module hardware diagnostic firmware.

6.3.2 Jet hit counting:

RAL is responsible for support of all logic common to CP f/ware.

Stockholm is responsible for support of the algorithm block, top-level integration of design, and subsystem hardware tests.

6.3.3 Energy Summing:

RAL is responsible for supporting all logic except algorithm block, and for top-level integration of the design.

Mainz is responsible for support of the algorithm block and subsystem hardware tests.

6.4 Project plan (Milestones)

1.PDR	11-Dec-2000
2.PDR Signed off	4-May-2001
3. Start Testing	31-Aug-2002.
4. FDR	20-Sep-2004
4. PRR	28-Feb-2005

6.5 Design Reviews

The progress of the project is reported on a monthly basis in the ATLAS Calorimeter First-level Trigger project monitor form.

6.6 Training

Training is carried out as required on the job.

6.7 CAE

Cadence for schematic capture, VHDL and FPGA design tools, and LabView for test software.

6.8 Costs and finance (Cost centre: FK42200)

6.8.1 Cost Estimate

£91,000 for 20 modules.

6.9 Intellectual Property Rights (IPR) and Confidentiality

All background and foreground Intellectual Property Rights in this project remain with CCLRC. The customer has unrestricted rights to items listed under deliverables (6.2). If the customer requires other data, then an appropriate protective agreement should be in place before releasing such data.

6.10 Safety

General laboratory safety codes apply.

6.11 Environmental impact

6.11.1 Disposal

RAL will dispose of the modules at end of their life.

6.11.2 EMC

The electronics shall comply with specifications intended to ensure operation without malfunction or unacceptable degradation of performance due to electromagnetic interference (EMI) within their intended operational environment.

7 Glossary

CMM	Common Merger Module (specified in this document)
backplane	High-speed custom backplane within CP and JEP crates
Processor module	Refers to either the CPM or JEM (see below)
CPM	Cluster Processor Module
JEM	Jet/Energy Module
CP	Cluster Processor sub-system of the Calorimeter Trigger
JEP	Jet/Energy Processor sub-system of the Calorimeter Trigger
TCM	Timing and Control Module
TTC	Timing, Trigger and Control
DCS	Detector Control System
ROD	Readout Driver module
L1A	Level-1 Accept signal distributed via the TTC system.
RoI	Region-of-Interest
$\mathbf{E_T}$	Transverse Energy
$\mathbf{E_X}$, $\mathbf{E_Y}$	X and Y components of the transverse energy
BC	12-bit LHC bunch crossing number
LVDS	Low-Voltage Differential Signalling

8 Revision History

8.1 Changes in Draft 0.2

Added Controller Control and Status, and FIFO Write and Read registers for system flash and crate flash memories.
Added TTC Broadcast data register, TTC DQ register, and TTC Dump ram register.
Distinguish between crate-level and system-level merging.
Use compressed energy scale throughout.
Clarify the energy summing process
Define parity scheme.
Define all output data formats
Separate timing controls for each cable and backplane link.
Control bit enabling playback mode.
Add register to set local pipeline delay

8.2 Changes in Draft 3:

Energy summation using linear energy scale between CMMs.
Energy readout format adapted to agree with above.
All registers limited to 16-bit width.
Diagram added of inter-CMM cabling, connector use clarified
Included Backplane spec of CMM Station.

8.3 Changes in Version Draft 0.9

Definition of Jet-Energy estimator algorithm
Backplane timing structure and module timing structure included.
Uniform terminology for main and forward jets.
Corrections and improvements to Slice and RoI data formats.
Approximate module layout included

8.4 Changes in Version Draft 0.95

Figure 11 and section 3.3.10.2 modified to include readout of 4 Jet ET hits on bit D16.
RoI format of Jet ET hits defined in paragraph 3.3.11.
Appendix 2 updated to backplane 0.9b2
Adapter board details in 5.2.2.2 and Figure 14 changed for backplane 0.9b2
TTCrx register access simplified to match CPM in section 5.3.4.16 & 5.3.4.17
Inter-CMM cables are grounded via network on adapter board, not CMM. Fig 18.
L1A and G-Link test points specified in section 5.6.1.

8.5 Changes in Version 1.0

Revised review dates
Missing characters and type problems fixed in figures 10 and 11.
Additional Power LEDs defined
New transition module board drawing from V. Perera
Registers added for FPGA and CPLD code version numbers
Registers added for DAQ and ROI slice offsets and FIFO address counters.

8.6 Changes in Version 1.1

Number of missing-ET thresholds corrected from four to eight in text and figure 8.

Front-panel connectors defined to be SCSI-3
Control Pulse register bits added.
Can access registers defined.
Single address space used for accessing System and Crate FPGA RAMs.
Register names adjusted to match software capitalisation, and spaces removed.

8.7 Changes in Version 1.2

Backplane connections confirmed to backplane spec v 1.0 and title updated.
Appendix B added with front panel and rear transition module pinout for CP firmware.
Definitions of VME access to FPGA dual-port memories and FIFOs added.
Added pinout details of all backplane input and output connectors.
Added mode bits to control mode register
Defined contents of CAN registers
Added details of crate and system energy summing.

8.8 Changes in Version 1.3

Changes to base addresses in programming model.
Update register map: add Jet-E_T threshold registers and RoI Dual-Port Ram and FIFO access.
Add labels for front-panel LEDs.
Update cabling diagrams to move grounded pairs to high-order bits, and to renumber thresholds to start from zero.
Change references to Jet-Energy to refer to Jet-E_T.
Re-insert Flash controls and TTC FPGA Controls
Add TTC Enable bit in Mode control register
Detail on parity and BCN bits in Crate FPGA input DPR

8.9 Changes in Version 1.3.1

CP and JEP backplane slot numbering both using physical slot numbering 0-15. Minor changes to documentation for registers: Backplane parity, backplane Timing Select A & B, DPR access Crate FPGA input data.

8.10 Changes in Version 1.3.2

Added control pulse register bits to reload Crate and System-summing FPGAs.
Corrected wrong incoming module numbers in Fig 5 (JetHitCrate).
Jet-E_T G-Link output changed to use identical format to Jet slice readout.

8.11 Changes in Version 1.3.3

Corrected name of Et threshold and LUT registers (previously named Jet-E …)
Added description of Energy summing and figure
Corrected definition of Crate numbers and functions (table 1)

8.12 Changes in Version 1.4

Corrected Cabling between CMM Crate and System modules (Figure 23).
Defined ordering of channel disable, replay, and parity check algorithms in 3.3.10

8.13 Changes in Version 1.4.1

Inserted registers for Jet-ET thresholds. Mapped Jet-ET LUTs.
Changed access to Missing ET LUT to provide full mapped access.

Doubled width of ET LUT output to 8 bits.

8.14 Changes in Version 1.4.2

Move FPGA Firmware type field from ModuleIdB to Crate FPGA version no and System FPGA version no registers.
Correct TtcI2cId register to read-only. Documented internal TTCrx registers
Update behaviour of backplane disable register to note recording of zeros (with parity correct) in input memories.
Documented DAV Gap in DAQ readout.
Documented TTC synchronize command in new section 3.3.9.
Introduced connector tables, front and rear connectors for Jet and Energy firmware.

8.15 Changes in Version 1.4.3

Update TTC Registers to bit ordering to match (updated) CPM

8.16 Changes in Version 1.4.4

Correct Figure 2 (remove extra readout line) and 3 (connect 50-pin input).
Added figure to describe signs of energy firmware
Corrections to adopt energy hit maps in figure 8,16,17 and sec 3.3.6.3.
Updated figures for Jet and Energy G-link data
Update DRPCrateIn FPGA 5.7.4.59, no BC Number, and added parity error indicator
Missing ET LUT description – added figure reference
Added outline of jet ET sums in section 3.6
Numbering consistency check, JEMs numbered 0-15
EtMiss Output bit width set to 8 bits in readout format.

8.17 Changes in Version 1.5

Fixed version for FDR

8.18 Changes in Version 1.6

Minor text clarifications as requested at FDR.
Clarify that all negative numbers are two's complement.
Specify 3M connectors to replace SCSI-3 connectors.
Split FIFO overflow into a FO and RFO bit. Change Clear Parity Error pulse to Clear Error. Add extra text to describe G-Link readout
Add description of I2C interface (Ian Brawn)
Add description of CANBus interface and functions (from Adam Davis)
Correct pinout of CMM-CTP connectors to match CTP_IN spec (parity, clock on pins 32, 33). Exchange polarity of signal pins. Use 3M connector and CERN halogen free cable.
Adjust RTM pinout and polarity to match front panel connectors.
Removed previous flash memory control registers

8.19 Changes in Version 1.7

Released for PRR
Minor text updates from FDR

8.20 Changes in Version 1.7.1

Minor text updates. Remove references to prototype modules; remove optional backplane signalling voltages not used; correct total numbers of modules needed; update glossary;

Specify identical FPGA devices for Crate and System-level summing

8.21 Changes in Version 1.7.2

Clarify placing of parity bits in DprSysFPGAInput. Move forward jet parity indicator from bank at 200 to bank at 600.
Change Parity Count Register to read only (always has been read-only in the actual firmware, and was intended to be so).

8.22 Changes in Version 1.7.3

Test clarification, System FPGA output data.

8.23 Changes in Version 1.7.4

Test corrections to clarify use of twos-complement arithmetic for energies.

8.24 Changes in version 1.7.5

Reference text converted to blue!!

8.25 Changes in version 1.7.6

Front panel labels for LEDs changes in module version 3.

8.26 Changes in version 1.7.7

Correct Table 1 to put tau CMMs on LHS of crate, e-gamma on right, to match CPM.

8.27 Changes in version 1.7.8

Updated connector numbers and signal names in pinouts in appendices B-E

8.28 Changes in Version 1.7.9

Added laser disable bits and TTC protection control bit to control mode register.
Added Crate Data Parity Error bit to Cable Link Parity Error register.

8.29 Changes in Version 1.7.10

Change Missing-ET Algorithm to use the four lowest groups of 6 bits to select ET Range.
Added rate metering function.

8.30 Changes in Version 1.8

Added rate metering function

Appendix A CMM backplane connector layout (Version 1.0)

Pos.	A	B	C	D	E

Guide Pin (0-8mm) (AMP parts 223956-1, 223957-1, or equivalent)

Connector 1 (8-46mm) Type B-19 connector (short through-pins)

1		<G>	VMED00	VMED08	VMED09
2		VMED01	VMED02	VMED10	VMED11
3		<G>	VMED03	VMED12	VMED13
4		VMED04	VMED05	VMED14	VMED15
5		<G>	VMED06	VMEA23	VMEA22
6		VMED07	<G>	VMEA21	VMEA20
7		<G>	VMEDS0*	<G>	<G>
8		VMEWRITE*	<G>	VMEA18	VMEA19
9		<G>	VMEDTACK*	VMEA16	VMEA17
10	<G>	VMEA07	VMEA06	VMEA14	VMEA15
11	P0_0	<G>	VMEA05	VMEA12	VMEA13
12	P0_1	VMEA04	VMEA03	VMEA10	VMEA11
13	P0_2	<G>	VMEA02	VMEA08	VMEA09
14	P0_3	VMERESET*	VMEA01	<G>	<G>
15	P0_4	P1_0	<G>	P2_0	P3_0
16	P0_5	<G>	P1_1	P2_1	P3_1
17	P0_6	P1_2	P2_2	<G>	P3_2
18	P0_7	<G>	P1_3	P2_3	P3_3
19	P0_8	P1_4	P2_4	<G>	P3_4

Connector 2 (46-84mm) Type B-19 connector (short through pins)

1	P0_9	<G>	P1_5	P2_5	P3_5
2	P0_10	P1_6	P2_6	<G>	P3_6
3	P0_11	<G>	P1_7	P2_7	P3_7
4	P0_12	P1_8	P2_8	<G>	P3_8
5	P0_13	<G>	P1_9	P2_9	P3_9
6	P0_14	P1_10	P2_10	<G>	P3_10
7	P0_15	<G>	P1_11	P2_11	P3_11
8	P0_16	P1_12	P2_12	<G>	P3_12
9	P0_17	<G>	P1_13	P2_13	P3_13
10	P0_18	P1_14	P2_14	<G>	P3_14
11	P0_19	<G>	P1_15	P2_15	P3_15
12	P0_20	P1_16	P2_16	<G>	P3_16
13	P0_21	<G>	P1_17	P2_17	P3_17
14	P0_22	P1_18	P2_18	<G>	P3_18
15	P0_23	<G>	P1_19	P2_19	P3_19
16	P0_24	P1_20	P2_20	<G>	P3_20
17	GEOADD5	P1_21	GEOADD4	P2_21	P3_21
18	GEOADD6	P1_22	P2_22	<G>	P3_22
19	GEOADD0	<G>	P1_23	P2_23	P3_23

Connector 3 (84-122mm) Type B-19 connector (short through pins)

1	P4_0	P1_24	P2_24	<G>	P3_24
2	P4_1	<G>	P5_0	P6_0	P7_0
3	P4_2	P5_1	P6_1	<G>	P7_1
4	P4_3	<G>	P5_2	P6_2	P7_2
5	P4_4	P5_3	P6_3	<G>	P7_3
6	P4_5	<G>	P5_4	P6_4	P7_4
7	P4_6	P5_5	P6_5	<G>	P7_5
8	P4_7	<G>	P5_6	P6_6	P7_6
9	P4_8	P5_7	P6_7	<G>	P7_7
10	P4_9	<G>	P5_8	P6_8	P7_8
11	P4_10	P5_9	P6_9	<G>	P7_9
12	P4_11	<G>	P5_10	P6_10	P7_10
13	P4_12	P5_11	P6_11	<G>	P7_11
14	P4_13	<G>	P5_12	P6_12	P7_12
15	P4_14	P5_13	P6_13	<G>	P7_13
16	P4_15	<G>	P5_14	P6_14	P7_14
17	P4_16	P5_15	P6_15	<G>	P7_15
18	P4_17	<G>	P5_16	P6_16	P7_16
19	P4_18	P5_17	P6_17	<G>	P7_17

Connector 4 (122-160mm) Type B-19 connector (long through pins)

1	P4_19	<G>	P5_18	P6_18	P7_18
2	P4_20	P5_19	P6_19	<G>	P7_19
3	P4_21	<G>	P5_20	P6_20	P7_20
4	P4_22	P5_21	P6_21	<G>	P7_21
5	P4_23	<G>	P5_22	P6_22	P7_22
6	P4_24	P5_23	P6_23	<G>	P7_23
7	<G>	<G>	P5_24	P6_24	P7_24
8	M_00+	M_01+	M_02+	M_03+	M_04+
9	M_00-	M_01-	M_02-	M_03-	M_04-
10	M_05+	M_06+	M_07+	<CG>	M_08+
11	M_05-	M_06-	M_07-	<CG>	M_08-
12	M_09+	M_10+	M_11+	M_12+	M_13+
13	M_09-	M_10-	M_11-	M_12-	M_13-
14	M_14+	<CG>	M_15+	M_16+	M_17+
15	M_14-	<CG>	M_15-	M_16-	M_17-
16	M_18+	M_19+	M_20+	M_21+	M_22+
17	**M_18-**	M_19-	M_20-	M_21-	M_22-
18	M_23+	M_24+	M_25+	<CG>	M_26+
19	M_23-	M_24-	M_25-	<CG>	M_26-

Connector 5 (160-210mm) Type B-25 connector (long through pins)

1	M_27+	M_28+	M_29+	M_30+	M_31+
2	M_27-	M_28-	M_29-	M_30-	M_31-
3	M_32+	<CG>	M_33+	M_34+	M_35+
4	M_32-	<CG>	M_33-	M_34-	M_35-
5	M_36+	M_37+	M_38+	M_39+	M_40+
6	M_36-	M_37-	M_38-	M_39-	M_40-
7	M_41+	M_42+	M_43+	<CG>	M_44+
8	M_41-	M_42-	M_43-	<CG>	M_44-
9	M_45+	M_46+	M_47+	M_48+	M_49+
10	M_45-	M_46-	M_47-	M_48-	M_49-
11	M_50+	M_51+	<CG>	M_52+	M_53+
12	M_50-	M_51-	<CG>	M_52-	M_53-
13	<G>	M_54+	M_55+	M_56+	M_57+
14	P8_0	M_54-	M_55-	M_56-	M_57-
15	P8_1	<G>	<CG>	M_59+	M_60+
16	P8_2	M_58+	<CG>	M_59-	M_60-
17	P8_3	M_58-	M_61+	M_62+	M_63+
18	P8_4	<G>	M_61-	M_62-	M_63-
19	P8_5	M_64+	M_65+	<CG>	M_66+
20	P8_6	M_64-	M_65-	**M_68+**	M_66-
21	P8_7	<G>	M_67+	**M_68-**	M_69+
22	P8_8	<G>	M_67-	**M_71+**	M_69-
23	P8_9	P9_0	M_70+	**M_71-**	M_72+
24	P8_10	P9_1	M_70-	**M_73+**	M_72-
25	P8_11	P9_2	<G>	**M_73-**	M_74+

Connector 6 (210-248mm) Type B-19 connector (long through pins)

1	P8_12	<G>	P9_3	**M_75+**	M_74-
2	P8_13	P9_4	<G>	**M_75-**	<CG>
3	P8_14	<G>	P9_5	**M_76+**	<CG>
4	P8_15	P9_6	<G>	**M_76-**	M_77+
5	P8_16	<G>	P9_7	**<G>**	M_77-
6	P8_17	P9_8	<G>	**P10_0**	M_78+
7	P8_18	<G>	P9_9	P10_1	M_78-
8	P8_19	P9_10	<G>	P10_2	<CG>
9	P8_20	<G>	P9_11	P10_3	M_79+
10	P8_21	P9_12	P10_4	<G>	M_79-
11	P8_22	<G>	P9_13	P10_5	M_80+
12	P8_23	P9_14	P10_6	<G>	M_80-
13	P8_24	<G>	P9_15	P10_7	<G>
14	M_81+	P9_16	P10_8	<G>	P11_0
15	M_81-	<G>	P9_17	P10_9	P11_1
16	M_82+	P9_18	P10_10	<G>	P11_2
17	M_82-	<G>	P9_19	P10_11	P11_3
18	M_83+	P9_20	P10_12	<G>	P11_4
19	M_83-	<G>	P9_21	P10_13	P11_5

Connector 7 (248-286mm) Type B-19 connector (short through pins)

1	<G>	P9_22	<G>	P10_14	P11_6
2	<G>	P9_23	P10_15	<G>	P11_7
3		P9_24	<G>	P10_16	P11_8
4			P10_17	<G>	P11_9
5			<G>	P10_18	P11_10
6			P10_19	<G>	P11_11
7			<G>	P10_20	P11_12
8			P10_21	<G>	P11_13
9	<G>	<G>	<G>	P10_22	P11_14
10	P12_0	P13_0	P10_23	<G>	P11_15
11	P12_1	<G>	P13_1	P10_24	P11_16
12	P12_2	P13_2	P14_0	<G>	P11_17
13	P12_3	<G>	P13_3	P14_1	P11_18
14	P12_4	P13_4	P14_2	<G>	P11_19
15	P12_5	<G>	P13_5	P14_3	P11_20
16	P12_6	P13_6	P14_4	<G>	P11_21
17	P12_7	<G>	P13_7	P14_5	P11_22
18	P12_8	P13_8	P14_6	<G>	P11_23
19	P12_9	<G>	P13_9	P14_7	P11_24

Connector 8 (286-336mm) Type B-25 connector (short through pins)

1	P12_10	P13_10	P14_8	<G>	P15_0
2	P12_11	<G>	P13_11	P14_9	P15_1
3	P12_12	P13_12	P14_10	<G>	P15_2
4	P12_13	<G>	P13_13	P14_11	P15_3
5	P12_14	P13_14	P14_12	<G>	P15_4
6	P12_15	<G>	P13_15	P14_13	P15_5
7	P12_16	P13_16	P14_14	<G>	P15_6
8	P12_17	<G>	P13_17	P14_15	P15_7
9	P12_18	P13_18	P14_16	<G>	P15_8
10	P12_19	<G>	P13_19	P14_17	P15_9
11	P12_20	P13_20	P14_18	<G>	P15_10
12	P12_21	<G>	P13_21	P14_19	P15_11
13	P12_22	P13_22	P14_20	<G>	P15_12
14	P12_23	<G>	P13_23	P14_21	P15_13
15	P12_24	P13_24	P14_22	<G>	P15_14
16			<G>	P14_23	P15_15
17			P14_24	<G>	P15_16
18					P15_17
19				<G>	P15_18
20					P15_19
21				<G>	P15_20
22					P15_21
23	<G>	<G>	<G>	<G>	P15_22
24	CAN+	<G>	TTC+	<G>	P15_23
25	CAN-	<G>	TTC-	<G>	P15_24

Connector 9 (336-361mm) Type D (N) connector

2	+3.3V
6	Power GND
10	+5.0V

Appendix B Front Panel connector layout, CP firmware.

The following tables show the connector pin-out of the front panel sockets.
Socket type 3M MDR 10268-55X3XX

Socket #1 (nearest top of module, CP firmware):

Pins	Schematic signal name	CMM output to CTP
1, 35	DOUT_CTP_0 (-, +)	hits_thr0_bit(0)
2, 36	DOUT_CTP_1 (-, +)	hits_thr0_bit(1)
3, 37	DOUT_CTP_2 (-, +)	hits_thr0_bit(2)
4, 38	DOUT_CTP_3 (-, +)	hits_thr1_bit(0)
5, 39	DOUT_CTP_4 (-, +)	hits_thr1_bit(1)
6, 40	DOUT_CTP_5 (-, +)	hits_thr1_bit(2)
7, 41	DOUT_CTP_6 (-, +)	hits_thr2_bit(0)
8, 42	DOUT_CTP_7 (-, +)	hits_thr2_bit(1)
9, 43	DOUT_CTP_8 (-, +)	hits_thr2_bit(2)
10, 44	DOUT_CTP_9 (-, +)	hits_thr3_bit(0)
11, 45	DOUT_CTP_10 (-, +)	hits_thr3_bit(1)
12, 46	DOUT_CTP_11 (-, +)	hits_thr3_bit(2)
13, 47	DOUT_CTP_12 (-, +)	hits_thr4_bit(0)
14, 48	DOUT_CTP_13 (-, +)	hits_thr4_bit(1)
15, 49	DOUT_CTP_14 (-, +)	hits_thr4_bit(2)
16, 50	DOUT_CTP_15 (-, +)	hits_thr5_bit(0)
17, 51	DOUT_CTP_16 (-, +)	hits_thr5_bit(1)
18, 52	DOUT_CTP_17 (-, +)	hits_thr5_bit(2)
19, 53	DOUT_CTP_18 (-, +)	hits_thr6_bit(0)
20, 54	DOUT_CTP_19 (-, +)	hits_thr6_bit(1)
21, 55	DOUT_CTP_20 (-, +)	hits_thr6_bit(2)
22, 56	DOUT_CTP_21 (-, +)	hits_thr7_bit(0)
23, 57	DOUT_CTP_22 (-, +)	hits_thr7_bit(1)
24, 58	DOUT_CTP_23 (-, +)	hits_thr7_bit(2)
25, 59	DOUT_CTP_24 (-, +)	Reserved
26, 60	DOUT_CTP_25 (-, +)	Reserved
27, 61	DOUT_CTP_26 (-, +)	Reserved
28, 62	DOUT_CTP_27 (-, +)	Reserved
29, 63	DOUT_CTP_28 (-, +)	Reserved
30, 64	DOUT_CTP_29 (-, +)	Reserved
31, 65	DOUT_CTP_30 (-, +)	Reserved
32, 66	DOUT_CTP_31 (-, +)	CLK
33, 67	DOUT_CTP_64 (-, +)	PARITY
34, 68	GND	GND

Pins shown as Reserved are driven to zero by the CMM, and their value is included in the parity calculation at the CTP_IN. Pins shown as GND are signal grounds as described in 5.5

Socket #2 (CP firmware)

Pins	Schematic signal name	CMM output to CTP
1, 35	DOUT_CTP_32 (-, +)	Reserved
2, 36	DOUT_CTP_33 (-, +)	Reserved
3, 37	DOUT_CTP_34 (-, +)	Reserved
4, 38	DOUT_CTP_35 (-, +)	Reserved
5, 39	DOUT_CTP_36 (-, +)	Reserved
6, 40	DOUT_CTP_37 (-, +)	Reserved
7, 41	DOUT_CTP_38 (-, +)	Reserved
8, 42	DOUT_CTP_39 (-, +)	Reserved
9, 43	DOUT_CTP_40 (-, +)	Reserved
10, 44	DOUT_CTP_41 (-, +)	Reserved
11, 45	DOUT_CTP_42 (-, +)	Reserved
12, 46	DOUT_CTP_43 (-, +)	Reserved
13, 47	DOUT_CTP_44 (-, +)	Reserved
14, 48	DOUT_CTP_45 (-, +)	Reserved
15, 49	DOUT_CTP_46 (-, +)	Reserved
16, 50	DOUT_CTP_47 (-, +)	Reserved
17, 51	DOUT_CTP_48 (-, +)	Reserved
18, 52	DOUT_CTP_49 (-, +)	Reserved
19, 53	DOUT_CTP_50 (-, +)	Reserved
20, 54	DOUT_CTP_51 (-, +)	Reserved
21, 55	DOUT_CTP_52 (-, +)	Reserved
22, 56	DOUT_CTP_53 (-, +)	Reserved
23, 57	DOUT_CTP_54 (-, +)	Reserved
24, 58	DOUT_CTP_55 (-, +)	Reserved
25, 59	DOUT_CTP_56 (-, +)	Reserved
26, 60	DOUT_CTP_57 (-, +)	Reserved
27, 61	DOUT_CTP_58 (-, +)	Reserved
28, 62	DOUT_CTP_59 (-, +)	Reserved
29, 63	DOUT_CTP_60 (-, +)	Reserved
30, 64	DOUT_CTP_61 (-, +)	Reserved
31, 65	DOUT_CTP_62 (-, +)	Reserved
32, 66	DOUT_CTP_63 (-, +)	Reserved
33, 67	DOUT_CTP_65 (-, +)	Reserved
34, 68	GND	GND

Pins shown as Reserved are driven to zero by the CMM, and their value is included in the parity calculation at the CTP_IN. Pins shown as GND are signal grounds as described in 5.5

Appendix C Front Panel connector layout, Jet firmware.

The following tables show the connector pin-out of the front panel sockets.
Socket type 3M MDR 10268-55X3XX. Note that the tables correctly show signals in order 0-31, 64, 32-64, 65 – chosen to avoid substantial module changes at a late stage.

Socket #1 (nearest top of module, Jet firmware)):

Pins	Schematic signal name	CMM output to CTP
1, 35	DOUT_CTP_0 (-, +)	hits_main_thr0_bit(0)
2, 36	DOUT_CTP_1 (-, +)	hits_main_thr0_bit(1)
3, 37	DOUT_CTP_2 (-, +)	hits_main_thr0_bit(2)
4, 38	DOUT_CTP_3 (-, +)	hits_main_thr1_bit(0)
5, 39	DOUT_CTP_4 (-, +)	hits_main_thr1_bit(1)
6, 40	DOUT_CTP_5 (-, +)	hits_main_thr1_bit(2)
7, 41	DOUT_CTP_6 (-, +)	hits_main_thr2_bit(0)
8, 42	DOUT_CTP_7 (-, +)	hits_main_thr2_bit(1)
9, 43	DOUT_CTP_8 (-, +)	hits_main_thr2_bit(2)
10, 44	DOUT_CTP_9 (-, +)	hits_main_thr3_bit(0)
11, 45	DOUT_CTP_10 (-, +)	hits_main_thr3_bit(1)
12, 46	DOUT_CTP_11 (-, +)	hits_main_thr3_bit(2)
13, 47	DOUT_CTP_12 (-, +)	hits_main_thr4_bit(0)
14, 48	DOUT_CTP_13 (-, +)	hits_main_thr4_bit(1)
15, 49	DOUT_CTP_14 (-, +)	hits_main_thr4_bit(2)
16, 50	DOUT_CTP_15 (-, +)	hits_main_thr5_bit(0)
17, 51	DOUT_CTP_16 (-, +)	hits_main_thr5_bit(1)
18, 52	DOUT_CTP_17 (-, +)	hits_main_thr5_bit(2)
19, 53	DOUT_CTP_18 (-, +)	hits_main_thr6_bit(0)
20, 54	DOUT_CTP_19 (-, +)	hits_main_thr6_bit(1)
21, 55	DOUT_CTP_20 (-, +)	hits_main_thr6_bit(2)
22, 56	DOUT_CTP_21 (-, +)	hits_main_thr7_bit(0)
23, 57	DOUT_CTP_22 (-, +)	hits_main_thr7_bit(1)
24, 58	DOUT_CTP_23 (-, +)	hits_main_thr7_bit(2)
25, 59	DOUT_CTP_24 (-, +)	hits_JetEt_bit(0)
26, 60	DOUT_CTP_25 (-, +)	hits_JetEt_bit(1)
27, 61	DOUT_CTP_26 (-, +)	hits_JetEt_bit(2)
28, 62	DOUT_CTP_27 (-, +)	hits_JetEt_bit(3)
29, 63	DOUT_CTP_28 (-, +)	Reserved
30, 64	DOUT_CTP_29 (-, +)	Reserved
31, 65	DOUT_CTP_30 (-, +)	Reserved
32, 66	DOUT_CTP_31 (-, +)	CLK
33, 67	DOUT_CTP_64 (-, +)	PARITY
34, 68	GND	GND

Pins shown as Reserved are driven to zero by the CMM, and their value is included in the parity calculation at the CTP_IN. Pins shown as GND are signal grounds as described in 5.5

Socket #2 (Jet firmware)

Pins	Schematic signal name	CMM output to CTP
1, 35	DOUT_CTP_33 (-, +)	hits_fwdL_thr0_bit(0)d
2, 36	DOUT_CTP_33 (-, +)	hits_fwdL_thr0_bit(1)
3, 37	DOUT_CTP_34 (-, +)	hits_fwdL_thr1_bit(0)d
4, 38	DOUT_CTP_35 (-, +)	hits_fwdL_thr1_bit(1)
5, 39	DOUT_CTP_36 (-, +)	hits_fwdL_thr2_bit(0)d
6, 40	DOUT_CTP_37 (-, +)	hits_fwdL_thr2_bit(1)
7, 41	DOUT_CTP_38 (-, +)	hits_fwdL_thr3_bit(0)d
8, 42	DOUT_CTP_39 (-, +)	hits_fwdL_thr3_bit(1)
9, 43	DOUT_CTP_40 (-, +)	hits_fwdR_thr0_bit(0)d
10, 44	DOUT_CTP_41 (-, +)	hits_fwdR_thr0_bit(1)
11, 45	DOUT_CTP_42 (-, +)	hits_fwdR_thr1_bit(0)d
12, 46	DOUT_CTP_43 (-, +)	hits_fwdR_thr1_bit(1)
13, 47	DOUT_CTP_44 (-, +)	hits_fwdR_thr2_bit(0)d
14, 48	DOUT_CTP_45 (-, +)	hits_fwdR_thr2_bit(1)
15, 49	DOUT_CTP_46 (-, +)	hits_fwdR_thr3_bit(0)d
16, 50	DOUT_CTP_47 (-, +)	hits_fwdR_thr3_bit(1)
17, 51	DOUT_CTP_48 (-, +)	Reserved
18, 52	DOUT_CTP_49 (-, +)	Reserved
19, 53	DOUT_CTP_50 (-, +)	Reserved
20, 54	DOUT_CTP_51 (-, +)	Reserved
21, 55	DOUT_CTP_52 (-, +)	Reserved
22, 56	DOUT_CTP_53 (-, +)	Reserved
23, 57	DOUT_CTP_54 (-, +)	Reserved
24, 58	DOUT_CTP_55 (-, +)	Reserved
25, 59	DOUT_CTP_56 (-, +)	Reserved
26, 60	DOUT_CTP_57 (-, +)	Reserved
27, 61	DOUT_CTP_58 (-, +)	Reserved
28, 62	DOUT_CTP_59 (-, +)	Reserved
29, 63	DOUT_CTP_60 (-, +)	Reserved
30, 64	DOUT_CTP_61 (-, +)	Reserved
31, 65	DOUT_CTP_62 (-, +)	Reserved
32, 66	DOUT_CTP_63 (-, +)	CLK
33, 67	DOUT_CTP_65 (-, +)	PARITY
34, 68	GND	GND

Pins shown as Reserved are driven to zero by the CMM, and their value is included in the parity calculation at the CTP_IN. Pins shown as GND are signal grounds as described in 5.5

Appendix D Front Panel connector layout, Energy firmware.

The following tables show the connector pin-out of the front panel sockets.
Socket type 3M MDR 10268-55X3XX

Socket #1 (nearest top of module, Energy firmware):

Pins	Schematic signal name	CMM output to CTP
1, 35	DOUT_CTP_0 (-, +)	hits_esum_bit(0)
2, 36	DOUT_CTP_1 (-, +)	hits_esum_bit(1)
3, 37	DOUT_CTP_2 (-, +)	hits_esum_bit(2)
4, 38	DOUT_CTP_3 (-, +)	hits_esum_bit(3)
5, 39	DOUT_CTP_4 (-, +)	hits_etmiss_bit(0)
6, 40	DOUT_CTP_5 (-, +)	hits_etmiss_bit(1)
7, 41	DOUT_CTP_6 (-, +)	hits_etmiss_bit(2)
8, 42	DOUT_CTP_7 (-, +)	hits_etmiss_bit(3)
9, 43	DOUT_CTP_8 (-, +)	hits_etmiss_bit(4)
10, 44	DOUT_CTP_9 (-, +)	hits_etmiss_bit(5)
11, 45	DOUT_CTP_10 (-, +)	hits_etmiss_bit(6)
12, 46	DOUT_CTP_11 (-, +)	hits_etmiss_bit(7)
13, 47	DOUT_CTP_12 (-, +)	Reserved
14, 48	DOUT_CTP_13 (-, +)	Reserved
15, 49	DOUT_CTP_14 (-, +)	Reserved
16, 50	DOUT_CTP_15 (-, +)	Reserved
17, 51	DOUT_CTP_16 (-, +)	Reserved
18, 52	DOUT_CTP_17 (-, +)	Reserved
19, 53	DOUT_CTP_18 (-, +)	Reserved
20, 54	DOUT_CTP_19 (-, +)	Reserved
21, 55	DOUT_CTP_20 (-, +)	Reserved
22, 56	DOUT_CTP_21 (-, +)	Reserved
23, 57	DOUT_CTP_22 (-, +)	Reserved
24, 58	DOUT_CTP_23 (-, +)	Reserved
25, 59	DOUT_CTP_24 (-, +)	Reserved
26, 60	DOUT_CTP_25 (-, +)	Reserved
27, 61	DOUT_CTP_26 (-, +)	Reserved
28, 62	DOUT_CTP_27 (-, +)	Reserved
29, 63	DOUT_CTP_28 (-, +)	Reserved
30, 64	DOUT_CTP_29 (-, +)	Reserved
31, 65	DOUT_CTP_30 (-, +)	Reserved
32, 66	DOUT_CTP_31 (-, +)	CLK
33, 67	DOUT_CTP_64 (-, +)	PARITY
34, 68	GND	GND

Pins shown as Reserved are driven to zero by the CMM, and their value is included in the parity calculation at the CTP_IN. Pins shown as GND are signal grounds as described in 5.5

Socket #2 (Energy firmware)

Pins	Schematic signal name	CMM output to CTP
1, 35	DOUT_CTP_32 (-, +)	Reserved
2, 36	DOUT_CTP_33 (-, +)	Reserved
3, 37	DOUT_CTP_34 (-, +)	Reserved
4, 38	DOUT_CTP_35 (-, +)	Reserved
5, 39	DOUT_CTP_36 (-, +)	Reserved
6, 40	DOUT_CTP_37 (-, +)	Reserved
7, 41	DOUT_CTP_38 (-, +)	Reserved
8, 42	DOUT_CTP_39 (-, +)	Reserved
9, 43	DOUT_CTP_40 (-, +)	Reserved
10, 44	DOUT_CTP_41 (-, +)	Reserved
11, 45	DOUT_CTP_42 (-, +)	Reserved
12, 46	DOUT_CTP_43 (-, +)	Reserved
13, 47	DOUT_CTP_44 (-, +)	Reserved
14, 48	DOUT_CTP_45 (-, +)	Reserved
15, 49	DOUT_CTP_46 (-, +)	Reserved
16, 50	DOUT_CTP_47 (-, +)	Reserved
17, 51	DOUT_CTP_48 (-, +)	Reserved
18, 52	DOUT_CTP_49 (-, +)	Reserved
19, 53	DOUT_CTP_50 (-, +)	Reserved
20, 54	DOUT_CTP_51 (-, +)	Reserved
21, 55	DOUT_CTP_52 (-, +)	Reserved
22, 56	DOUT_CTP_53 (-, +)	Reserved
23, 57	DOUT_CTP_54 (-, +)	Reserved
24, 58	DOUT_CTP_55 (-, +)	Reserved
25, 59	DOUT_CTP_56 (-, +)	Reserved
26, 60	DOUT_CTP_57 (-, +)	Reserved
27, 61	DOUT_CTP_58 (-, +)	Reserved
28, 62	DOUT_CTP_59 (-, +)	Reserved
29, 63	DOUT_CTP_60 (-, +)	Reserved
30, 64	DOUT_CTP_61 (-, +)	Reserved
31, 65	DOUT_CTP_62 (-, +)	Reserved
32, 66	DOUT_CTP_63 (-, +)	Reserved
33, 67	DOUT_CTP_65 (-, +)	Reserved
34, 68	GND	GND

Pins shown as Reserved are driven to zero by the CMM, and their value is included in the parity calculation at the CTP_IN. Pins shown as GND are signal grounds as described in 5.5

Appendix E Rear Transition Module connector layout, CP firmware.

The following tables show the connector pin-out of the rear transition module sockets.
Socket type 3M MDR 10268-55X3XX

Rear Transition Module socket 1 (nearest top of board):

Pins	schematic signal	CP Crate CMM output	CP System CMM input
1, 35	M_0 (-, +)	hits_thr0_bit(0)	hits_moda_thr0_bit(0)
2, 36	M_1 (-, +)	hits_thr0_bit(1)	hits_moda_thr0_bit(1)
3, 37	M_2 (-, +)	hits_thr0_bit(2)	hits_moda_thr0_bit(2)
4, 38	M_3 (-, +)	hits_thr1_bit(0)	hits_moda_thr1_bit(0)
5, 39	M_4 (-, +)	hits_thr1_bit(1)	hits_moda_thr1_bit(1)
6, 40	M_5 (-, +)	hits_thr1_bit(2)	hits_moda_thr1_bit(2)
7, 41	M_6 (-, +)	hits_thr2_bit(0)	hits_moda_thr2_bit(0)
8, 42	M_7 (-, +)	hits_thr2_bit(1)	hits_moda_thr2_bit(1)
9, 43	M_8 (-, +)	hits_thr2_bit(2)	hits_moda_thr2_bit(2)
10, 44	M_9 (-, +)	hits_thr3_bit(0)	hits_moda_thr3_bit(0)
11, 45	M_10 (-, +)	hits_thr3_bit(1)	hits_moda_thr3_bit(1)
12, 46	M_11 (-, +)	hits_thr3_bit(2)	hits_moda_thr3_bit(2)
13, 47	M_12 (-, +)	hits_thr4_bit(0)	hits_moda_thr4_bit(0)
14, 48	M_13 (-, +)	hits_thr4_bit(1)	hits_moda_thr4_bit(1)
15, 49	M_14 (-, +)	hits_thr4_bit(2)	hits_moda_thr4_bit(2)
16, 50	M_15 (-, +)	hits_thr5_bit(0)	hits_moda_thr5_bit(0)
17, 51	M_16 (-, +)	hits_thr5_bit(1)	hits_moda_thr5_bit(1)
18, 52	M_17 (-, +)	hits_thr5_bit(2)	hits_moda_thr5_bit(2)
19, 53	M_18 (-, +)	hits_thr6_bit(0)	hits_moda_thr6_bit(0)
20, 54	M_19 (-, +)	hits_thr6_bit(1)	hits_moda_thr6_bit(1)
21, 55	M_20(-, +)	hits_thr6_bit(2)	hits_moda_thr6_bit(2)
22, 56	M_21 (-, +)	hits_thr7_bit(0)	hits_moda_thr7_bit(0)
23, 57	M_22 (-, +)	hits_thr7_bit(1)	hits_moda_thr7_bit(1)
24, 58	M_23 (-, +)	hits_thr7_bit(2)	hits_moda_thr7_bit(2)
25, 59	M_24 (-, +)	Reserved	Reserved
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_25 (-, +)	Reserved	Reserved
33, 67	M_26 (-, +)	Parity	Parity
34, 68	GND	GND	GND

Rear Transition Module socket 2: (CP firmware)

Pins	schematic signal	CP Crate CMM output	CP System CMM input
1, 35	M_27 (-, +)	Reserved	hits_modb_thr0_bit(0)
2, 36	M_28 (-, +)	Reserved	hits_modb_thr0_bit(1)
3, 37	M_29 (-, +)	Reserved	hits_modb_thr0_bit(2)
4, 38	M_30 (-, +)	Reserved	hits_modb_thr1_bit(0)
5, 39	M_31 (-, +)	Reserved	hits_modb_thr1_bit(1)
6, 40	M_32 (-, +)	Reserved	hits_modb_thr1_bit(2)
7, 41	M_33 (-, +)	Reserved	hits_modb_thr2_bit(0)
8, 42	M_34 (-, +)	Reserved	hits_modb_thr2_bit(1)
9, 43	M_35 (-, +)	Reserved	hits_modb_thr2_bit(2)
10, 44	M_36 (-, +)	Reserved	hits_modb_thr3_bit(0)
11, 45	M_37 (-, +)	Reserved	hits_modb_thr3_bit(1)
12, 46	M_38 (-, +)	Reserved	hits_modb_thr3_bit(2)
13, 47	M_39 (-, +)	Reserved	hits_modb_thr4_bit(0)
14, 48	M_40 (-, +)	Reserved	hits_modb_thr4_bit(1)
15, 49	M_41 (-, +)	Reserved	hits_modb_thr4_bit(2)
16, 50	M_42 (-, +)	Reserved	hits_modb_thr5_bit(0)
17, 51	M_43 (-, +)	Reserved	hits_modb_thr5_bit(1)
18, 52	M_44 (-, +)	Reserved	hits_modb_thr5_bit(2)
19, 53	M_45 (-, +)	Reserved	hits_modb_thr6_bit(0)
20, 54	M_46 (-, +)	Reserved	hits_modb_thr6_bit(1)
21, 55	M_47 (-, +)	Reserved	hits_modb_thr6_bit(2)
22, 56	M_50 (-, +)	Not Connected	hits_modb_thr7_bit(0)
23, 57	M_51 (-, +)	Not Connected	hits_modb_thr7_bit(1)
24, 58	M_52 (-, +)	Not Connected	hits_modb_thr7_bit(2)
25, 59	M_53 (-, +)	Not Connected	Reserved
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_48 (-, +)	Reserved	Reserved
33, 67	M_49 (-, +)	Reserved	Parity
34, 68	GND	GND	GND

Rear Transition Module socket 3: (CP firmware)

pins	schematic signal	CP Crate CMM output	CP System CMM input
1, 35	M_54 (-, +)	Not Connected	hits_modc_thr0_bit(0)
2, 36	M_55 (-, +)	Not Connected	hits_modc_thr0_bit(1)
3, 37	M_56 (-, +)	Not Connected	hits_modc_thr0_bit(2)
4, 38	M_57 (-, +)	Not Connected	hits_modc_thr1_bit(0)
5, 39	M_58 (-, +)	Not Connected	hits_modc_thr1_bit(1)
6, 40	M_59 (-, +)	Not Connected	hits_modc_thr1_bit(2)
7, 41	M_60 (-, +)	Not Connected	hits_modc_thr2_bit(0)
8, 42	M_61 (-, +)	Not Connected	hits_modc_thr2_bit(1)
9, 43	M_62 (-, +)	Not Connected	hits_modc_thr2_bit(2)
10, 44	M_63 (-, +)	Not Connected	hits_modc_thr3_bit(0)
11, 45	M_64 (-, +)	Not Connected	hits_modc_thr3_bit(1)
12, 46	M_65 (-, +)	Not Connected	hits_modc_thr3_bit(2)
13, 47	M_66 (-, +)	Not Connected	hits_modc_thr4_bit(0)
14, 48	M_67 (-, +)	Not Connected	hits_modc_thr4_bit(1)
15, 49	M_68 (-, +)	Not Connected	hits_modc_thr4_bit(2)
16, 50	M_69 (-, +)	Not Connected	hits_modc_thr5_bit(0)
17, 51	M_70 (-, +)	Not Connected	hits_modc_thr5_bit(1)
18, 52	M_71 (-, +)	Not Connected	hits_modc_thr5_bit(2)
19, 53	M_72 (-, +)	Not Connected	hits_modc_thr6_bit(0)
20, 54	M_73 (-, +)	Not Connected	hits_modc_thr6_bit(1)
21, 55	M_74 (-, +)	Not Connected	hits_modc_thr6_bit(2)
22, 56	M_75 (-, +)	Not Connected	hits_modc_thr7_bit(0)
23, 57	M_76 (-, +)	Not Connected	hits_modc_thr7_bit(1)
24, 58	M_77 (-, +)	Not Connected	hits_modc_thr7_bit(2)
25, 59	GND	Terminated	Terminated
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_78 (-, +)	Not Connected	Reserved
33, 67	M_79 (-, +)	Not Connected	Parity
34, 68	GND	GND	GND

Appendix F Rear Transition Module connector layout, Jet firmware.

The following tables show the connector pin-out of the rear transition module sockets. Socket type 3M MDR 10268-55X3XX

Rear Transition Module socket 1 (nearest top of board, Jet firmware):

Pins	schematic signal	Jet Crate CMM output	Jet System CMM input
1, 35	M_0 (-, +)	main_jets_thr0_bit(0)	main_jets_thr0_bit(0)
2, 36	M_1 (-, +)	main_jets_thr0_bit(1)	main_jets_thr0_bit(1)
3, 37	M_2 (-, +)	main_jets_thr0_bit(2)	main_jets_thr0_bit(2)
4, 38	M_3 (-, +)	main_jets_thr1_bit(0)	main_jets_thr1_bit(0)
5, 39	M_4 (-, +)	main_jets_thr1_bit(1)	main_jets_thr1_bit(1)
6, 40	M_5 (-, +)	main_jets_thr1_bit(2)	main_jets_thr1_bit(2)
7, 41	M_6 (-, +)	main_jets_thr2_bit(0)	main_jets_thr2_bit(0)
8, 42	M_7 (-, +)	main_jets_thr2_bit(1)	main_jets_thr2_bit(1)
9, 43	M_8 (-, +)	main_jets_thr2_bit(2)	main_jets_thr2_bit(2)
10, 44	M_9 (-, +)	main_jets_thr3_bit(0)	main_jets_thr3_bit(0)
11, 45	M_10 (-, +)	main_jets_thr3_bit(1)	main_jets_thr3_bit(1)
12, 46	M_11 (-, +)	main_jets_thr3_bit(2)	main_jets_thr3_bit(2)
13, 47	M_12 (-, +)	main_jets_thr4_bit(0)	main_jets_thr4_bit(0)
14, 48	M_13 (-, +)	main_jets_thr4_bit(1)	main_jets_thr4_bit(1)
15, 49	M_14 (-, +)	main_jets_thr4_bit(2)	main_jets_thr4_bit(2)
16, 50	M_15 (-, +)	main_jets_thr5_bit(0)	main_jets_thr5_bit(0)
17, 51	M_16 (-, +)	main_jets_thr5_bit(1)	main_jets_thr5_bit(1)
18, 52	M_17 (-, +)	main_jets_thr5_bit(2)	main_jets_thr5_bit(2)
19, 53	M_18 (-, +)	main_jets_thr6_bit(0)	main_jets_thr6_bit(0)
20, 54	M_19 (-, +)	main_jets_thr6_bit(1)	main_jets_thr6_bit(1)
21, 55	M_20(-, +)	main_jets_thr6_bit(2)	main_jets_thr6_bit(2)
22, 56	M_21 (-, +)	main_jets_thr7_bit(0)	main_jets_thr7_bit(0)
23, 57	M_22 (-, +)	main_jets_thr7_bit(1)	main_jets_thr7_bit(1)
24, 58	M_23 (-, +)	main_jets_thr7_bit(2)	main_jets_thr7_bit(2)
25, 59	M_24 (-, +)	Reserved	Reserved
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_25 (-, +)	Reserved	Reserved
33, 67	M_26 (-, +)	Parity	Parity
34, 68	GND	GND	GND

Rear Transition Module socket 2: (Jet firmware)

Pins	schematic signal	Jet Crate CMM output	Jet System CMM input
1, 35	M_27 (-, +)	fwd_jets_Lthr0_bit(0)	fwd_jets_Lthr0_bit(0)
2, 36	M_28 (-, +)	fwd_jets_Lthr0_bit(1)	fwd_jets_Lthr0_bit(1)
3, 37	M_29 (-, +)	fwd_jets_Lthr1_bit(0)	fwd_jets_Lthr1_bit(0)
4, 38	M_30 (-, +)	fwd_jets_Lthr1_bit(1)	fwd_jets_Lthr1_bit(1)
5, 39	M_31 (-, +)	fwd_jets_Lthr2_bit(0)	fwd_jets_Lthr2_bit(0)
6, 40	M_32 (-, +)	fwd_jets_Lthr2_bit(1)	fwd_jets_Lthr2_bit(1)
7, 41	M_33 (-, +)	fwd_jets_Lthr3_bit(0)	fwd_jets_Lthr3_bit(0)
8, 42	M_34 (-, +)	fwd_jets_Lthr3_bit(1)	fwd_jets_Lthr3_bit(1)
9, 43	M_35 (-, +)	fwd_jets_Rthr0_bit(0)	fwd_jets_Rthr0_bit(0)
10, 44	M_36 (-, +)	fwd_jets_Rthr0_bit(1)	fwd_jets_Rthr0_bit(1)
11, 45	M_37 (-, +)	fwd_jets_Rthr1_bit(0)	fwd_jets_Rthr1_bit(0)
12, 46	M_38 (-, +)	fwd_jets_Rthr1_bit(1)	fwd_jets_Rthr1_bit(1)
13, 47	M_39 (-, +)	fwd_jets_Rthr2_bit(0)	fwd_jets_Rthr2_bit(0)
14, 48	M_40 (-, +)	fwd_jets_Rthr2_bit(1)	fwd_jets_Rthr2_bit(1)
15, 49	M_41 (-, +)	fwd_jets_Rthr3_bit(0)	fwd_jets_Rthr3_bit(0)
16, 50	M_42 (-, +)	fwd_jets_Rthr3_bit(1)	fwd_jets_Rthr3_bit(1)
17, 51	M_43 (-, +)	Reserved	Reserved
18, 52	M_44 (-, +)	Reserved	Reserved
19, 53	M_45 (-, +)	Reserved	Reserved
20, 54	M_46 (-, +)	Reserved	Reserved
21, 55	M_47 (-, +)	Reserved	Reserved
22, 56	M_50 (-, +)	Not Connected	Not Connected
23, 57	M_51 (-, +)	Not Connected	Not Connected
24, 58	M_52 (-, +)	Not Connected	Not Connected
25, 59	M_53 (-, +)	Not Connected	Not Connected
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_48 (-, +)	Reserved	Reserved
33, 67	M_49 (-, +)	Parity	Parity
34, 68	GND	GND	GND

Rear Transition Module socket 3: (Jet firmware)

pins	schematic signal	Jet Crate CMM output	Jet System CMM input
1, 35	M_54 (-, +)	Not Connected	Reserved
2, 36	M_55 (-, +)	Not Connected	Reserved
3, 37	M_56 (-, +)	Not Connected	Reserved
4, 38	M_57 (-, +)	Not Connected	Reserved
5, 39	M_58 (-, +)	Not Connected	Reserved
6, 40	M_59 (-, +)	Not Connected	Reserved
7, 41	M_60 (-, +)	Not Connected	Reserved
8, 42	M_61 (-, +)	Not Connected	Reserved
9, 43	M_62 (-, +)	Not Connected	Reserved
10, 44	M_63 (-, +)	Not Connected	Reserved
11, 45	M_64 (-, +)	Not Connected	Reserved
12, 46	M_65 (-, +)	Not Connected	Reserved
13, 47	M_66 (-, +)	Not Connected	Reserved
14, 48	M_67 (-, +)	Not Connected	Reserved
15, 49	M_68 (-, +)	Not Connected	Reserved
16, 50	M_69 (-, +)	Not Connected	Reserved
17, 51	M_70 (-, +)	Not Connected	Reserved
18, 52	M_71 (-, +)	Not Connected	Reserved
19, 53	M_72 (-, +)	Not Connected	Reserved
20, 54	M_73 (-, +)	Not Connected	Reserved
21, 55	M_74 (-, +)	Not Connected	Reserved
22, 56	M_75 (-, +)	Not Connected	Reserved
23, 57	M_76 (-, +)	Not Connected	Reserved
24, 58	M_77 (-, +)	Not Connected	Reserved
25, 59	GND	Terminated	Terminated
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_78 (-, +)	Not Connected	Reserved
33, 67	M_79 (-, +)	Not Connected	Reserved
34, 68	GND	GND	GND

Appendix G Rear Transition Module connector layout, Energy firmware.

The following tables show the connector pin-out of the rear transition module sockets.
Socket type 3M MDR 10268-55X3XX

Rear Transition Module socket 1 (nearest top of board, Energy):

Pins	schematic signal	E Crate CMM output	E System CMM input
1, 35	M_0 (+, -)	Et_bit(0)	Et_bit(0)
2, 36	M_1 (+, -)	Et_bit(1)	Et_bit(1)
3, 37	M_2 (+, -)	Et_bit(2)	Et_bit(2)
4, 38	M_3 (+, -)	Et_bit(3)	Et_bit(3)
5, 39	M_4 (+, -)	Et_bit(4)	Et_bit(4)
6, 40	M_5 (+, -)	Et_bit(5)	Et_bit(5)
7, 41	M_6 (+, -)	Et_bit(6)	Et_bit(6)
8, 42	M_7 (+, -)	Et_bit(7)	Et_bit(7)
9, 43	M_8 (+, -)	Et_bit(8)	Et_bit(8)
10, 44	M_9 (+, -)	Et_bit(9)	Et_bit(9)
11, 45	M_10 (+, -)	Et_bit(10)	Et_bit(10)
12, 46	M_11 (+, -)	Et_bit(11)	Et_bit(11)
13, 47	M_12 (+, -)	Et_bit(12)	Et_bit(12)
14, 48	M_13 (+, -)	Et_bit(13)	Et_bit(13)
15, 49	M_14 (+, -)	Et_bit(14)	Et_bit(14)
16, 50	M_15 (+, -)	Et_Parity	Et_Parity
17, 51	M_16 (+, -)	Ex_bit(0)	Ex_bit(0)
18, 52	M_17 (+, -)	Ex_bit(1)	Ex_bit(1)
19, 53	M_18 (+, -)	Ex_bit(2)	Ex_bit(2)
20, 54	M_19 (+, -)	Ex_bit(3)	Ex_bit(3)
21, 55	M_20(+, -)	Ex_bit(4)	Ex_bit(4)
22, 56	M_21 (+, -)	Ex_bit(5)	Ex_bit(5)
23, 57	M_22 (+, -)	Ex_bit(6)	Ex_bit(6)
24, 58	M_23 (+, -)	Ex_bit(7)	Ex_bit(7)
25, 59	M_24 (+, -)	Ex_bit(8)	Ex_bit(8)
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_25 (+, -)	Ex_bit(9)	Ex_bit(9)
33, 67	M_26 (+, -)	Ex_bit(10)	Ex_bit(10)
34, 68	GND	GND	GND

Rear Transition Module socket 2: (Energy firmware)

Pins	schematic signal	E Crate CMM output	E System CMM input
1, 35	M_27 (+, -)	Ex_bit(11)	Ex_bit(11)
2, 36	M_28 (+, -)	Ex_bit(12)	Ex_bit(12)
3, 37	M_29 (+, -)	Ex_bit(13)	Ex_bit(13)
4, 38	M_30 (+, -)	Ex_bit(14)	Ex_bit(14)
5, 39	M_31 (+, -)	Ex_bit(15)	Ex_bit(15)
6, 40	M_32 (+, -)	Ex_Parity	Ex_Parity
7, 41	M_33 (+, -)	Ey_bit(0)	Ey_bit(0)
8, 42	M_34 (+, -)	Ey_bit(1)	Ey_bit(1)
9, 43	M_35 (+, -)	Ey_bit(2)	Ey_bit(2)
10, 44	M_36 (+, -)	Ey_bit(3)	Ey_bit(3)
11, 45	M_37 (+, -)	Ey_bit(4)	Ey_bit(4)
12, 46	M_38 (+, -)	Ey_bit(5)	Ey_bit(5)
13, 47	M_39 (+, -)	Ey_bit(6)	Ey_bit(6)
14, 48	M_40 (+, -)	Ey_bit(7)	Ey_bit(7)
15, 49	M_41 (+, -)	Ey_bit(8)	Ey_bit(8)
16, 50	M_42 (+, -)	Ey_bit(9)	Ey_bit(9)
17, 51	M_43 (+, -)	Ey_bit(10)	Ey_bit(10)
18, 52	M_44 (+, -)	Ey_bit(11)	Ey_bit(11)
19, 53	M_45 (+, -)	Ey_bit(12)	Ey_bit(12)
20, 54	M_46 (+, -)	Ey_bit(13)	Ey_bit(13)
21, 55	M_47 (+, -)	Ey_bit(14)	Ey_bit(14)
22, 56	M_50 (+, -)	Not Connected	Reserved
23, 57	M_51 (+, -)	Not Connected	Reserved
24, 58	M_52 (+, -)	Not Connected	Reserved
25, 59	M_53 (+, -)	Not Connected	Reserved
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_48 (+, -)	Ey_bit(15)	Ey_bit(15)
33, 67	M_49 (+, -)	Ey_Parity	Ey_Parity
34, 68	GND	GND	GND

Rear Transition Module socket 3: (|Energy firmware)

pins	schematic signal	E Crate CMM output	E System CMM input
1, 35	M_54 (+, -)	Not Connected	Reserved
2, 36	M_55 (+, -)	Not Connected	Reserved
3, 37	M_56 (+, -)	Not Connected	Reserved
4, 38	M_57 (+, -)	Not Connected	Reserved
5, 39	M_58 (+, -)	Not Connected	Reserved
6, 40	M_59 (+, -)	Not Connected	Reserved
7, 41	M_60 (+, -)	Not Connected	Reserved
8, 42	M_61 (+, -)	Not Connected	Reserved
9, 43	M_62 (+, -)	Not Connected	Reserved
10, 44	M_63 (+, -)	Not Connected	Reserved
11, 45	M_64 (+, -)	Not Connected	Reserved
12, 46	M_65 (+, -)	Not Connected	Reserved
13, 47	M_66 (+, -)	Not Connected	Reserved
14, 48	M_67 (+, -)	Not Connected	Reserved
15, 49	M_68 (+, -)	Not Connected	Reserved
16, 50	M_69 (+, -)	Not Connected	Reserved
17, 51	M_70 (+, -)	Not Connected	Reserved
18, 52	M_71 (+, -)	Not Connected	Reserved
19, 53	M_72 (+, -)	Not Connected	Reserved
20, 54	M_73 (+, -)	Not Connected	Reserved
21, 55	M_74 (+, -)	Not Connected	Reserved
22, 56	M_75 (+, -)	Not Connected	Reserved
23, 57	M_76 (+, -)	Not Connected	Reserved
24, 58	M_77 (+, -)	Not Connected	Reserved
25, 59	GND	Terminated	Terminated
26, 60	GND	Terminated	Terminated
27, 61	GND	Terminated	Terminated
28, 62	GND	Terminated	Terminated
29, 63	GND	Terminated	Terminated
30, 64	GND	Terminated	Terminated
31, 65	GND	Terminated	Terminated
32, 66	M_78 (+, -)	Not Connected	Reserved
33, 67	M_79 (+, -)	Not Connected	Reserved
34, 68	GND	GND	GND