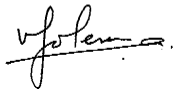
# Project Specification

# Project Name: ATLAS Calorimeter First Level Trigger- Data Source and Sink Module

**Version: 2d.**

**March 2000**

| Approval | Name | Signature | Date |
|---|---|---|---|
| Project Manager | V. Perera |  | |

**Distribution for all updates:**

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**Last release: Version 2b May 1999**
**Note: Pages 11-13, 19, 21, 22 has been updated since the last release**

**Last release: Version 2c July 1999**
**Note: Pages 11, 12, 13, 14, 15, 18, 19 has been updated since the last release**
**(See page 47)**

# 1. Scope

Data source and sink (DSS) modules are required to generate the test patterns for testing links (G-links, LVDS, and others) and to test modules such as the prototype read-out drivers (ROD). Also the DSS module can be also used for testing the ASICs as well as MCMs.
A general-purpose motherboard will be designed to meet all the data source and sink functions as described below, with the requirement of only having to design specific daughter boards for various applications.

## 2.Related Projects and Documents

2.1 S-Link interface specification http://www.cern.ch/hsi/s-link/
2.2 Draft Standard for a Common Mezzanine Card Family: CMC, P1386/Draft 2.0 April 4, 1995.
2.3 TTCrx Reference Manual, J. Christiansen, *et al*, CERN-ECP/MIC, Version 2.2, July 1997
2.4 Specification of the 'G-Link' Daughter Boards for the 'DSS' Test Platform, R.Hatley
2.5 LVDS Source and Sink CMC Daughter Boards for the DSS Module, R. Staley.
2.6 HDMP-1022/1024 Low cost Gigabit Rate Transmit/Receive Chip set with TTLI/O, Hewlett Packard.
2.7 DS92LV1021 and DS92LV1210 serialiser deserialiser, National Semiconductor
2.8 Clock and Control Module draft 2.0 Specification, V. Perera

# 3. Technical Aspects

The DSS motherboard will be 6U VME with slots for two single CMC standard daughter modules or one double CMC standard daughter module. Two S-link daughter cards can also be used on the motherboard with its dedicated connectors and electronics.

## 3.1 Requirements and Specifications

Test modules are required for testing modules and data links for the ATLAS first-level calorimeter trigger processor.
The DSS modules will generate and receive the test data from the device under test for verification.

The DSS module will comprise of a mother board, which will implement common functions such as generate, receive and compare test patterns in real time up to 40 MHz; VME interface, control and status registers, etc.
The daughter boards will implement the physical layer to transmit/receive data up to 80 bits wide and can configure the mother board to perform source (transmit) or sink (receive) functions on either or both CMC slots. However in the case of the S-links, only one source and one destination card is possible on predefined positions (Key-in pins) on the motherboard.

### 3.2 DSS Mother Board

The 6U-mother board will have a standard A32, A24, D32 VME interface, and a TTC interface. Eight 32K x 32 bit Dual-port RAMs and eight FPGAs (Data FPGA) will handle the data source, sink requirements, and handle all the interface signals required by each type of daughter board. Figure 1 shows a block diagram of the DSS motherboard. The S-link data will be handled by the S-link FPGAs and the dual port RAMs for implementation convenience.
When a daughter board (except for S-Link) is plugged on the mother board, the mother board EEPROMs will be disabled and the daughter board specific logic will be down loaded to the Data FPGAs from the daughter board EEPROMs

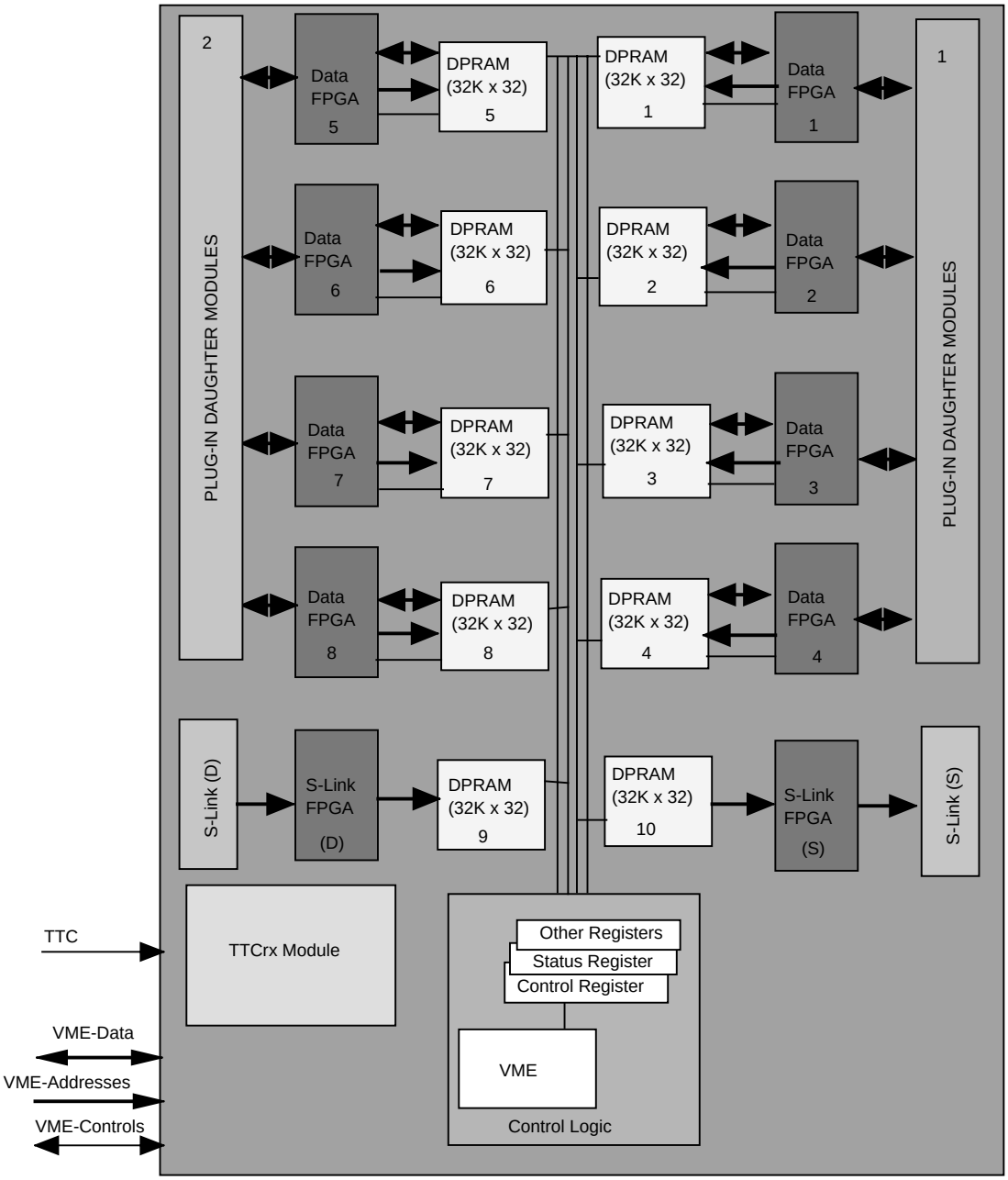


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Figure 1. Block Diagram of DSS Module- Mother Board

## 3.2.1 FPGA Implementation

There are two types of 'data FPGAs' which handles source data and sink data in two blocks of four, interfacing to the two daughter board via the CMC connectors as shown in figure 1. The S-link data is handled by separate FPGAs.

### 3.2.1.1 Source FPGA

The source FPGAs will perform the following functions:
1. Provide interface to the daughter boards.
2. Implements the Serialiser ASIC readout logic. - required to test the Readout Driver
3. Implements a Pseudo Random Bit Pattern (PRBP) generator and checker. Other data patterns such as ramps can also be implemented if required.
4. Directly connect the Dual-port RAM data bus on to the connector pins -allowing to generate any test pattern.
5. FPGA code can be developed to implement the test data for the Jet system.

A block diagram is shown below.

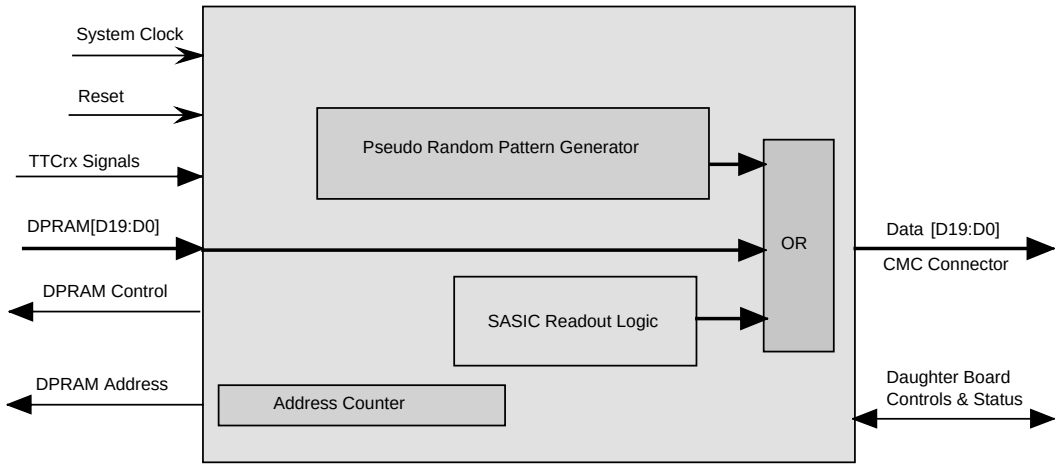



Figure 2. Block Diagram of the Source FPGAs

### 3.2.1.2 Sink FPGAs

The sink FPGAs will interface between the Dual-port RAM and the daughter boards, recording the data on to the dual-port RAM from the daughter boards, which can then be accessed via the VME. It will also provide:
1. Bit error checking facility on the PRBP data, this data is also written onto the dual port RAMs.
2. Bit error checking between the received data and pre-loaded data on the dual port RAM.
3. When an error occurs the data word is recorded onto an internal register with the contents of the address counter, which can be read out via the VME.

Figure 3 shows the block diagram of the sink functions.

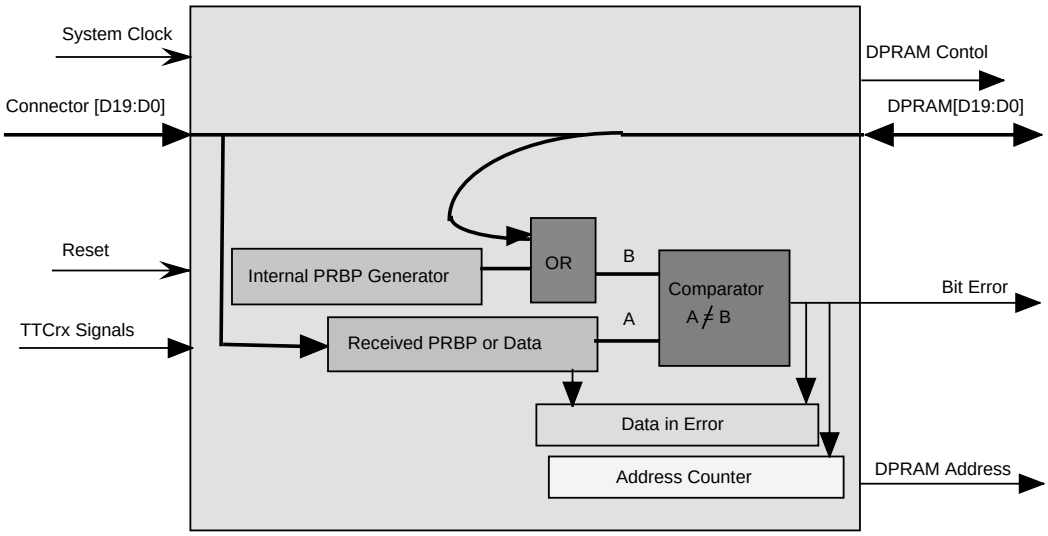



Figure 3. Block Diagram of the Sink FPGAs

#### 3.2.1.3 S-Link FPGA

There will be two separate FPGAs to handle data from a destination S-link and the source S-link.

### 3.2.2 Dual port RAM

32K x 32 wide Dual port memory will be used for test data buffers.
In the case of G-Link and LVDS serialiser/deserialiser daughter boards, only 20 bits out of the 32 will be used on each channel.

### 3.2.3 VME Logic

All VME related logic such as; address decoding, memory addressing, and any other controls and status registers required will be implemented on a programmable logic device (Control Logic)

### 3.2.4 TTC Module

A plug-in daughter module (CERN TTCrx module) will generate the TTC signals by using a TTCrx chip. When the TTC system is not available the appropriate signals (Clock, Start, etc.) will be received from an external source, such as the one used in the demonstrator system (TCM). For more details refer to the CMM draft specification.

### 3.2.5 Component Height Restrictions on the Mother Board

The component height restrictions and exclusion zones are shown in figure 4.

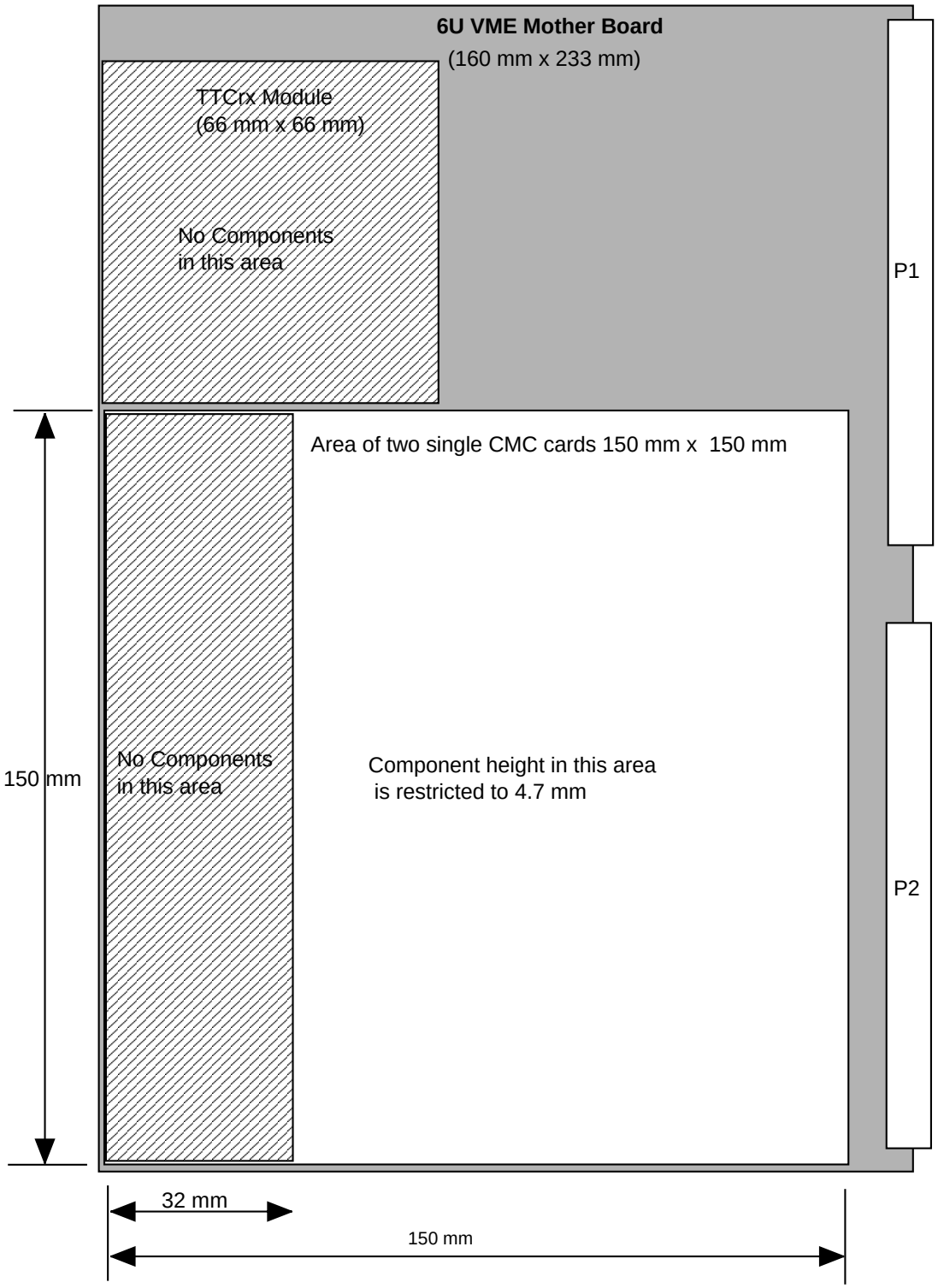



Figure 4. Mother Board Component Placement Restrictions (not to scale)

### 3.2.6 Signal Handling on the Mother Boards

The source modules will terminate the signals using series termination (Rs) for a 75 Ω track impedance. Since the same pins of the FPGA are used when in sink mode or in source mode, the series resister (Rs) at the FPGA end will be present in both modes.

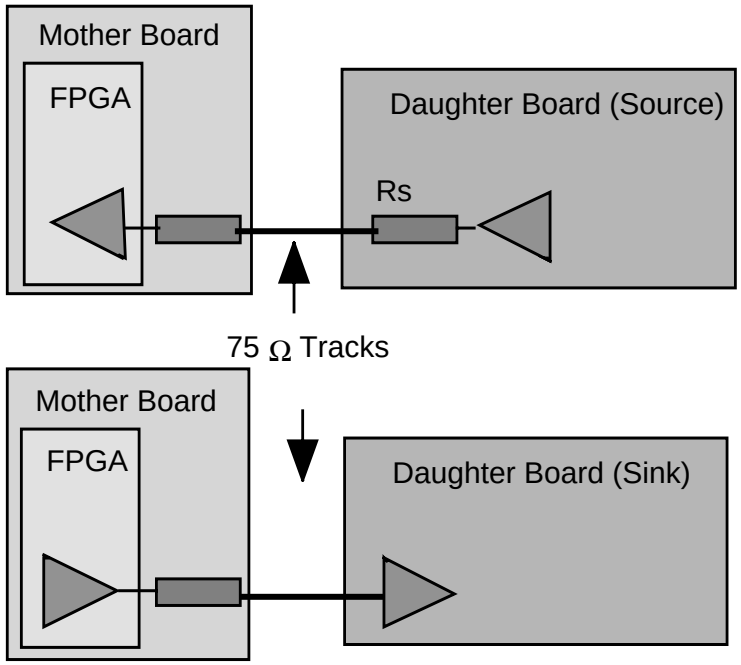



Figure 5. Source Termination

The following table indicates the minimum and maximum values of the signal through the CMC connectors. All signals are TTL compatible

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
|---|---|---|---|---|---|
| Output Drive Low/High | $I_{OL}/I_{OH}$ | | | 24 | mA |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | | 3.3 | V |
| Clock | CLK | - | - | 40 | MHz |

## 3.2.7 Front Panel Input and Outputs

### *3.2.7.1 Front Panel Inputs*

| Description | Logic | Connector |
|---|---|---|
| TTCin | Balanced LVDS | LEMO 00 |
| 40 MHz System Clock * | Balanced ECL | LEMO 00 |
| Start * | Balanced ECL | LEMO 00 |
| Stop Transmission # | Balanced LVDS | 2 Pin Harwin 2pin |

***Notes:* *** Not required when the TTC is in use

Start is an active high signal, which will emulate the broadcast start from TTC (see 3.2.8.5.1)

# Active high; for example BUSY from the ROD module

### **3.2.7.*2 Front Panel Outputs***

| Description | Logic | Connector |
|---|---|---|
| Logical OR of Bit Errors | Balanced ECL | 2 Pin Harwin 2pin |

Note: space permitting, individual bit error signals will brought on to the front panel via an IDC connector.

### *3.2.7.3 Front Panel Monitoring (LEDs)*

The LEDs will be located at the top of the front panel.

| Description | Signal name | Colour |
|---|---|---|
| +5 Volts | | Green |
| -5 Volts | | Green |
| +3.3 Volts | | Green |
| System clock is active | SYSCLK | Green |
| FPGAs Loaded | PromsDone+ | Green |
| VME active | ModuleSel | Yellow |
| Bit Errors | Bit_Error | Red |

* Fast signals will be stretched so that they will light the LEDs for long enough to be seen.
+ Logical AND of all the PromDone signals

### *3.2.7.4 Rear Panel Input and Outputs*

1) VME J1 Connector
2) VME J2 Connector

### *3.2.7.5 Power Requirements*

| Voltage rail | Maximum. Current |
|---|---|
| +5V & +3.3V | 9A |
| -5V | 200 mA |
| +3.3V | 7A |

### 3.2.7.*6 Ground Points*

Ground points will be provided for scope probe grounding in exposed areas of the motherboard.

### *3.2.7.7 Test and Set-up Points*

1. There will be logic analyser probe points on various data paths to aid in debugging the module.
2. JTAG boundary scan port

### 3.2.7.8 Configuring the Data FPGAs

The Data FPGAs can be configured in the following ways to give maximum flexibility for the module users.

On the Mother Board:
1. EEPROMs (equivalent to Xilinx XC1701L) will be socketed so that they can be programmed with the configuration data using a standalone device programmer.
2. ISP port (Xilinx exchequer) will be provided to down load configuration data from a PC for example.
3. VME port via a register will be provided, for downloading the FPGAs as well as the EEPROMs. The user must provide the software drivers.

On the Daughter Board:
1. EEPROMs (AT17LV010) must be socketed
2. If you require in-circuit programmability of the EEPROM then the daughter board designers must provide a relevant socket and software drivers.
3. The EEPROM can also be programmed in a similar manner to 3 above.

The Mother board will drive the DisMotherProm1 signal and control the way in which the FPGAs will be configured, therefore the daughter board must connect DisMotherProm2 pin to DisMotherProm1 pin.

## *3.2.8* Programming Model

### *3.2.8.1 Guidelines*

These are to aid the software control of the module.

1. All registers can be read by the computer, hence there are no 'write only' registers.

   1.1 All Status Registers shall be Read-Only registers.
   1.2 All Control Registers shall be Read/Write registers.
   1.3 Reading back a register will return the last value written.
   1.4 Attempts to write to read-only registers or undefined portions of registers will result in the non-modifiable fields being left unchanged.

2. If the computer tries to read or write a value, which the DSS module itself is able to modify at the same time, the data integrity cannot be guaranteed. The only exception been the Control Register and the Status Register. Therefore it is recommended that before any software tries to read or write to any registers the status of the module should ascertained by reading the Status Register.

3. When the address space occupied by the DSS module is accessed, it will always respond with a handshake to avoid a bus error.

4. The power-up condition of all registers will be all zeros, unless otherwise stated.

### *3.2.8.2 Notation*

The names of the registers and bit fields within them are written in *italic*. The names of the signal lines are *underlined italic*. Bit fields are labelled Input to Card and Output from Card rather than Write and Read to make it clear whether it is the card or the computer which is doing the writing.

In this document, a byte is always an 8-bit field, a word is always 16 bits and a long-word is always 32 bits.

Setting a bit field means writing a 1 to it, clearing it means writing a 0.

### *3.2.8.3 Memory Map*

The DSS module is addressed using an A32/A24 address bus. It uses the 21 least significant bits (up to A20) of the A32 address bus, hence the address space of the DSS module is 21-bits. This corresponds to 2048 kilobytes per module. The most significant bits of the address bus can be pre-set by switches (accessible from the front panel) to allow the 2048 kilobyte memory space required to sit at any convenient 2048 kilobyte boundary within the four Giga byte A32 address space.

| Byte Address | Register type | Register Name | Size in bytes | Description |
|---|---|---|---|---|
| 000000 | RO | *MotherID* | 4 | Type, serial number & revision of mother board |
| 000004 | RW | *MotherCR* | 4 | Control Register |
| 000008 | RO | *MotherSR* | 4 | Status Register |
| 00000C | RO | *DaughterID* | 4 | Type, serial number & revision of daughter board |
| 000010 | RW | *DaughterCR* | 4 | Control Register |
| 000014 | RO | *DaughterSR* | 4 | Status Register |
| 000018 | RW | *Timing_Reg* | 4 | Clock Phase adjustment |
| 00001C | RW | *OffsetReg* | 4 | Offset Register |
| 000020 | RW | *Pulse Register* | 4 | Generates pulses |
| 000024 | RO | *Bit-error Register* | 4 | Bit errors |
| 000028 | RO | *VME-Revision* | 4 | VME Revision |
| 00002C | RW | *Program_Reg* | 4 | VME 'ISP' programming |
| 000030 00003C | | | | Undefined |
| 000040 | RO | *FPGA_Reg_A1* | 4 | BCID Counter (Source) Error Counter (Sink) |
| 000044 | RO | *FPGA_Reg_A2* | 4 | BCID/Error Counter |
| 000048 | RO | *FPGA_Reg_A3* | 4 | BCID/Error Counter |
| 00004C | RO | *FPGA_Reg_A4* | 4 | BCID/Error Counter |
| 000050 | RO | *FPGA_Reg_A5* | 4 | BCID/Error Counter |
| 000054 | RO | *FPGA_Reg_A6* | 4 | BCID/Error Counter |
| 000058 | RO | *FPGA_Reg_A7* | 4 | BCID/Error Counter |
| 00005C | RO | *FPGA_Reg_A8* | 4 | BCID/Error Counter |
| 000060 | RW | *SLINK_FIFO* | 4 | FIFO (S-Link Destination) |
| 000064 | RW | ---------- | 4 | *Reserved* |
| 000068 | RW | *FPGA_Reg_B1* | 4 | Pseudo Random Generator Seed (FPGA 1) |
| 00006C | RW | *FPGA_Reg_B2* | 4 | Pseudo Random Generator Seed (FPGA 2) |
| 000070 | RW | *FPGA_Reg_B3* | 4 | Pseudo Random Generator Seed (FPGA 3) |
| 000074 | RW | *FPGA_Reg_B4* | 4 | Pseudo Random Generator Seed (FPGA 4) |
| 000078 | RW | *FPGA_Reg_B5* | 4 | Pseudo Random Generator Seed (FPGA 5) |
| 00007C | RW | *FPGA_Reg_B6* | 4 | Pseudo Random Generator Seed (FPGA 6) |
| 000080 | RW | *FPGA_Reg_B7* | 4 | Pseudo Random Generator Seed (FPGA 7) |
| 000084 | RW | *FPGA_Reg_B8* | 4 | Pseudo Random Generator Seed (FPGA 8) |

| | | | | |
|---|---|---|---|---|
| 000088 | RW | *Slink_D_CR* | 4 | Control Reg (S-Link Destination) |
| 00008C | RW | *Slink_S_CR* | 4 | Control Reg (S-Link Source) |
| 000090 | RW | *FPGA_Reg_C1* | 4 | Last Word in Error (Sink) |
| 000094 | RW | *FPGA_Reg_C2* | 4 | Last Word in Error (Sink) |
| 000098 | RW | *FPGA_Reg_C3* | 4 | Last Word in Error (Sink) |
| 00009C | RW | *FPGA_Reg_C4* | 4 | Last Word in Error (Sink) |
| 0000A0 | RW | *FPGA_Reg_C5* | 4 | Last Word in Error (Sink) |
| 0000A4 | RW | *FPGA_Reg_C6* | 4 | Last Word in Error (Sink) |
| 0000A8 | RW | *FPGA_Reg_C7* | 4 | Last Word in Error (Sink) |
| 0000AC | RW | *FPGA_Reg_C8* | 4 | Last Word in Error (Sink) |
| 0000B0 | RW | ---------- | 4 | *undefined* |
| 0000B4 | RW | *Slink_S_SR* | 4 | Status Reg (S-Link Source) |
| 0000B8 | RO | *Address_counter1* | 4 | Address when the error occurred (Sink) |
| 0000BC | RO | *Address_counter2* | 4 | Address when the error occurred (Sink) |
| 0000C0 | RO | *Address_counter3* | 4 | Address when the error occurred (Sink) |
| 0000C4 | RO | *Address_counter4* | 4 | Address when the error occurred (Sink) |
| 0000C8 | RO | *Address_counter5* | 4 | Address when the error occurred (Sink) |
| 0000CC | RO | *Address_counter6* | 4 | Address when the error occurred (Sink) |
| 0000D0 | RO | *Address_counter7* | 4 | Address when the error occurred (Sink) |
| 0000D4 | RO | *Address_counter8* | 4 | Address when the error occurred (Sink) |
| 0000D8 | RO | *Address_counter9* | 4 | Address Counter (S-Link Destination) |
| 0000DC | RO | *Address_counter10* | 4 | Address Counter (S-Link Source) |
| 0000E0 | RO | *FPGA1_Rev* | 4 | Revision register |
| 0000E4 | RO | *FPGA2_Rev* | 4 | Revision register |
| 0000E8 | RO | *FPGA3_Rev* | 4 | Revision register |
| 0000EC | RO | *FPGA4_Rev* | 4 | Revision register |
| 0000F0 | RO | *FPGA5_Rev* | 4 | Revision register |
| 0000F4 | RO | *FPGA6_Rev* | 4 | Revision register |
| 0000F8 | RO | *FPGA7_Rev* | 4 | Revision register |
| 0000FC | RO | *FPGA8_Rev* | 4 | Revision register |
| 000100 | RO | *S-Link(D)-Revision* | 4 | Revision register |
| 000104 | RO | *S-Link(S)-Revision* | 4 | Revision register |
| 000108<br>001FFF | | | | Undefined |

| | | | | |
|---|---|---|---|---|
| 020000<br>03FFFF | RW | *Data Buffer 1* | 128K<br>(32 K x 32) | Daughter board 1<br>DC_Data_A[19:0] |
| 040000<br>05FFFF | RW | *Data Buffer 2* | 128K<br>(32 K x 32) | Daughter board 1<br>DC_Data_B[19:0] |
| 060000<br>07FFFF | RW | *Data Buffer 3* | 128K<br>(32 K x 32) | Daughter board 1<br>DC_Data_C[19:0] |
| 080000<br>09FFFF | RW | *Data Buffer 4* | 128K<br>(32 K x 32) | Daughter board 1<br>DC_Data_D[19:0] |
| 0A0000<br>0BFFFF | RW | *Data Buffer 5* | 128K<br>(32 K x 32) | Daughter board 2<br>DC_Data_A[19:0] |
| 0C0000<br>0DFFFF | RW | *Data Buffer 6* | 128K<br>(32 K x 32) | Daughter board 2<br>DC_Data_B[19:0] |
| 0E0000<br>0FFFFF | RW | *Data Buffer 7* | 128K<br>(32 K x 32) | Daughter board 2<br>DC_Data_C[19:0] |
| 100000<br>11FFFF | RW | *Data Buffer 8* | 128K<br>(32 K x 32) | Daughter board 2<br>DC_Data_D[19:0] |
| 120000<br>13FFFF | RW | *Data Buffer 9* | 128K<br>(32 K x 32) | Data Buffer 9 S-Link Source |
| 140000<br>15FFFF | RW | *Data Buffer 10* | 128K<br>(32 K x 32) | Data Buffer 10 S-Link Destination |
| 160000<br>1FFFFF | | | | Undefined |

RO means that the computer can only read the value of this register, writing has no effect either to the value or the state of the module.

RW means that the computer can affect the state of the module by writing to this register.

All memory on the board is directly mapped into VME address space so as to be conveniently accessible by the computer.

The module responds to the following VME Address Modifier codes.

| AM code | |
|---|---|
| 39 | Standard (A24) non-privileged data access |
| 3D | Standard (A24) supervisory data access |
| 09 | Extended (A32) non-privileged data access |
| 0D | Extended (A32) supervisory data access |

### *3.2.8.4 Mother ID Register*

The DSS module identification register is used to uniquely identify the module.

| Register Bits | Assignment | Description |
|---|---|---|
| 0-15 | RAL Number (2414) | Same for each module type, number recorded in RAL register |
| 16-23 | Module Serial number | an unique number assigned to each module |
| 24-27 | Issue | Issue number |
| 28 -31 | - | Unused |

### *3.2.8.5 Mother Control Register*

All bit fields are inputs to board. Power-up condition will initially set all control register bits to 0 unless otherwise stated.

| Bit | Descriptive Name | Signal name | |
|---|---|---|---|
| 0 (LSB) | *Test Mode 0* | *Mode-0* | |
| 1 | *Test Mode 1* | *Mode-1* | |
| 2 | *Test Mode 2* | *Mode-2* | |
| 3 | *Test Mode 3* | *Mode-3* | Reserved |
| 4 | *Start Stop Test* | *StartTest* | |
| 5 | *Software Xoff* | *SXoff* | |
| 6 | *Cascade* | *FPGA_CASCADE* | |
| 7 | *Enable Readout* | *FPGA_EN_ROUT* | |

#### *3.2.8.5.1 Mode Bits*

| Mode bit 2 | Mode bit 1 | Mode bit 0 | Descriptive Name |
|---|---|---|---|
| 0 | 0 | 0 | No Test |
| 0 | 0 | 1 | *Pseudo Random Pattern -32K* |
| 0 | 1 | 0 | *Memory to Memory Test (Bypass)- 32K* |
| 0 | 1 | 1 | *Read Back and Compare Test - 32 K* |
| 1 | 0 | 1 | *Pseudo Random Pattern Forever* |
| 1 | 1 | 0 | *Bypass Forever* |
| 1 | 1 | 1 | *Read Back and Compare Test Forever* |
| 1 | 0 | 0 | *S-Link Test* |

#### **3.2.8.*5.1.1 Pseudo Random Pattern***

When selected, pseudo-random patterns are generated internally as the data source, and automatically checked.

### 3.2.8.5.1.2 *Bypass Readout Logic*

When selected the data source is the DPRAM's, the transmitted data is written into the Sink DPRAM's

***Read back test***

The same data is written into the source and sink DPRAM's, and automatically checked.

### 3.2.8.5.2 *Start/Stop Test*

**Bit 4**

When a 1 is written to this bit it will start the test sequence.

| | |
|---|---|
| 0 | Stops the test sequence |
| 1 | Starts the test sequence |

This bit will be combined (OR) with a broadcast start signal which will be received from the TTC system and decoded by the TTCrx chip (Brcst[7:6])**.**

| Brcst[7] | Brcst[6] | Function |
|---|---|---|
| 0 | 0 | stop |
| 0 | 1 | start |

### *3.2.8.5.3 Software Xoff (specific for the ROD)*

**Bit 5**

| | |
|---|---|
| 0 | when this bit is set to one Xoff will be generated in software |
| 1 | when this bit is set to zero only the hardware Xoff is active |

### *3.2.8.5.4 Cascade (specific for testing the ROD function on the Serialising ASIC)*

**Bit 6**

| | |
|---|---|
| 0 | when this bit is set to zero, only data from one "serial ASIC" will be transmitted. |
| 1 | when this bit is set to one, data from two "serial ASIC"s will be cascaded and transmitted |

### *3.2.8.5.5 Enable Read out (specific for ROD tests)*

**BIT 7**

| | |
|---|---|
| 0 | disables readout. |
| 1 | enables readout |

### *3.2.8.6 Mother Status Register*

This is a read-only register.

| Bit | Descriptive Name | Signal name | |
|---|---|---|---|
| 0 (LSB) | *Data Buffer 1 Full* | *DB1FF* | |
| 1 | *Data Buffer 2 Full* | *DB2FF* | |
| 2 | *Data Buffer 3 Full* | *DB3FF* | |
| 3 | *Data Buffer 4 Full* | *DB4FF* | |
| 4 | *Data Buffer 5 Full* | *DB5FF* | |
| 5 | *Data Buffer 6 Full* | *DB6FF* | |
| 6 | *Data Buffer 7 Full* | *DB7FF* | |
| 7 | *Data Buffer 8 Full* | *DB8FF* | |
| 8 | *Data Buffer 9 Full* | *DB9FF* | |
| 9 | *Data Buffer 10 Full* | *DB10FF* | |
| 10 | *FPGA 1 Loaded* | *Prom1Done* | |
| 11 | *FPGA 2 Loaded* | *Prom2Done* | |
| 12 | *FPGA 3 Loaded* | *Prom3Done* | |
| 13 | *FPGA 4 Loaded* | *Prom4Done* | |
| 14 | *FPGA 5 Loaded* | *Prom5Done* | |
| 15 | *FPGA 6 Loaded* | *Prom6Done* | |
| 16 | *FPGA 7 Loaded* | *Prom7Done* | |
| 17 | *FPGA 8 Loaded* | *Prom8Done* | |
| 18 | *FPGA 9 Loaded* | *Prom9Done* | |
| 19 | *FPGA 10 Loaded* | *Prom10Done* | |
| 20 | *Module Status* | *Start/Stop* | |
| 21 | *TTC Status* | *BroadcastStart* | |
| 22 | *TTC Ready* | *TTCReady* | |
| 23 | | | |
| 24-31 | | | Not used |

**3.2.8.*6.1Data* Buffer Full**

**Bit 0 - 9**

0 Data buffer not full
1 Data buffer full

**3.2.8.*6.2***

**Bits 10 -19**

0 FPGA ‘n’ not loaded
1 FPGA ‘n’ successfully loaded

**3.2.8.6.3**

**Bit 20**

| | |
|---|---|
| 0 | Testing stopped |
| 1 | Testing started |

**3.2.8.6.4**

**Bit 21**

| | |
|---|---|
| 0 | Testing stopped via TTC broadcast |
| 1 | Testing started via TTC broadcast |

**3.2.8.*6.3***

**Bit 22**

| | |
|---|---|
| 0 | TTCrx is not ready |
| 1 | TTCrx is ready |

**3.2.8.6.4**

**Bit 23 - 31** Not used

### *3.2.8.7 Daughter Card Serial number*

Bits 0-15 is reserved for the daughter card 1 and bits (16-31) is reserved for the daughter card 2

| Register Bits | Assignment | Description |
|---|---|---|
| 0-4 (16-20) | Serial number | an unique number assigned to each module |
| 5-7 (21-23 | zero | Set to zero |
| 8-12 (24-28) | zero | Set to zero |
| 13-15 (28-31) | zero | Set to zero |

### *3.2.8.8* **Daughter Control Register**

Bits 0 to 15 are reserved for daughter board 1. Bits 16 to 31 are reserved for daughter board 2 and has the same bit definition as for bits 0 to 15 (3.2.8.7.1)

#### *3.2.8.8.1* **LVDSSYNC (Controls G-Link Rx Equiliser)**
**Bits 0-3 (16-19)**

| | |
|---|---|
| 0 | Normal running |
| 1 | PLL synchronisation mode * |

* LVDS (SYNC) hold these bits high for a minimum of 1024, 40 MHz clock cycles (one bit per pair of chips).

**3.2.8.8.2 DIV0**

**Bits 4-(20)**

0 set 0 on DIV0 of G-links
1 set 1 on DIV0 of G-links

**3.2.3.8.3 Bits 5-7 (21-23) not used**

***3.2.8.8.4*** **LVDS PWDN**

**Bit 8 (24)**

0 writing a 0 takes the signal low
1 writing a 1 takes the signal high
(Hold this signal low for 1 micro second to initialise the LVDS chips)

***3.2.8.8.5***

**Bits 9 (25) (REN/DEN)**

0 Tri-states the outputs on the LVDS chips
1 Data enabled

***3.2.8.8.6***

**Bits 10-15 (26-31)**

These bits are not defined

***3.2.8.9*** **Daughter Status register**

Bits 0 to 15 are reserved for daughter board 1. Bits 16 to 31 are reserved for daughter board 2 and has the same bit definition as for bits 0 to 15 (3.2.8.8.1)

***3.2.8.9.1*** **Links Locked**

**Bits 0 - 7 (16 - 23)**

0 Links locked
1 Links not locked

* LVDS uses eight bits and G-links uses the first four bits per daughter board

***3.2.8.9.2***

**Bits 8-15 (24-31)** Not used

### *3.2.8.10 Timing_Reg*

**Bits 0 - 4** Adjust the phase of the 40 MHz clock, clock40Des 1 in 1 ns steps.
**Bits 5 - 9** Adjust the phase of the 40 MHz clock, clock40Des 2 in 1 ns steps
**Bits 10 - 15** Not defined.
**Bits 16 - 17** Two bits for FPGAs 1-4, for one of three clock selection
**Bits 18 - 19** Two bits for FPGAs 5-8, for one of three clock selection
**Bits 20 - 21** Two bits for FPGA (S), for one of three clock selection.
**Bits 22 - 23** Not used.
**Bits 24 - 31** Not used

Note: bits 0-9 are only used with a clock source other than the TTC.

See Appendix A for timing Scheme

### *3.2.8.11 Offset Register*

**Bits 0 - 6**
The function of this register is to provide a latency offset to pick out the correct data from the dual port memory within the FPGAs which implements the Serialiser ASIC logic to test the ROD module

### *3.2.8.12 Pulse Register*

| Bit | Descriptive Name | Signal name | |
|---|---|---|---|
| 0 (LSB) | *FPGA Reset* | *GLReset* | Pulse (200ns) |
| 1 | *TTC Reset* | *TTCReset* | Pulse (200ns) |
| 2 | *Reset daughter card 1* | *DC1-RESET* | Pulse (200ns) |
| 3 | *Reset daughter card 2* | *DC2-RESET* | Pulse (200ns) |
| 4 | *Reset Address Counters* | *RS_Count* | Pulse (200ns) |
| 5 | *Reset S-Link(D) Counter* | *RS-S-Count* | Pulse (200ns) |

#### 3.2.8.*12.1 Global Reset*

**Bit 0**

When a 1 is written to this bit, a single pulse will reset the DSS module to a known power-up state. *Global Reset* is always read 0, and writing 0 has no effect.

The same effect can be produced using the VME *System Reset**.

0 Read value, no effect on writing
1 Resets the DSS module to the initial power-up state

### 3.2.8.*12.2 TTC Reset*

**Bit 1**

When a 1 is written to this bit, a single pulse will reset the TTCrx chip to power-up state. *TTC reset* is always read 0, and writing 0 has no effect.

| | |
|---|---|
| 0 | Read value, no effect on writing |
| 1 | Resets the TTCrx chip |

### 3.2.8.*12.3 Reset Daughter Card 1,2*

**Bit 2, 3**

When a 1 is written to this bit, a single pulse will reset the G-Link chips to power-up state. *G-Link reset* is always read 0, and writing 0 has no effect.

| | |
|---|---|
| 0 | Read value, no effect on writing |
| 1 | Resets the G-Link chips |

### *3.2.8.13 Bit Error register (FIFO Buffer Empty flag register)*

***Bits 0-7***
Indicates the bit error flag from the data FPGAs when the FPGAs are used in the destination. When the data FPGAs are used as source FPGAs to test the "Serialising ASIC" read-out function these bits will indicate FIFO buffer empty flags. Bits 0 to 7 corresponding to FPGA 1 to 8.

### *3.2.8.14 VME Revision*
Specifies the current version loaded into the VME CPLD.

| | |
|---|---|
| Bits 31-24 | Version (Starts at 01) |
| Bits 23-16 | Function code. |
| Bits 15-0 | "2414" for DSS. |

### *3.2.8.15 Program_Reg*
This register is used to program the FPGAs as well the EEPROMs via the VME

| | |
|---|---|
| Bit 0 | Serial data to FPGAs and EEPROMs (Din) |
| Bits 15-1 | Reserved (read back as zero) |
| Bit 16 | Sel-1 |
| Bit 17 | Sel-2 |
| Bit 18 | Sel-3 |
| Bit 19 | Sel-4 |
| Bit 20 | Writing a one will generate a clock for the FPGA/EEPROM |
| Bit 21 | Reset |
| Bit 22 | Program |
| Bit 23 | Monitor INIT signal |
| Bit 24 | Monitor done signal |
| Bits 31-25 | Reserved (read back as zero) |

The Sel lines will select one of the devices for programming by selecting Ser_En or CE line of the appropriate FPGAs or the EEPROMs.

| Sel[3:0] | Program Block |
|---|---|
| 0001 | FPGA 1-4 via Xchecker |
| 0010 | FPGA 5-8 via Xchecker |
| 0011 | SLINK Source FPGA via Xchecker |
| 0100 | SLINK Destination FPGA via Xchecker |
| 0101 | FPGA 1-4 via VME |
| 0110 | FPGA 5-8 via VME |
| 0111 | SLINK Source FPGA via VME |
| 1000 | SLINK Destination FPGA via VME |
| 1001 | EEPROM on Daughter card 1 |
| 1010 | EEPROM on Daughter card 2 |

#### *3.2.8.16 FPGA_Reg_A*

**Bits 11-0**
Bunch count number available on each of the FPGAs when it is implementing the serialiser ASIC logic (Source FPGA).

**Bits 15-0 (Glink)**
**Bits 31-16, 15-0 (LVDS)**
Bit error counter (Sink FPGA)

#### *3.2.8.17 FPGA_Reg_B*

**Bits 19-0 (Glink)**
**Bits 25-16, 9-0 (LVDS)**

Pseudo Seed register for Pseudo Random data generator.

#### *3.2.8.18 FPGA_Reg_C*

**Bits 19-0 (Glink)**
**Bits 25-16, 9-0 (LVDS)**

Last word in Error. (Sink only)

#### *3.2.8.19 Address Counters*

**Bits 31-0**

Indicates the address location of the dual-port RAMs (Source)
Address where the last error occurred. (Sink)

### *3.2.8.20 FPGA Revision Registers*

**Bits 31-24** Revision number (Starts at 01)
**Bits 23-16** Function code.
**Bits 15-0** "2414" (used with the DSS motherboard, therefore this should match with the DSS mother ID).

#### *3.2.8.20.1 Function Codes (Bits 23-16)*

| Code (Binary) | PLD function |
|---|---|
| "00010000" | GLINK SOURCE |
| "00010001" | GLINK SINK |
| "00010010" | LVDS SOURCE |
| "00010011" | LVDS SINK |
| "00100000" | VME TYPE |
| "00010100" | SLINK SOURCE |
| "00010101" | SLINK DESTINATION |

### *3.2.8.21 Registers for S-Link*

#### *3.2.8.21.1 S-Link Source Control Register (Slink_S_CR)*

**Bit 4** UTEST

#### *3.2.8.21.2 S-Link Source Status Register (Slink_S_SR)*

**Bits 3-0** LRL

#### *3.2.8.21.3 S-Link Destination FIFO (Slink_FIFO)*

**Bits 15-0** copies the address of the dual-port memory (S-Link associated) when a S-Link control word is received. Hence this FIFO will indicate the addresses of the beginning of a fragment (BOF00000Hex) and end of fragment (EOF00000Hex) of a S-Link frame written on to the dual-port RAM via S-Link.

**Bit 16** status of LDERR.

**Bit 17** will be '1' when you read the last word from the FIFO.

#### *3.2.8.21.4 S-Link Destination Control Register (Slink_D_CR)*

**Bits 3-0** URL
**Bit 4** UTDO

### *3.3* DSS Daughter Boards.

As shown in figure 6, a selection of daughter boards such as G-link transmitter and receivers, LVDS serialiser and deserialiser and parallel LVDS are possible.
Many others are also possible to satisfy future test requirements of ASICs, MCMs and modules.

The motherboard can be configured by the daughter modules to be either all source modules or all sink modules or half-and-half, except for the S-Link cards. Since the S-Link cards are hard coded with a key pin, only one S-Link source and one S-Link destination card is allowed on the motherboard.

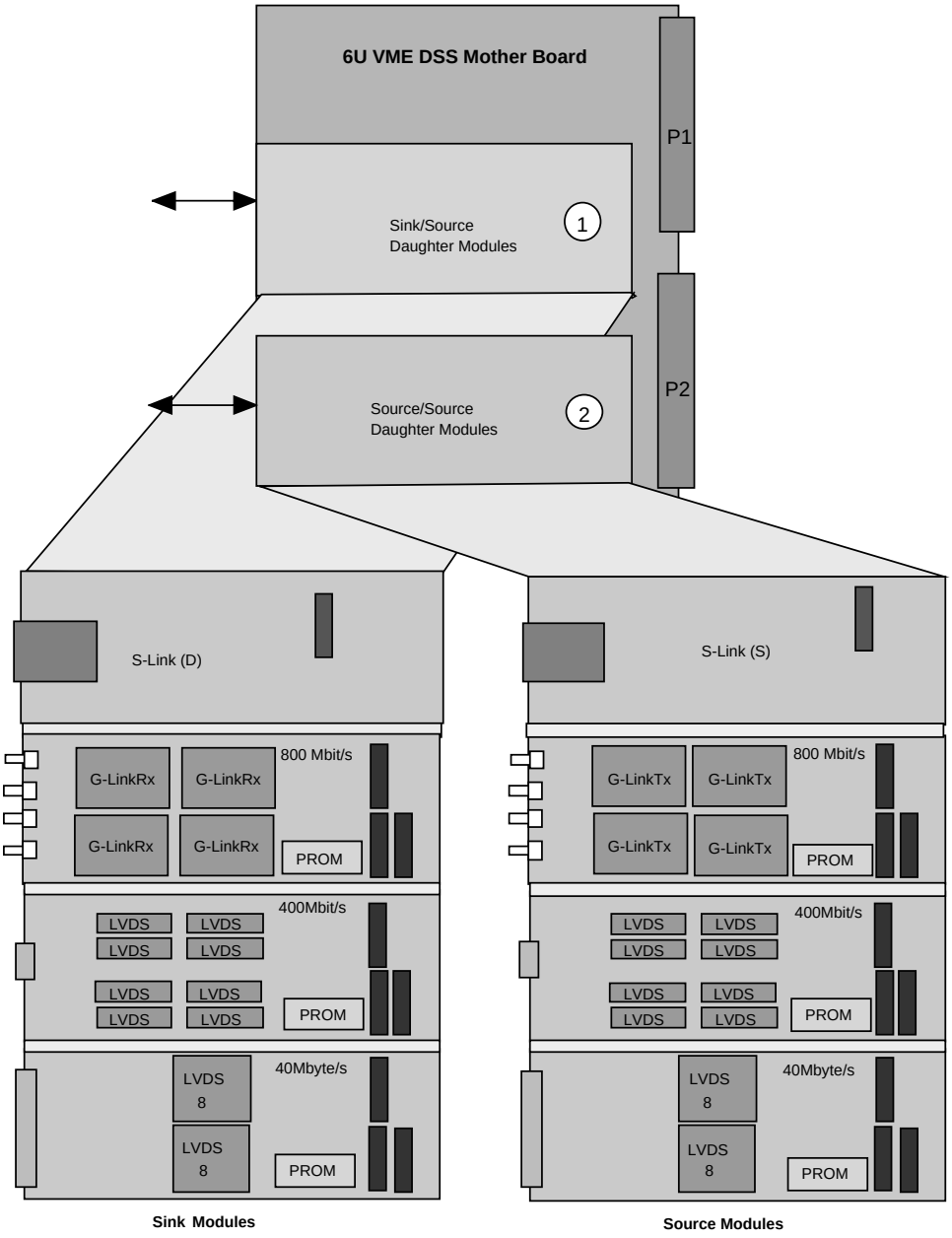



Figure 6. DSS Daughter Card Options

When a daughter board is plugged onto the mother board, the mother board PROM handling the daughter card data, will be automatically disabled and the PROM on the daughter board will automatically configure the mother board to be source or sink module. Separate FPGAs will handle the data from the S-Link daughter cards

### 3.3.1 Daughter Board Standard

The daughter board designs must comply with the IEEE P1386/Draft 2.0, 4 April-1995, standard for a Common Mezzanine Card (CMC) family.
The connector definitions and the physical description of the boards are given below. Figure 7 shows the generic daughter boards and the connector positions.

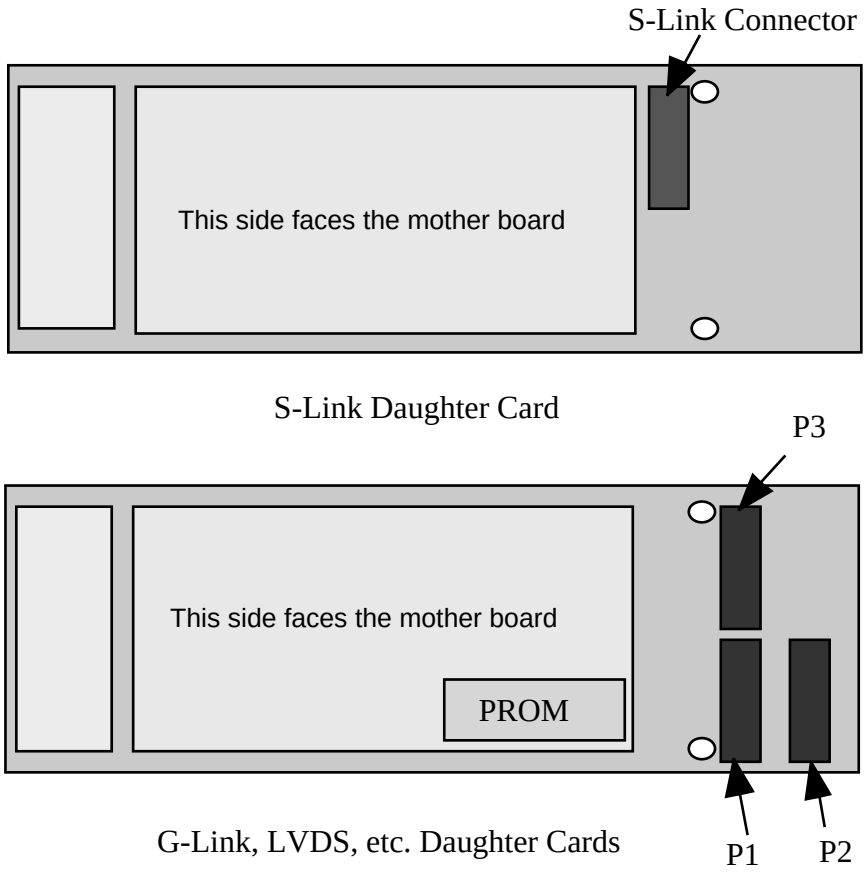



Figure 7 . Daughter board view facing the mother board

The connectors used in these modules will be: (10 mm stand-off)
1. Plug (P) (Molex 53483-0649) on the daughter boards
2. Socket (J) (Molex 52763-0649) on the motherboards

### 3.3.2 Connector Definitions.

#### 3.3.2.1 S-Link Source Card (LSC) Connector

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | LRL3 | LRL2 | 2 |
| 3 | VCC | LRL1 | 4 |
| 5 | VCC | LRL0 | 6 |
| 7 | LDOWN# | GROUND | 8 |
| 9 | GROUND | LFF# | 10 |
| 11 | UCLK | GROUND | 12 |
| 13 | GROUND | UWEN# | 14 |
| 15 | URESET# | GROUND | 16 |
| 17 | UDW1 | UTEST# | 18 |
| 19 | UCTRL# | UDW0 | 20 |
| 21 | UD31 | VCC | 22 |
| 23 | GROUND | UD30 | 24 |
| 25 | UD29 | UD28 | 26 |
| 27 | UD27 | GROUND | 28 |
| 29 | UD26 | UD25 | 30 |
| 31 | GROUND | UD24 | 32 |
| 33 | UD23 | UD22 | 34 |
| 35 | UD21 | GROUND | 36 |
| 37 | UD20 | UD19 | 38 |
| 39 | VCC | UD18 | 40 |
| 41 | UD17 | UD16 | 42 |
| 43 | UD15 | GROUND | 44 |
| 45 | UD14 | UD13 | 46 |
| 47 | GROUND | UD12 | 48 |
| 49 | UD11 | UD10 | 50 |
| 51 | UD9 | VCC | 52 |
| 53 | UD8 | UD7 | 54 |
| 55 | GROUND | UD6 | 56 |
| 57 | UD5 | UD4 | 58 |
| 59 | UD3 | GROUND | 60 |
| 61 | UD2 | UD1 | 62 |
| 63 | VCC | UD0 | 64 |

Table 1. S-Link Source Card pin-out

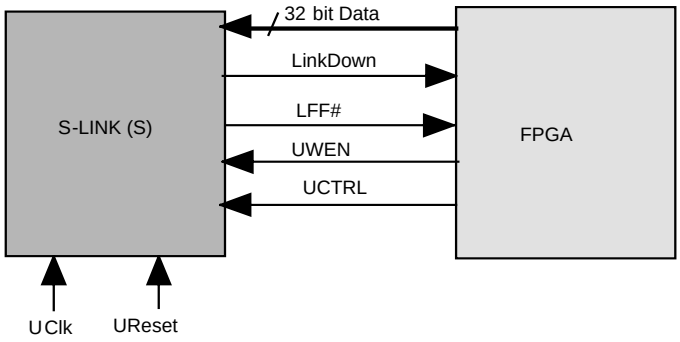



Figure 8. Interface between the S-Link Source and the FPGA

### 3.3.2.2. G-Link Source Board Connector P1

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | GLinkRESET* (C) | -12V | 2 |
| 3 | GROUND | PLL_LOCKED-A (S) | 4 |
| 5 | DBID-1 | PLL_LOCKED-B (S) | 6 |
| 7 | Busmode1# | +5V | 8 |
| 9 | DBID-2 | PLL_LOCKED-C (S) | 10 |
| 11 | GROUND | PLL_LOCKED-D (S) | 12 |
| 13 | | GROUND | 14 |
| 15 | GROUND | GLinkDAVA* (F) | 16 |
| 17 | DBID-3 | +5V | 18 |
| 19 | V(I/O)-1 | GLinkDAVB* (F) | 20 |
| 21 | | GLinkDAVC* (F) | 22 |
| 23 | | GROUND | 24 |
| 25 | GROUND | GLinkDAVD* (F) | 26 |
| 27 | | DBID-4 | 28 |
| 29 | | +5V | 30 |
| 31 | V(I/O)-1 | DBID-5 | 32 |
| 33 | DC_DATA_D0 | GROUND | 34 |
| 35 | GROUND | DC_DATA_D1 | 36 |
| 37 | DC_DATA_D2 | +5V | 38 |
| 39 | GROUND | DC_DATA_D3 | 40 |
| 41 | DC_DATA_D4 | DC_DATA_D5 | 42 |
| 43 | DC_DATA_D6 | GROUND | 44 |
| 45 | V(I/O)-1 | DC_DATA_D7 | 46 |
| 47 | DC_DATA_D8 | DC_DATA_D9 | 48 |
| 49 | DC_DATA_D10 | +5V | 50 |
| 51 | GROUND | DC_DATA_D11 | 52 |
| 53 | DC_DATA_D12 | DC_DATA_D13 | 54 |
| 55 | DC_DATA_D14 | GROUND | 56 |
| 57 | V(I/O)-1 | DC_DATA_D15 | 58 |
| 59 | DC_DATA_D16 | DC_DATA_D17 | 60 |
| 61 | DC_DATA_D18 | +5V | 62 |
| 63 | GROUND | DC_DATA_D19 | 64 |

Table 2. G-Link Source Board Connector P1 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

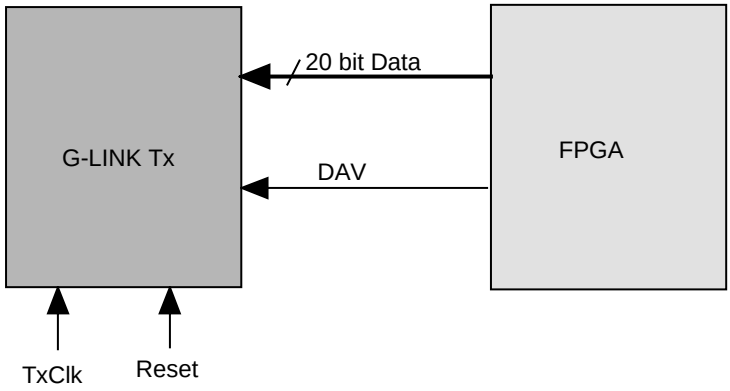



Figure 9. Interface between the G-Link and the FPGAs

### 3.3.2.3. G-Link Source Board Connector P2

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | +12V | DisMotherProm1 | 2 |
| 3 | | DisMotherProm2 | 4 |
| 5 | PromDONE | GROUND | 6 |
| 7 | GROUND | PromDATA | 8 |
| 9 | PromINIT | DIV0 (C) | 10 |
| 11 | Busmode2# | +3.3V | 12 |
| 13 | | Busmode3# | 14 |
| 15 | +3.3V | Busmode4# | 16 |
| 17 | | GROUND | 18 |
| 19 | GLinkStrbA | GLinkStrbB | 20 |
| 21 | GROUND | | 22 |
| 23 | GLinkStrbC | +3.3V | 24 |
| 25 | | Ser_En (C) | 26 |
| 27 | +3.3V | GLinkStrbD | 28 |
| 29 | DC_DATA_C0 | GROUND | 30 |
| 31 | DC_DATA_C2 | Mod20Sel (C) | 32 |
| 33 | GROUND | DC_DATA_C1 | 34 |
| 35 | PromCCLK | +3.3V | 36 |
| 37 | GROUND | DC_DATA_C3 | 38 |
| 39 | DC_DATA_C4 | GROUND | 40 |
| 41 | +3.3V | DC_DATA_C5 | 42 |
| 43 | DC_DATA_C6 | GROUND | 44 |
| 45 | DC_DATA_C8 | DC_DATA_C7 | 46 |
| 47 | GROUND | DC_DATA_C9 | 48 |
| 49 | DC_DATA_C10 | +3.3V | 50 |
| 51 | DC_DATA_C12 | DC_DATA_C11 | 52 |
| 53 | +3.3V | DC_DATA_C13 | 54 |
| 55 | DC_DATA_C14 | GROUND | 56 |
| 57 | DC_DATA_C16 | DC_DATA_C15 | 58 |
| 59 | GROUND | DC_DATA_C17 | 60 |
| 61 | DC_DATA_C18 | +3.3V | 62 |
| 63 | GROUND | DC_DATA_C19 | 64 |

Table 3. G-Link Source Board Connector P2 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

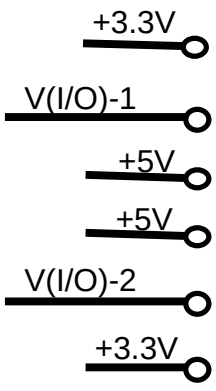
Note 1. Busmode [4:2]# signals are driven by the motherboard, Busmode 1# is returned by the daughter card to indicate presence of the card. These signals are not used in the G-Link and LVDS daughter card designs.
2. User Defined pins are spare pins for future use.

### 3.3.2.4. G-Link Source Board Connector P3

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | DC_DATA_A0 | GROUND | 2 |
| 3 | GROUND | DC_DATA_A1 | 4 |
| 5 | DC_DATA_A2 | DC_DATA_A3 | 6 |
| 7 | DC_DATA_A4 | GROUND | 8 |
| 9 | V(I/O)-2 | DC_DATA_A5 | 10 |
| 11 | DC_DATA_A6 | DC_DATA_A7 | 12 |
| 13 | DC_DATA_A8 | GROUND | 14 |
| 15 | GROUND | DC_DATA_A9 | 16 |
| 17 | DC_DATA_A10 | DC_DATA_A11 | 18 |
| 19 | DC_DATA_A12 | GROUND | 20 |
| 21 | V(I/O)-2 | DC_DATA_A13 | 22 |
| 23 | DC_DATA_A14 | DC_DATA_A15 | 24 |
| 25 | DC_DATA_A16 | GROUND | 26 |
| 27 | GROUND | DC_DATA_A17 | 28 |
| 29 | DC_DATA_A18 | DC_DATA_A19 | 30 |
| 31 | DC_DATA_B0 | GROUND | 32 |
| 33 | GROUND | DC_DATA_B1 | 34 |
| 35 | DC_DATA_B2 | DC_DATA_B3 | 36 |
| 37 | DC_DATA_B4 | GROUND | 38 |
| 39 | V(I/O)-2 | DC_DATA_B5 | 40 |
| 41 | DC_DATA_B6 | DC_DATA_B7 | 42 |
| 43 | DC_DATA_B8 | GROUND | 44 |
| 45 | GROUND | DC_DATA_B9 | 46 |
| 47 | DC_DATA_B10 | DC_DATA_B11 | 48 |
| 49 | DC_DATA_B12 | GROUND | 50 |
| 51 | GROUND | DC_DATA_B13 | 52 |
| 53 | DC_DATA_B14 | DC_DATA_B15 | 54 |
| 55 | DC_DATA_B16 | GROUND | 56 |
| 57 | V(I/O)-2 | DC_DATA_B17 | 58 |
| 59 | DC_DATA_B18 | DC_DATA_B19 | 60 |
| 61 | Spare (C) | GROUND | 62 |
| 63 | GROUND | | 64 |

Table 4. G-Link Source Board Connector P3 pin-out

Note: The V(I/O) pins on P1 and P3 should be tracked as shown below for selecting additional voltage pins if necessary



### 3.3.2.5. LVDS (400 Mbit/s) Source Board Connector P1

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | DC RESET | -12V | 2 |
| 3 | GROUND | | 4 |
| 5 | DBID-1 | | 6 |
| 7 | Busmode1# | +5V | 8 |
| 9 | DBID-2 | | 10 |
| 11 | GROUND | | 12 |
| 13 | | GROUND | 14 |
| 15 | GROUND | | 16 |
| 17 | DBID-3 | +5V | 18 |
| 19 | V(I/O)-1 | | 20 |
| 21 | | | 22 |
| 23 | | GROUND | 24 |
| 25 | GROUND | | 26 |
| 27 | | DBID-4 | 28 |
| 29 | | +5V | 30 |
| 31 | V(I/O)-1 | DBID-5 | 32 |
| 33 | DC_DATA_D0 | GROUND | 34 |
| 35 | GROUND | DC_DATA_D1 | 36 |
| 37 | DC_DATA_D2 | +5V | 38 |
| 39 | GROUND | DC_DATA_D3 | 40 |
| 41 | DC_DATA_D4 | DC_DATA_D5 | 42 |
| 43 | DC_DATA_D6 | GROUND | 44 |
| 45 | V(I/O)-1 | DC_DATA_D7 | 46 |
| 47 | DC_DATA_D8 | DC_DATA_D9 | 48 |
| 49 | DC_DATA_D10 | +5V | 50 |
| 51 | GROUND | DC_DATA_D11 | 52 |
| 53 | DC_DATA_D12 | DC_DATA_D13 | 54 |
| 55 | DC_DATA_D14 | GROUND | 56 |
| 57 | V(I/O)-1 | DC_DATA_D15 | 58 |
| 59 | DC_DATA_D16 | DC_DATA_D17 | 60 |
| 61 | DC_DATA_D18 | +5V | 62 |
| 63 | GROUND | DC_DATA_D19 | 64 |

Table 5. LVDS (400Mbit/s) Source Board Connector P1 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

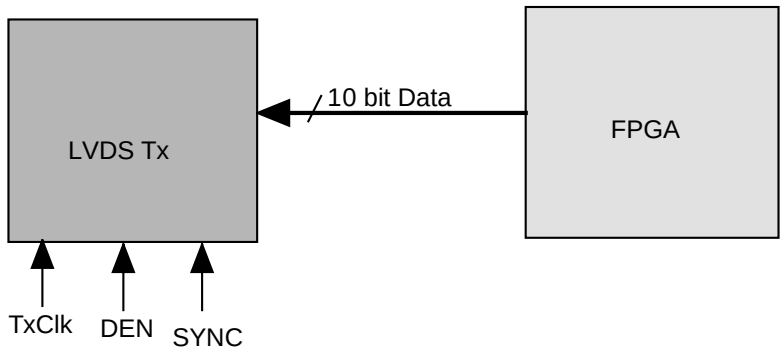



Figure 10. Interface between the LVDS Serialisers and the FPGAs

### 3.3.2.6. LVDS (400 Mbit/s) Source Board Connector P2

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | +12V | DisMotherProm1 | 2 |
| 3 | LVDS-PWDN* (C) | DisMotherProm2 | 4 |
| 5 | PromDONE | GROUND | 6 |
| 7 | GROUND | PromDATA | 8 |
| 9 | PromINIT | | 10 |
| 11 | Busmode2# | +3.3V | 12 |
| 13 | LVDSSYNCA (C) | Busmode3# | 14 |
| 15 | +3.3V | Busmode4# | 16 |
| 17 | LVDSSYNCB (C) | GROUND | 18 |
| 19 | TCLKA | TCLKB | 20 |
| 21 | GROUND | LVDSSYNCC (C) | 22 |
| 23 | TCLKC | +3.3V | 24 |
| 25 | LVDSSYNCD (C) | Ser_En | 26 |
| 27 | +3.3V | TCLKD | 28 |
| 29 | DC_DATA_C0 | GROUND | 30 |
| 31 | DC_DATA_C2 | | 32 |
| 33 | GROUND | DC_DATA_C1 | 34 |
| 35 | PromCCLK | +3.3V | 36 |
| 37 | GROUND | DC_DATA_C3 | 38 |
| 39 | DC_DATA_C4 | GROUND | 40 |
| 41 | +3.3V | DC_DATA_C5 | 42 |
| 43 | DC_DATA_C6 | GROUND | 44 |
| 45 | DC_DATA_C8 | DC_DATA_C7 | 46 |
| 47 | GROUND | DC_DATA_C9 | 48 |
| 49 | DC_DATA_C10 | +3.3V | 50 |
| 51 | DC_DATA_C12 | DC_DATA_C11 | 52 |
| 53 | +3.3V | DC_DATA_C13 | 54 |
| 55 | DC_DATA_C14 | GROUND | 56 |
| 57 | DC_DATA_C16 | DC_DATA_C15 | 58 |
| 59 | GROUND | DC_DATA_C17 | 60 |
| 61 | DC_DATA_C18 | +3.3V | 62 |
| 63 | GROUND | DC_DATA_C19 | 64 |

Table 6. LVDS (400Mbit/s) Source Board Connector P2 pin-out

(S) -Status Register
(F) - Data FPGA
(C) - Control Register

Note 1. Busmode [4:2]# signals are driven by the motherboard, Busmode 1# is returned by the daughter card to indicate presence of the card. These signals are not used in the G-Link and LVDS daughter card designs.
2. User Defined pins are spare pins for future use.

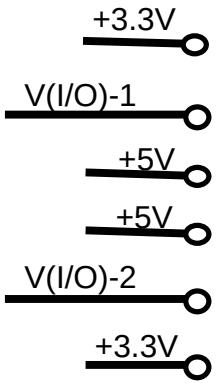
### 3.3.2.7 LVDS (400 Mbit/s) Source Board Connector P3

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | DC_DATA_A0 | GROUND | 2 |
| 3 | GROUND | DC_DATA_A1 | 4 |
| 5 | DC_DATA_A2 | DC_DATA_A3 | 6 |
| 7 | DC_DATA_A4 | GROUND | 8 |
| 9 | V(I/O)-2 | DC_DATA_A5 | 10 |
| 11 | DC_DATA_A6 | DC_DATA_A7 | 12 |
| 13 | DC_DATA_A8 | GROUND | 14 |
| 15 | GROUND | DC_DATA_A9 | 16 |
| 17 | DC_DATA_A10 | DC_DATA_A11 | 18 |
| 19 | DC_DATA_A12 | GROUND | 20 |
| 21 | V(I/O)-2 | DC_DATA_A13 | 22 |
| 23 | DC_DATA_A14 | DC_DATA_A15 | 24 |
| 25 | DC_DATA_A16 | GROUND | 26 |
| 27 | GROUND | DC_DATA_A17 | 28 |
| 29 | DC_DATA_A18 | DC_DATA_A19 | 30 |
| 31 | DC_DATA_B0 | GROUND | 32 |
| 33 | GROUND | DC_DATA_B1 | 34 |
| 35 | DC_DATA_B2 | DC_DATA_B3 | 36 |
| 37 | DC_DATA_B4 | GROUND | 38 |
| 39 | V(I/O)-2 | DC_DATA_B5 | 40 |
| 41 | DC_DATA_B6 | DC_DATA_B7 | 42 |
| 43 | DC_DATA_B8 | GROUND | 44 |
| 45 | GROUND | DC_DATA_B9 | 46 |
| 47 | DC_DATA_B10 | DC_DATA_B11 | 48 |
| 49 | DC_DATA_B12 | GROUND | 50 |
| 51 | GROUND | DC_DATA_B13 | 52 |
| 53 | DC_DATA_B14 | DC_DATA_B15 | 54 |
| 55 | DC_DATA_B16 | GROUND | 56 |
| 57 | V(I/O)-2 | DC_DATA_B17 | 58 |
| 59 | DC_DATA_B18 | DC_DATA_B19 | 60 |
| 61 | Spare (C) | GROUND | 62 |
| 63 | GROUND | LVDS-DEN | 64 |

Table 7. LVDS (400Mbit/s) Source Board Connector P3 pin-out

The data bits are defined as 0 to 19 and the corresponding controls are defined as:
L for bits 0 - 9 and H for bits 10 - 19.

Note: The V(I/O) pins on P1 and P3 should be tracked as shown below for selecting additional voltage pins if necessary



### 3.3.2.8 S-Link Destination Board (LDC)

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | URL3 | URL2 | 2 |
| 3 | VCC | URL1 | 4 |
| 5 | LDERR# | URL0 | 6 |
| 7 | LDOWN# | GROUND | 8 |
| 9 | GROUND | UXOFF# | 10 |
| 11 | LCLK | GROUND | 12 |
| 13 | GROUND | LWEN# | 14 |
| 15 | URESET# | GROUND | 16 |
| 17 | UDW1 | UTD0# | 18 |
| 19 | LCTRL# | UDW0 | 20 |
| 21 | LD31 | VCC | 22 |
| 23 | GROUND | LD30 | 24 |
| 25 | LD29 | LD28 | 26 |
| 27 | LD27 | GROUND | 28 |
| 29 | LD26 | LD25 | 30 |
| 31 | GROUND | LD24 | 32 |
| 33 | LD23 | LD22 | 34 |
| 35 | LD21 | GROUND | 36 |
| 37 | LD20 | LD19 | 38 |
| 39 | VCC | LD18 | 40 |
| 41 | LD17 | LD16 | 42 |
| 43 | LD15 | GROUND | 44 |
| 45 | LD14 | LD13 | 46 |
| 47 | GROUND | LD12 | 48 |
| 49 | LD11 | LD10 | 50 |
| 51 | LD9 | VCC | 52 |
| 53 | LD8 | LD7 | 54 |
| 55 | GROUND | LD6 | 56 |
| 57 | LD5 | LD4 | 58 |
| 59 | LD3 | GROUND | 60 |
| 61 | LD2 | LD1 | 62 |
| 63 | VCC | LD0 | 64 |

Table 8. S-Link Destination Board pin-out

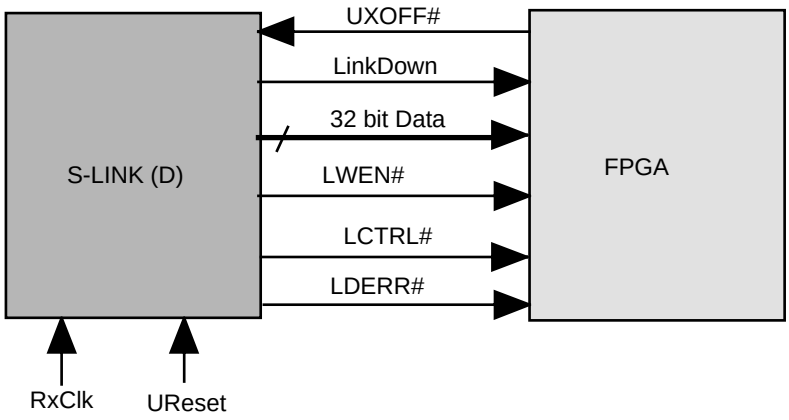



Figure 11. Interface between the S-Link Destination Board and the FPGA

### 3.3.2.9 G-Link Destination Board Connector P1

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | GLinkRESET* (C) | -12V | 2 |
| 3 | GROUND | GLinkRdyA* (S) | 4 |
| 5 | DBID-1 | GLinkRdyB* (S) | 6 |
| 7 | Busmode1# | +5V | 8 |
| 9 | DBID-2 | GLinkRdyC* (S) | 10 |
| 11 | GROUND | GLinkRdyD* (S) | 12 |
| 13 | GLinkRefCLK | GROUND | 14 |
| 15 | GROUND | GLinkDAVA* (F) | 16 |
| 17 | DBID-3 | +5V | 18 |
| 19 | V(I/O)-1 | GLinkDAVB* (F) | 20 |
| 21 | GLinkErrA | GLinkDAVC* (F) | 22 |
| 23 | GLinkErrB | GROUND | 24 |
| 25 | GROUND | GLinkDAVD* (F) | 26 |
| 27 | GLinkErrC | DBID-4 | 28 |
| 29 | GLinkErrD | +5V | 30 |
| 31 | V(I/O)-1 | DBID-5 | 32 |
| 33 | DC_DATA_D0 | GROUND | 34 |
| 35 | GROUND | DC_DATA_D1 | 36 |
| 37 | DC_DATA_D2 | +5V | 38 |
| 39 | GROUND | DC_DATA_D3 | 40 |
| 41 | DC_DATA_D4 | DC_DATA_D5 | 42 |
| 43 | DC_DATA_D6 | GROUND | 44 |
| 45 | V(I/O)-1 | DC_DATA_D7 | 46 |
| 47 | DC_DATA_D8 | DC_DATA_D9 | 48 |
| 49 | DC_DATA_D10 | +5V | 50 |
| 51 | GROUND | DC_DATA_D11 | 52 |
| 53 | DC_DATA_D12 | DC_DATA_D13 | 54 |
| 55 | DC_DATA_D14 | GROUND | 56 |
| 57 | V(I/O)-1 | DC_DATA_D15 | 58 |
| 59 | DC_DATA_D16 | DC_DATA_D17 | 60 |
| 61 | DC_DATA_D18 | +5V | 62 |
| 63 | GROUND | DC_DATA_D19 | 64 |

Table 9. G-Link Destination Board Connector P1 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

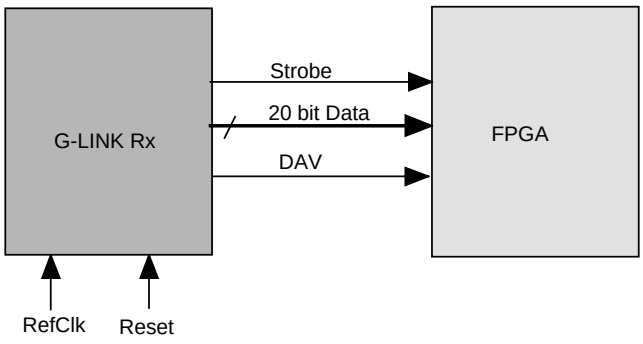



Figure 12. Interface between the G-Link receivers and the FPGAs

### 3.3.2.10 G-Link Destination Board Connector P2

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | +12V | DisMotherProm1 | 2 |
| 3 | | DisMotherProm2 | 4 |
| 5 | PromDONE | GROUND | 6 |
| 7 | GROUND | PromDATA | 8 |
| 9 | PromINIT | DIV0(C) | 10 |
| 11 | Busmode2# | +3.3V | 12 |
| 13 | EqA(C) | Busmode3# | 14 |
| 15 | +3.3V | Busmode4# | 16 |
| 17 | EqB(C) | GROUND | 18 |
| 19 | GLinkStrbA (F) | GLinkStrbB (F) | 20 |
| 21 | GROUND | EqC(C) | 22 |
| 23 | GLinkStrbC (F) | +3.3V | 24 |
| 25 | EqD(C) | Ser_En | 26 |
| 27 | +3.3V | GLinkStrbD (F) | 28 |
| 29 | DC_DATA_C0 | GROUND | 30 |
| 31 | DC_DATA_C2 | Mod20Sel (C) | 32 |
| 33 | GROUND | DC_DATA_C1 | 34 |
| 35 | PromCCLK | +3.3V | 36 |
| 37 | GROUND | DC_DATA_C3 | 38 |
| 39 | DC_DATA_C4 | GROUND | 40 |
| 41 | +3.3V | DC_DATA_C5 | 42 |
| 43 | DC_DATA_C6 | GROUND | 44 |
| 45 | DC_DATA_C8 | DC_DATA_C7 | 46 |
| 47 | GROUND | DC_DATA_C9 | 48 |
| 49 | DC_DATA_C10 | +3.3V | 50 |
| 51 | DC_DATA_C12 | DC_DATA_C11 | 52 |
| 53 | +3.3V | DC_DATA_C13 | 54 |
| 55 | DC_DATA_C14 | GROUND | 56 |
| 57 | DC_DATA_C16 | DC_DATA_C15 | 58 |
| 59 | GROUND | DC_DATA_C17 | 60 |
| 61 | DC_DATA_C18 | +3.3V | 62 |
| 63 | GROUND | DC_DATA_C19 | 64 |

Table 10. G-Link Destination Board Connector P2 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

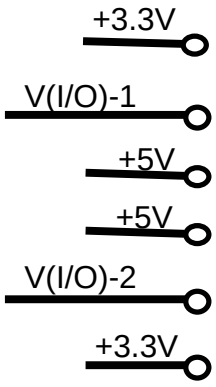
Note 1. Busmode [4:2]# signals are driven by the motherboard, Busmode 1# is returned by the daughter card to indicate presence of the card. These signals are not used in the G-Link and LVDS daughter card designs.
2. User Defined pins are spare pins for future use.

### 3.3.2.11 G-Link Destination Board Connector P3

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | DC_DATA_A0 | GROUND | 2 |
| 3 | GROUND | DC_DATA_A1 | 4 |
| 5 | DC_DATA_A2 | DC_DATA_A3 | 6 |
| 7 | DC_DATA_A4 | GROUND | 8 |
| 9 | V(I/O)-2 | DC_DATA_A5 | 10 |
| 11 | DC_DATA_A6 | DC_DATA_A7 | 12 |
| 13 | DC_DATA_A8 | GROUND | 14 |
| 15 | GROUND | DC_DATA_A9 | 16 |
| 17 | DC_DATA_A10 | DC_DATA_A11 | 18 |
| 19 | DC_DATA_A12 | GROUND | 20 |
| 21 | V(I/O)-2 | DC_DATA_A13 | 22 |
| 23 | DC_DATA_A14 | DC_DATA_A15 | 24 |
| 25 | DC_DATA_A16 | GROUND | 26 |
| 27 | GROUND | DC_DATA_A17 | 28 |
| 29 | DC_DATA_A18 | DC_DATA_A19 | 30 |
| 31 | DC_DATA_B0 | GROUND | 32 |
| 33 | GROUND | DC_DATA_B1 | 34 |
| 35 | DC_DATA_B2 | DC_DATA_B3 | 36 |
| 37 | DC_DATA_B4 | GROUND | 38 |
| 39 | V(I/O)-2 | DC_DATA_B5 | 40 |
| 41 | DC_DATA_B6 | DC_DATA_B7 | 42 |
| 43 | DC_DATA_B8 | GROUND | 44 |
| 45 | GROUND | DC_DATA_B9 | 46 |
| 47 | DC_DATA_B10 | DC_DATA_B11 | 48 |
| 49 | DC_DATA_B12 | GROUND | 50 |
| 51 | GROUND | DC_DATA_B13 | 52 |
| 53 | DC_DATA_B14 | DC_DATA_B15 | 54 |
| 55 | DC_DATA_B16 | GROUND | 56 |
| 57 | V(I/O)-2 | DC_DATA_B17 | 58 |
| 59 | DC_DATA_B18 | DC_DATA_B19 | 60 |
| 61 | Spare (C) | GROUND | 62 |
| 63 | GROUND | | 64 |

Table 11. G-Link Destination Board Connector P3 pin-out

Note: The V(I/O) pins on P1 and P3 should be tracked as shown below for selecting additional voltage pins if necessary



### 3.3.2.12 LVDS (400 Mbit/s) Destination Board Connector P1

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | DC Reset | -12V | 2 |
| 3 | GROUND | LVDSLock*AL (S) | 4 |
| 5 | DBID-1 | LVDSLock*BL (S) | 6 |
| 7 | Busmode1# | +5V | 8 |
| 9 | DBID-2 | LVDSLock*CL (S) | 10 |
| 11 | GROUND | LVDSLock*DL (S) | 12 |
| 13 | LVDSRefCLK | GROUND | 14 |
| 15 | GROUND | RCLKAH (F) | 16 |
| 17 | DBID-3 | +5V | 18 |
| 19 | V(I/O)-1 | RCLKBH (F) | 20 |
| 21 | LVDSLock*AH (S) | RCLKCH (F) | 22 |
| 23 | LVDSLock *BH (S) | GROUND | 24 |
| 25 | GROUND | RCLKDH (F) | 26 |
| 27 | LVDSLock *CH (S) | DBID-4 | 28 |
| 29 | LVDSLock *DH (S) | +5V | 30 |
| 31 | V(I/O)-1 | DBID-5 | 32 |
| 33 | DC_DATA_D0 | GROUND | 34 |
| 35 | GROUND | DC_DATA_D1 | 36 |
| 37 | DC_DATA_D2 | +5V | 38 |
| 39 | GROUND | DC_DATA_D3 | 40 |
| 41 | DC_DATA_D4 | DC_DATA_D5 | 42 |
| 43 | DC_DATA_D6 | GROUND | 44 |
| 45 | V(I/O)-1 | DC_DATA_D7 | 46 |
| 47 | DC_DATA_D8 | DC_DATA_D9 | 48 |
| 49 | DC_DATA_D10 | +5V | 50 |
| 51 | GROUND | DC_DATA_D11 | 52 |
| 53 | DC_DATA_D12 | DC_DATA_D13 | 54 |
| 55 | DC_DATA_D14 | GROUND | 56 |
| 57 | V(I/O)-1 | DC_DATA_D15 | 58 |
| 59 | DC_DATA_D16 | DC_DATA_D17 | 60 |
| 61 | DC_DATA_D18 | +5V | 62 |
| 63 | GROUND | DC_DATA_D19 | 64 |

Table 12. LVDS (400Mbit/s) Destination Board Connector P1 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

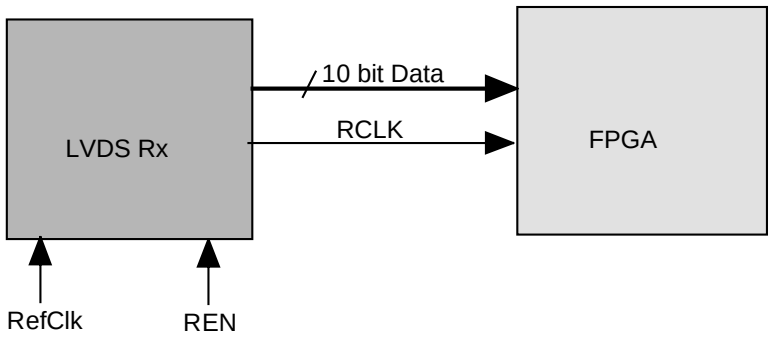



Figure 13. Interface between the LVDS De-serialiser and the FPGAs

### 3.3.2.13 LVDS (400 Mbit/s) Destination Board Connector P2

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | +12V | DisMotherProm1 | 2 |
| 3 | LVDS-PWDN* (C) | DisMotherProm2 | 4 |
| 5 | PromDONE | GROUND | 6 |
| 7 | GROUND | PromDATA | 8 |
| 9 | PromINIT | | 10 |
| 11 | Busmode2# | +3.3V | 12 |
| 13 | User defined | Busmode3# | 14 |
| 15 | +3.3V | Busmode4# | 16 |
| 17 | | GROUND | 18 |
| 19 | RCLKAL (F) | RCLKBL (F) | 20 |
| 21 | GROUND | | 22 |
| 23 | RCLKCL (F) | +3.3V | 24 |
| 25 | | Ser_En | 26 |
| 27 | +3.3V | RCLKDL (F) | 28 |
| 29 | DC_DATA_C0 | GROUND | 30 |
| 31 | DC_DATA_C2 | | 32 |
| 33 | GROUND | DC_DATA_C1 | 34 |
| 35 | PromCCLK | +3.3V | 36 |
| 37 | GROUND | DC_DATA_C3 | 38 |
| 39 | DC_DATA_C4 | GROUND | 40 |
| 41 | +3.3V | DC_DATA_C5 | 42 |
| 43 | DC_DATA_C6 | GROUND | 44 |
| 45 | DC_DATA_C8 | DC_DATA_C7 | 46 |
| 47 | GROUND | DC_DATA_C9 | 48 |
| 49 | DC_DATA_C10 | +3.3V | 50 |
| 51 | DC_DATA_C12 | DC_DATA_C11 | 52 |
| 53 | +3.3V | DC_DATA_C13 | 54 |
| 55 | DC_DATA_C14 | GROUND | 56 |
| 57 | DC_DATA_C16 | DC_DATA_C15 | 58 |
| 59 | GROUND | DC_DATA_C17 | 60 |
| 61 | DC_DATA_C18 | +3.3V | 62 |
| 63 | GROUND | DC_DATA_C19 | 64 |

Table 13. LVDS (400Mbit/s) Destination Board Connector P2 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

Note 1. Busmode [4:2]# signals are driven by the motherboard, Busmode 1# is returned by the daughter card to indicate presence of the card. These signals are not used in the G-Link and LVDS daughter card designs.
2. User Defined pins are spare pins for future use.

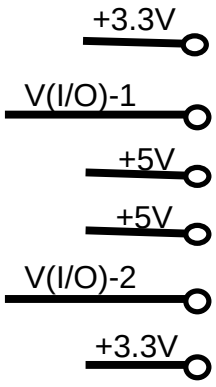
### 3.3.2.14 LVDS (400 Mbit/s) Destination Board Connector P3

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | DC_DATA_A0 | GROUND | 2 |
| 3 | GROUND | DC_DATA_A1 | 4 |
| 5 | DC_DATA_A2 | DC_DATA_A3 | 6 |
| 7 | DC_DATA_A4 | GROUND | 8 |
| 9 | V(I/O)-2 | DC_DATA_A5 | 10 |
| 11 | DC_DATA_A6 | DC_DATA_A7 | 12 |
| 13 | DC_DATA_A8 | GROUND | 14 |
| 15 | GROUND | DC_DATA_A9 | 16 |
| 17 | DC_DATA_A10 | DC_DATA_A11 | 18 |
| 19 | DC_DATA_A12 | GROUND | 20 |
| 21 | V(I/O)-2 | DC_DATA_A13 | 22 |
| 23 | DC_DATA_A14 | DC_DATA_A15 | 24 |
| 25 | DC_DATA_A16 | GROUND | 26 |
| 27 | GROUND | DC_DATA_A17 | 28 |
| 29 | DC_DATA_A18 | DC_DATA_A19 | 30 |
| 31 | DC_DATA_B0 | GROUND | 32 |
| 33 | GROUND | DC_DATA_B1 | 34 |
| 35 | DC_DATA_B2 | DC_DATA_B3 | 36 |
| 37 | DC_DATA_B4 | GROUND | 38 |
| 39 | V(I/O)-2 | DC_DATA_B5 | 40 |
| 41 | DC_DATA_B6 | DC_DATA_B7 | 42 |
| 43 | DC_DATA_B8 | GROUND | 44 |
| 45 | GROUND | DC_DATA_B9 | 46 |
| 47 | DC_DATA_B10 | DC_DATA_B11 | 48 |
| 49 | DC_DATA_B12 | GROUND | 50 |
| 51 | GROUND | DC_DATA_B13 | 52 |
| 53 | DC_DATA_B14 | DC_DATA_B15 | 54 |
| 55 | DC_DATA_B16 | GROUND | 56 |
| 57 | V(I/O)-2 | DC_DATA_B17 | 58 |
| 59 | DC_DATA_B18 | DC_DATA_B19 | 60 |
| 61 | Spare (C) | GROUND | 62 |
| 63 | GROUND | LVDS-REN | 64 |

Table 14. LVDS (400Mbit/s) Destination Board Connector P3 pin-out

The data bits are defined as 0 to 19 and the corresponding controls are defined as:
L for bits 0 - 9 and H for bits 10 - 19.

Note: The V(I/O) pins on P1 and P3 should be tracked as shown below for selecting additional voltage pins if necessary



### 3.3.3 Physical Dimensions

The following diagram shows the physical dimensions for the daughter board.

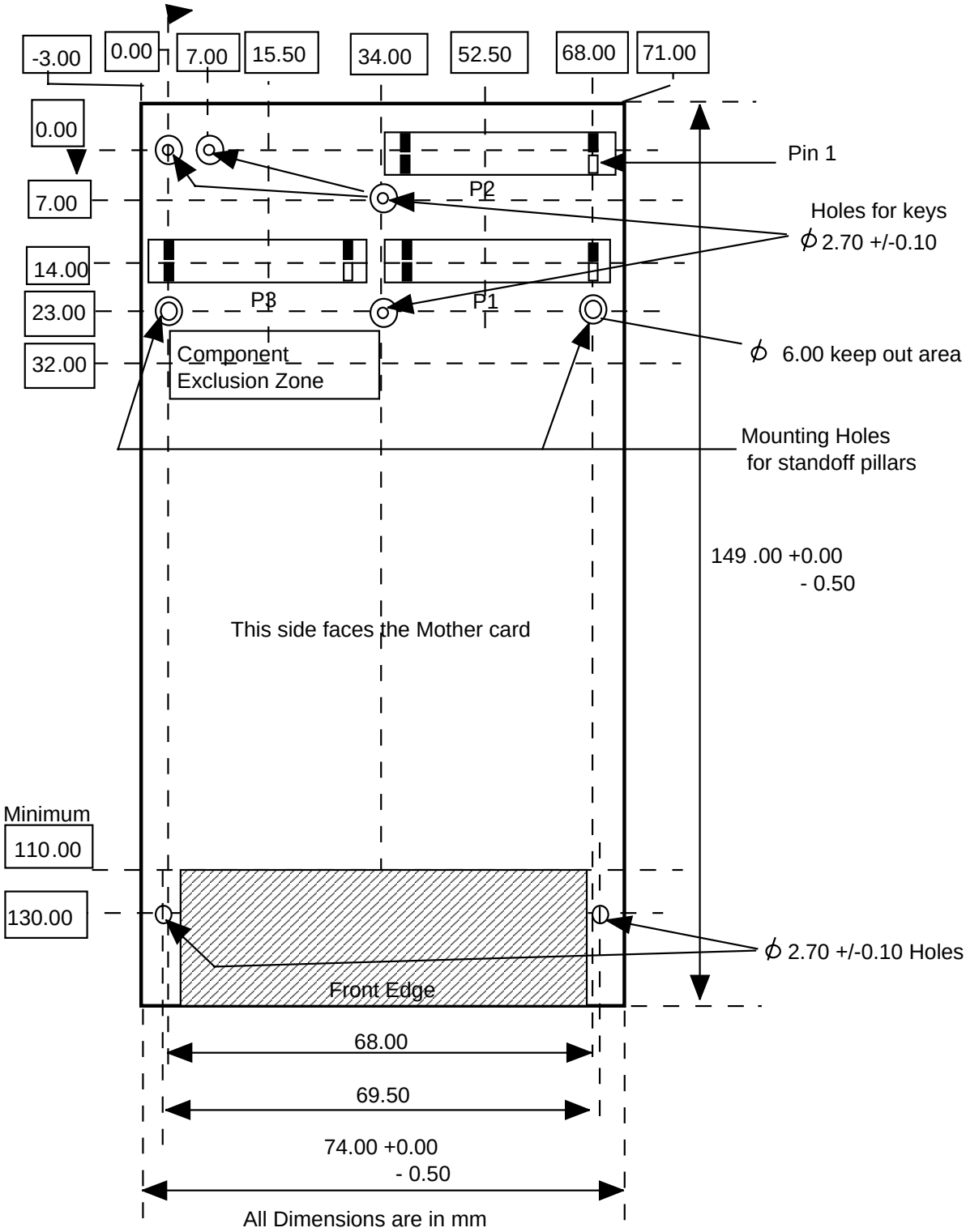



Figure 14. Dimensions for the CMC Daughter boards (not to scale)

Note: Due to mixed voltage designs, the voltage key pins on the motherboard will be left out.

### 3.3.4 Component Height Restrictions

On the side facing the mother board the component height is restricted to 4.7 mm, except:
1. Where there is an exclusion zone of 34 mm x 6 mm.
2. In the shaded area (68 mm x 33 mm) the component height could be up to 9.8 mm.
On the top side of the board the component height restriction is 3.50 mm including the board thickness (for a VME single width module). See figure 14.

### 3.3.5 CMC Bezel

For the front bezel and for other mechanical details refer to the IEEE P1386/Draft 2.0, 4 April-1995, standard for a Common Mezzanine Board family.

### 3.3.6 Signal Handling on the Daughter Boards

Since the signals between the daughter boards and the FPGAs on the mother board have to travel long distances, the tracks carrying the signals have to be transmission lines and must be terminated appropriately to the characteristic impedance (75 Ω) of these tracks. Only the source module should have series terminations as described in section 3.2.6.

### 3.3.7 Daughter Board PROMs

The PROMs on the daughter boards must be XC1701L-PD8 C (or equivalent), and should be in a socket.

### 3.3.8 *Ground Points*

At least one ground point must be provided for scope probe grounding.

## 3.3.8 Front Panel Input and Outputs

The front panel inputs/outputs to the daughter card will be through the front bezel and will differ from module to module.

#### *3.3.8.1 Front Panel Monitoring (LEDs)*

A minimum set of LEDs is recommended for the daughter modules depending on its functionality.

| Description | Signal name | Colour |
|---|---|---|
| Vcc | | Green |
| System clock is active | SYSCLK | Green |
| Locked signals | | Green |

## 3.4 Testing

### 3.4.1 Test Strategy

The DSS module allows the following tests to be carried out.
1. Stand alone test of the mother board (VME read/write and Loop back tests)
2. Test data loaded on to the dual-port RAMs and transmitting the data.
3. Serialising ASIC readout logic implemented on the FPGAs.
4. Transmitting pseudo random patterns implemented on the FPGAs

Figure 15 shows a typical test set-up to test a readout driver module.

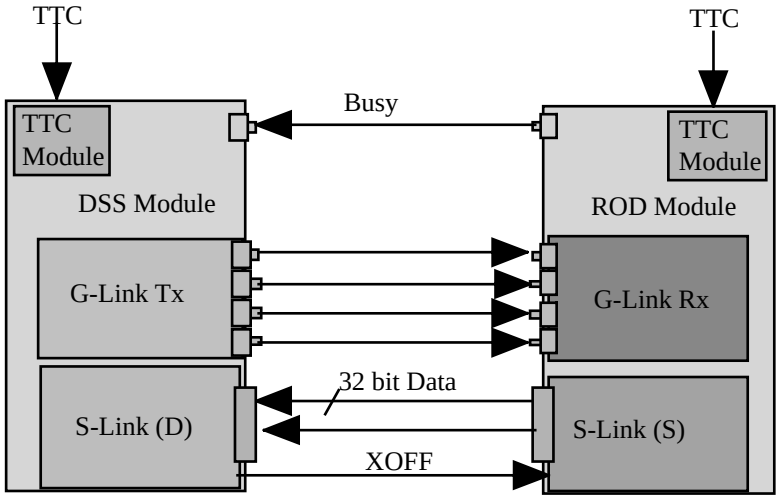



Figure 15. ROD Test set-up

### 3.4.2 Test Equipment

(1) VME crate
(2) 32 bit VME interface
(3) Computer to run software
(4) Demonstrator CPM and the TXM (initial tests on the G-Links)
(5) Demonstrator DAQ system
(6) Logic analyser
(7) Oscilloscope
(8) VME Extenders

## 3.5 Software

A test engineer from the System Support Group will develop the LabView test software.
For the complete tests for example with the ROD module, software will be required from the customer.

## 3.6 Manufacturing

An outside manufacturer will carry out the manufacture of the PCBs and the component assembly.

## 3.7 Installation

The DSS motherboard is designed to sit in a 6U crate with a VME (J1, J2) back plane. The module will be provided with a front panel containing sockets and monitoring LEDs as described in section 3.2.7, two slots for CMC modules. It may be implemented as double width module when using with G-Link daughter boards to accommodate the heat sinks.

## 3.8 Maintenance and further orders

This module is expected to be used in testing various prototype and production modules, and may be required by the other collaborating institutes. In the first instance a minimum of four DSS modules will be required for the UK group.

# 4. Project Management

## 4.1 Personnel

| | | RAL Ext. | RAL Location |
|---|---|---|---|
| Customer: | C. N. P. Gee | 6244 | R1, 1.39 |
| Project Manager: | V. Perera | 5692 | R68, 2.31 |
| Project Engineer | J. Edwards | 6814 | R68, 2.09 |

## 4.2 Deliverables

### 4.2.1 *To the Customer:*

1. Eight DSS mother boards.
2. Specification document and User Manual

### *4.2.2 From the Customer:*

Test Software, Powered VME crate (with J1 and J2 connectors) and a software platform to allow the test software to drive the DSS Module.

## 4.3 Project plan **(Milestones)**

| | |
|---|---|
| 1. Preliminary Design Review (PDR) | February - 1999 |
| 2. Final Design Review (FDR) | July - 1999 |
| 3. Start Testing | August - 1999 |
| 4. Concluding Review (CR) | December -1999 |

## 4.4 Design Reviews

The customer must be present at the PDR and the CR. If the customer wishes, he may attend the FDR.
The progress of the project will be reported on a monthly basis in the ATLAS Calorimeter First-level Trigger project monitor form.

## 4.5 Training

Training will be carried out as required on the job.

## 4.6 CAE

Cadence for schematic capture, VHDL and FPGA design tools, and Lab View for test software.

## 4.7 Costs and finance

**Cost Estimation**

All manufacturing, assembly and component costs will be charged to FK40000.

## 4.8 Intellectual Property Rights (IPR) and Confidentiality

All background and foreground Intellectual Property Rights in this project will remain with CLRC. The customer will have unrestricted rights to items listed under deliverables (4.2). If the customer requires other data, then an appropriate protective agreement should be in place before releasing such data.

## 4.9 Safety

General laboratory safety codes apply.

## 4.10 Environmental impact

### *4.10.1 Disposal*

RAL will dispose of the modules at end of their life.

### *4.10.2 EMC*

Since these are test modules and only to be used in a test environment by the collaborating institutes, the modules will not carry a CE mark. However since the electronics must function as designed, without malfunction or unacceptable degradation of performance due to electromagnetic interference (EMI) within their intended operational environment, the electronics shall comply with specifications intended to ensure electromagnetic compatibility.

## 4.11 Handling Precautions

Anti-static precautions must be taken when handling the module to prevent damage to expensive components.

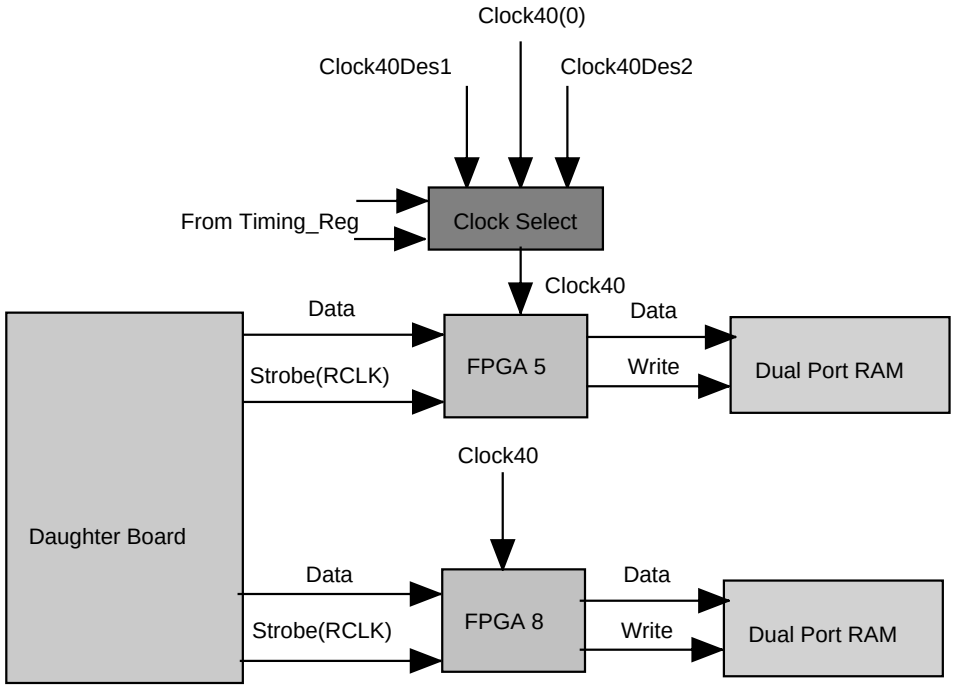
## Appendix A

### Timing Scheme for the DSS Modules

When using the TTC system or the TCM used in the demonstrator system, there will be three clock phases available on the motherboard. An appropriate clock phase from these three clocks will used on the daughter boards,
The three clocks are:

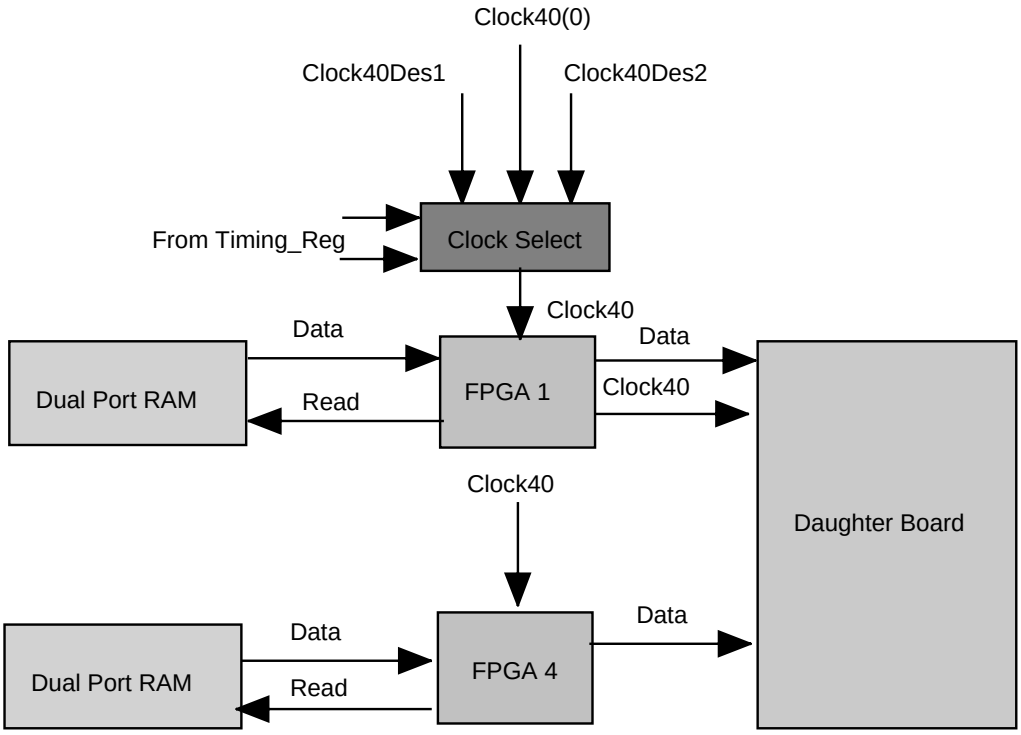
- Clock40
- Clock40Des1
- Clock40Des2

In the case of the TTC system the de-skew is programmed into the TTCrx chip. When using the TCM system, delay lines with step size of 1 ns to span the 25 ns clock cycle will be provided to adjust Clock40Des1 and Clock40Des2. The values of these delay lines can be set by the Timing Register (3.2.8.10)
These three clocks should be sufficient to adjust any ns for transmit and receive functions.




A suitable clock per group of four FPGAs is selected to to synchronise the data from the daughter board

Figure 1. Data Received Mode




A suitable clock per group of four FPGAs is selected to clock the data onto the Daughter Board

Figure 2. Data Transmit Mode

## Changes to DSS Specification version 2c July 1999

1. Page 11. Registers 40 to 5C are read only registers
2. Page 12. Registers B8 - DC are read only registers
3. Page 13. 120000-13FFFF data buffer 9 is source, 140000-15FFF data buffer 10 is Destination
4. Page 14. The mode bit definition will be as follows:

   ***3.2.8.5.1 Mode Bits***

| Mode bit 2 | Mode bit 1 | Mode bit 0 | Descriptive Name |
|---|---|---|---|
| 0 | 0 | 0 | No Test |
| 0 | 0 | 1 | *Pseudo Random Pattern -32K* |
| 0 | 1 | 0 | *Memory to Memory Test (Bypass)- 32K* |
| 0 | 1 | 1 | *Read Back and Compare Test - 32 K* |
| 1 | 0 | 1 | *Pseudo Random Pattern Forever* |
| 1 | 1 | 0 | *Bypass Forever* |
| 1 | 1 | 1 | *Read Back and Compare Test Forever* |
| 1 | 0 | 0 | *S-Link Test* |

5. Page 15
   1. section 3.2.8.5.2 Brcst bits 6 and 7 definitions
   2. section 3.2.8.5.3, 0 and 1 definitions swapped
6. Page 18. Section 3.2.8.9.1

   Bits 0-7 (16-23)

   0 Links locked

   1 Links not locked
7. Page 19 section 3.2.8.12 Pulse Register

   Bit 0 renamed to FPGA Reset

   Bit 5 added for S-Link destination counter reset