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SPECIFICATION OF 'G-LINK' DAUGHTER BOARDS FOR THE DATA SOURCE AND SINK MODULE 'DSS' TEST PLATFORM.

'G-LINK' SOURCE DAUGHTER BOARD 'GTx' IN SINGLE CMC FORMAT.
'G-LINK' SINK DAUGHTER BOARD 'GRx' IN SINGLE CMC FORMAT.

OVERVIEW.

The 'G-LINK' SOURCE DAUGHTER BOARD and 'G-LINK' SINK DAUGHTER BOARD will provide the physical layer of a system to allow testing of data transfer techniques between prototype modules for the Level 1 Calorimeter Trigger System and evaluate some elements of data transfer technologies. These boards will use the TTL version of HP G-LINK devices transmitting serialised data over a copper conductor. There will be four transmitter channels on the GTx board and four receiver channels on the GRx board. The data input to the GTx board will be as four parallel data words each of 20 bits at up to 40 MHz. The data output from the GRx board will be as four parallel data words each of 20 bits at up to 40 MHz.
The DSS mother board will interface between the controller (e.g. VME 147) and the Daughter Boards and provide control and timing signals and return status and error signals.
The principle use of this link technology is for the transmission of DAQ and RoI information between the Cluster Processing Modules (CPMs), Read Out Drivers (RODs), Cluster Merger Modules (CMMs), Jet Energy Modules (JEMs) and Jet Merger Modules (JMMs). Data will be transmitted following Level 1 Accepts and valid data will be indicated by assertion of the DAV signal.
G-LINK technology is an established medium for data transmission. These boards are intended to allow system tests with prototype Level 1 Trigger modules and therefore the ability to vary the operating modes of the G-LINK devices is limited to those necessary or to any previously untried modes. For example Flag control and Fill Frame control will not be accessible.
The two modules together with appropriate cabling will form a SIMPLEX link.
Note that while this specification concentrates on the operation of the G-LINK Daughter Board modules when fitted to a 'DSS' Mother Board, comparable interfacing must exist for the operation of these modules when operating within other systems e.g. the Prototype Read Out Driver (ROD) Module.

REFERENCE DOCUMENTS.

HEWLETT PACKARD Low Cost Gigabit Transmit/Receive Chip Set Technical Data Sheet for HDMP -1022 Transmitter and HDMP- 1024 Receiver.
Project Specification - ATLAS Calorimeter First level Trigger - Data Source and Sink Module Version 5.0.
Project Specifications for CPM & ROD.
Draft Standard for a Common Mezzanine Board Family: CMC, P1386/Draft 2.0 April 4, 1995.
Draft Standard Physical and Environmental Layers for PCI Mezzanine Boards: PMC, P1386.1/Draft 2.0 April 4, 1995.

ABBREVIATIONS USED

MB, DB	==	Mother Board, Daughter Board.
Tx, Rx	==	Transmitter, Receiver.
TCM, TTC	==	Timing Control Module, Timing Trigger Control.
CPM, ROD	==	Cluster Processor Module, Read Out Driver.

SERIAL INPUT AND OUTPUT FUNCTIONALITY.

The G-LINK GTx and GRx modules will be configurable to operate in either 'Differential Drive' or 'Single Ended Drive' mode each with a separate connector type.

The two serial input and output connection options will be selectable via jumper pads. Option 1 will be via 2mm grid connectors e.g. Metral and twinax or screened twisted pair cable and option 2 will be via coaxial connectors e.g. Metral coaxial and miniature coaxial cable. A range of lengths will be tested.

These I/O connectors will be electrically isolated from any front panel, see CMC spec.

No direct ground connection will be provided between the GTx and GRx modules. A configurable ground connection via jumpers will be available. Overall strategy on grounding between modules is to be agreed.

THE INTERFACE BETWEEN MOTHER BOARD AND DAUGHTER BOARDS.

DATA, STROBES, CONTROL and STATUS SIGNALS IDENTIFICATION.

The signals comprising the four channels will be identified and labelled with suffixes A to D. D00 will be the least significant data bit and D19 the most significant. Signals common to all channels will not have a suffix.

INTERFACING OF INTER MOTHER BOARD & DAUGHTER BOARD SIGNALS

All MB to DB signals are routed via connectors P1, P2 and P3. These are placed and have the basic pin configurations as per the CMC and PCM specifications.

The signal levels at this interface will be standard TTL.

The polarity of signals at the interface will be that as directly required for or generated by the G-LINK devices.

SIGNAL TERMINATION

All signals (data, strobes, control and status lines) will be series terminated with 100 ohms at the signal source.
Hence inputs to the DB from the MB will be terminated on the MB and outputs from the DB to the MB will be terminated on the DB.

LOGIC LEVEL TRANSLATIONS

None is required.

SIGNAL TRACKS ON THE DAUGHTER BOARDS

Where practical all signal paths on the daughter boards will be constructed as 100 ohm Micro-strip or Strip lines.

MB TO GTx DB INTERFACE; DEFINITION & FUNCTION OF SIGNALS.

Interface signal name	G_LINK signal name	Description.
GLinkReset*;	RST*	Generated from Reset Control Register. Resets all G-LINK internal registers, assert for >5 transmit clock periods.
GLinkRdy(n)*;	RFD(n)	Generated by G-LINK device. Indicates that device is ready to accept data for transmission. One line per channel.
GLinkDav(n)*;	DAV(n)*	Generated on Mother Board. Indicates that valid data is present on the device data input lines. One line per channel.
GLinkClk(n);	STRBIN	Generated on Mother Board. Indicates rate of data frame transmission. One line per channel

MB TO DESTINATION (Rx) DB INTERFACE; DEFINITION & FUNCTION OF SIGNALS.

Interface signal name	G_LINK signal name	Description.
GLinkReset*;	SMRST0*	Generated from Reset Control Register. Resets G-LINK device, causes PLL locking restart.
GLinkRdy(n)*;	LINKRDY(n)*	Generated by G-LINK device. Indicates that device has correctly initialised and has valid controls states. One line per channel.
GLinkDav(n)*;	DAV(n)*	Generated by G-LINK device. Indicates that valid data is present on the device data output lines. One line per channel.
GlinkRefClk;	LIN	Generated on Mother Board, approximates to rate of data frame reception. Common to all channels.
GLinkErr(n);	ERROR(n)	Generated by G-LINK device. Indicates that device has received a frame with invalid encoding. One line per channel.
GLinkStrb(n);	STRBOUT(n)	Generated by G-LINK device. Indicates actual frame receipt rate and time at which received data is valid.
DIV0;	DIV0	Generated from controller. Sets G-LINK V.C.O. division chain factor. Common to all channels.
EQEN(n);	EQEN(n)	Generated from controller. Selects input cable equalisation amplifier. One line per channel.
MOD20SEL;	MOD20SEL	Generated from controller. Selects 16 bits or 20 bits mode. Common to all channels.

G-LINK TRANSMITTER DEVICE, FUNCTION IMPLEMENTATION

The following G-LINK TRANSMITTER control/strobe functions will be accessible via the DSS MB to DB interface:-

DAV*, RST*.

A transmit clock will be applied to STRBIN.

The following G-LINK control/strobe functions will NOT be accessible via the DSS MB to DB interface but set at an appropriate logic level:-

CAV*, DIV0, DIV1, ED, EHCLKSEL, FF, FLAG, FLAGSEL, HCLKON, LOOPEN, MDFSEL, M20SEL.

The following G-LINK TRANSMITTER status output will be accessible via the DSS MB to DB interface:-

LOCKED (via ED & RFD)

The following G-LINK TRANSMITTER functions or outputs will be accessible via local monitoring points:-

LOCKED, STRBOUT.

The following G-LINK TRANSMITTER functions or outputs will be NOT be accessible:-

HCLK, HCLK*, INV, LOUT, LOUT*, TEMP, TEMP*.

G-LINK RECEIVER DEVICE, FUNCTION IMPLEMENTATION

The following G-LINK RECEIVER control/strobe functions will be accessible via the DSS MB to DB interface:-

DIV0, EQEN, M20SEL, SMRST0*.

A reference clock (GlinkRefClk) will be applied to LIN.

The following G-LINK RECEIVER controllable functions will NOT be accessible via the DSS MB to DB interface but set at an appropriate logic level or configured as required:-

ACTIVE, DIV1, FDIS, FLAGSEL, LOOPEN, SMRST1*, TCLK, TCLKSEL .

The following G-LINK RECEIVER status or strobe functions will be accessible via the DSS MB to DB interface:-

DAV*, ERROR, LINKRDY*, STRBOUT.

The following G-LINK RECEIVER function will also be accessible via local monitoring points:-

STRBOUT.

The following G-LINK RECEIVER functions or outputs will be NOT be accessible via the DSS MB to DB interface but will be set at an appropriate logic level or configured as required:-

CAV*, FLAG, FF, LIN*, STAT0, STAT1, TEMP, TEMP* .

INTERFACE SIGNAL TYPES AND ASSOCIATED TIMINGS

The timing specifications are as per the G-LINK data sheet. These specify the G-LINK signals at the MB / DB interface either received from, or transmitted to, the Mother Board.

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Source (GTx) Module.

RST*	Generated from Reset Control Register. Assert for >5 transmit clock periods.
D00 - D19	1 Clock Cycle Pulse; Output from Data FPGAs on MB.
DAV	1 Clock Cycle Pulse; From data flow control logic on MB.
STRBIN	From MB, 50% Duty cycle at frame transmit rate.
RFD	Level; From G-LINK device, re-timed LOCKED signal.

D00 - D19 & DAV presented with minimum or greater set up and hold times w.r.t. STRBIN. (Min = 2nS.)

Destination (GRx) Module.

DIV0, EQEN, MOD20SEL	Level; Programmed to logic 0 or logic 1 via DB Control Register.
SMRST0*	Generated from Reset Control Register.
D00 - D19	1 Clock Cycle Pulse; Input to Data FPGAs on MB.
DAV	1 Clock Cycle Pulse; Input to data flow control logic on MB.
ERROR	1 Clock Cycle Pulse; Input to MB.
LINKRDY	Level; Input to Status Register on MB.
STRBOUT	Duty Cycle as per spec; Input at frame received rate to data flow control and status logic on MB.

D00 - D19, DAV and ERROR asserted by G-LINK device with specified set up and hold times w.r.t. STRBOUT.

DAUGHTER BOARD'S PHYSICAL CHARACTERISTICS

VOLTAGE SUPPLIES

Voltage rail	Estimated Current
+5V	? Amps
V(I/O)	See note
+3.3V	? mA

All supply voltages are supplied by the Mother Board via the P1, P2 & P3 connectors, none is derived on the Daughter Board. N.B. The V(I/O) pins on P1 may be used as additional VCC contacts by bridging links provided. +3.3v only used to supply FPGA (E)EPROM.

G-LINK DEVICES ENVIRONMENT

0.1uF capacitors will be fitted between the CAP0B and CAP1B connections on all devices. VCC, VCC_HS, VCCTTL, GND and GNDTTL connections will be made to VCC and GND supply planes. He recommended de-coupling and termination will be applied.

MOTHER BOARD TO DAUGHTER BOARD CONNECTOR TYPES

The following MB/DB connectors will give 10 mm stacking.
Plug (P) (Molex 53483-0649) on the Daughter Boards.
Socket (J) (Molex 52763-0649) on the Mother Boards.

BOARD PROFILE

As per CMC specification. See references.

COMPONENT HEIGHT RESTRICTIONS

On the side facing the mother board - 'Side 1' - the maximum component height is 4.7 mm. Other exclusion zones are detailed in the DSS specification, eg 'SLink' connector area.
No limit can be placed on the height of components on Side 2 due to the need for heat sinks on the G_LINK and other devices.

FRONT PANEL FORMAT & GENERAL MECHANICAL FEATURES

For the front panel and for other mechanical details refer to the IEEE P1386/Draft 2.0, 4 April-1995, standard for a Common Mezzanine Board family. However the size of connectors required on the bezel excludes the use of a standard sized bezel.

FRONT PANEL MONITORING (LEDS)

Leds will be provided in the Daughter Board's front panel.

Leds fitted will depend on board type

GTx Led Displays	Colour	GRx Led Displays	Colour
VCC	Green	VCC	Green
G-LINK Clock Present	Green	G-LINK Clock Present	Green
DAV(n) - 1 per channel	Green	DAV(n) - 1 per channel	Green
Link Ready (n) - 1 per channel	Green	Link Ready (n) - 1 per channel?	Green
		Link Error (n) - 1 per channel?	Yellow

FRONT PANEL CONNECTOR TYPES

Connector types for the serial inputs and outputs are BERG Metral signal (5x6) and BERG Metral Co-Axial (6 ways). The configuration of the connectors will be by patching links on the PCB.

CONNECTOR & INTER-MODULE GROUNDING

Links will be provided to enable inter-module grounding via the I/O cables if required.

CABLE TYPES & LENGTHS

To be decided.

DAUGHTER BOARDS CONTROLS AND TESTING

MEMORY MAP

The control and status registers for both Daughter Boards types are configured into the Mother Board Control logic, see DSS Mother Board specification (3.2.8.x). No additional registers will exist on the Daughter Boards

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DAUGHTER BOARD CONFIGURATION PROMS

The E(E)PROMs on the Daughter Boards will be socketed . Sockets for XC1701L (DIP - 8) and AT17LV010 (PLCC - 20) will be provided.

DAUGHTER BOARD CONFIGURATION E(E)PROMS PROGRAMMING

The daughter board configuration E(E)PROMS are programmed via the MB or off-line. An 'In-System-Programming Port' (ISP) and a VME programming port are provided on the Mother Board for transferring configuration data to the DB configuration E(E)PROMs. Programmable parts or separate ISP ports on the Daughter Board are not provided.

CONFIGURATION CODE DEVELOPMENT

Development of the configuration code will be done in conjunction with the MB designers i.e. RAL Technology Department.

TEST PROGRAMMING

Test software is required to perform the following functions.

Source Module (GTx) - Generate module 'Reset', set up operating mode(s), read status, take correcting action as required on error conditions, load test or other data patterns into DSS module, initiate data transfers, perform timing adjustments i.e. vary delays.

Destination Module (GRx) - Generate module 'Reset', set up operating mode(s), read status, take correcting action as required on error conditions, initiate data transfers into DSS module, compare received data patterns with transmitted data patterns, perform timing adjustments i.e. vary delays.

TESTING

Stand alone testing will be limited to DC and continuity checks, all functional tests will require a Mother Board and computer access.

DAUGHTER BOARDS DESIGN & MANUFACTURE

A provisional date of mid April '99 has been given by RAL Drawing Office for layout.

ASSOCIATED DSS MOTHER BOARD INFORMATION

CLOCK OPTIONS ON THE DSS (MB) MODULE (Taken from DSS Specification).

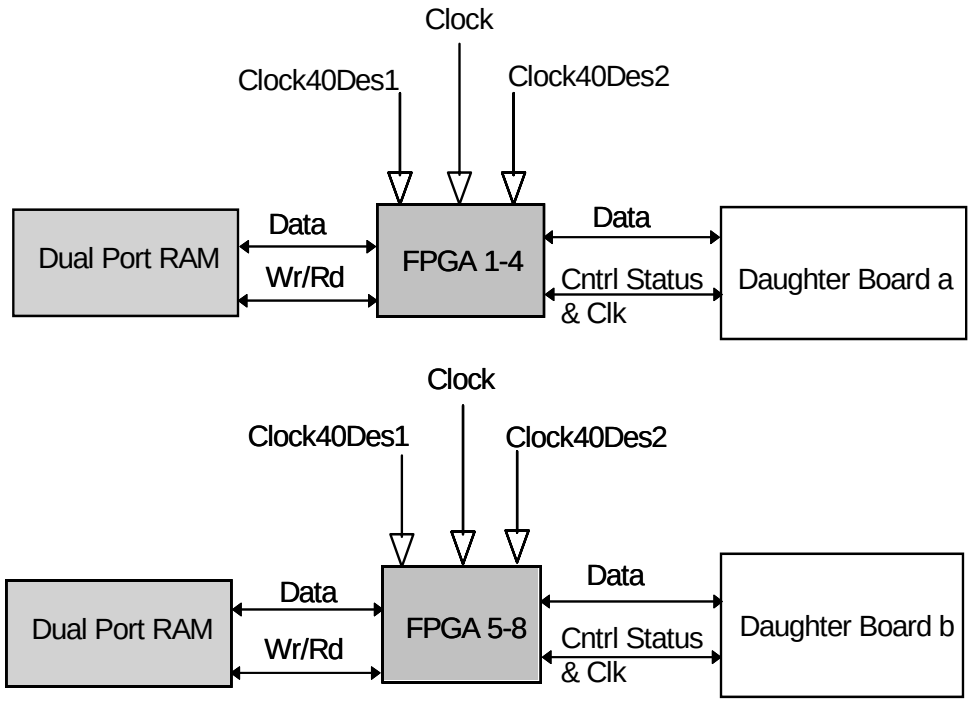
A system clock will be generated from either the TTCrx (normally) or TCM (initially) modules. Three phases will be derived on the mother board and an appropriate phase from one of these will be made available to the daughter boards. The three clocks are:

- Clock40
- Clock40Des1
- Clock40Des2

In the case of the TTC system the de-skew (delay) is programmed into the TTCrx chip. When using the TCM system (mother board) programmable delays, with step size of 1 ns to span the 25 ns clock cycle, will be provided to adjust Clock40Des1 and Clock40Des2. The values of these delays can be set by the Timing Register.

In addition a Reference clock at approximately 40Mhz will be available for the GRx module.

CLOCK USAGE BASIC DIAGRAM.

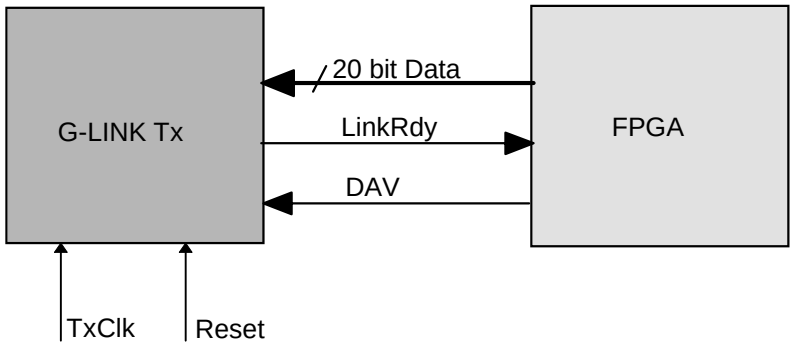


One of the three clocks is used by the FPGA to clock data to or from the Daughter Boards

MB - DB INTER CONNECTIONS SIGNAL TO PIN ALLOCATION

G-Link Source Board (GTx) Connector P1

Pin	Signal	Signal	Pin
1	GLinkRESET* (Common Reset)	-12V	2
3	GROUND	GLinkRdyA* (Channel A Status)	4
5	DBID-1	GLinkRdyB* (" B ")	6
7	Busmode1#	+5V	8
9	DBID-2	GLinkRdyC* (" C ")	10
11	GROUND	GLinkRdyD* (" D ")	12
13		GROUND	14
15	GROUND	GLinkDAVA* (Channel A Data Ready Flag)	16
17	DBID-3	+5V	18
19	V (I/O)	GLinkDAVB* (" B " " ")	20
21		GLinkDAVC* (" C " " ")	22
23		GROUND	24
25	GROUND	GLinkDAVD* (" D " " ")	26
27		DBID-4	28
29		+5V	30
31	V (I/O)	DBID-5	32
33	GDD0	GROUND	34
35	GROUND	GDD1	36
37	GDD2	+5V	38
39	GROUND	GDD3	40
41	GDD4	GDD5	42
43	GDD6	GROUND	44
45	V (I/O)	GDD7	46
47	GDD8	GDD9	48
49	GDD10	+5V	50
51	GROUND	GDD11	52
53	GDD12	GDD13	54
55	GDD14	GROUND	56
57	V (I/O)	GDD15	58
59	GDD16	GDD17	60
61	GDD18	+5V	62
63	GROUND	GDD19	64



Data Interface between the G-Links and FPGAs

G-Link Source Board (GTx) Connector P2

Pin	Signal	Signal	Pin
1	+12V	DisMotherProm1	2
3		DisMotherProm2	4
5	PromDONE	GROUND	6
7	GROUND	PromDATA	8
9	PromINIT		10
11	Busmode2#	+3.3V	12
13		Busmode3#	14
15	+3.3V	Busmode4#	16
17		GROUND	18
19	GlinkClk_A	GlinkClk_B	20
21	GROUND		22
23	GlinkClk_C	+3.3V	24
25		Ser_En	26
27	+3.3V	GlinkClk_D	28
29	GDC0	GROUND	30
31	GDC2		32
33	GROUND	GDC1	34
35	PromCCLK	+3.3V	36
37	GROUND	GDC3	38
39	GDC4	GROUND	40
41	+3.3V	GDC5	42
43	GDC6	GROUND	44
45	GDC8	GDC7	46
47	GROUND	GDC9	48
49	GDC10	+3.3V	50
51	GDC12	GDC11	52
53	+3.3V	GDC13	54
55	GDC14	GROUND	56
57	GDC16	GDC15	58
59	GROUND	GDC17	60
61	GDC18	+3.3V	62
63	GROUND	GDC19	64

G-Link Source Board (GTx) Connector P3

Pin	Signal	Signal	Pin
1	GDA0	GROUND	2
3	GROUND	GDA1	4
5	GDA2	GDA3	6
7	GDA4	GROUND	8
9	V (I/O)	GDA5	10
11	GDA6	GDA7	12
13	GDA8	GROUND	14
15	GROUND	GDA9	16
17	GDA10	GDA11	18
19	GDA12	GROUND	20
21	V (I/O)	GDA13	22
23	GDA14	GDA15	24
25	GDA16	GROUND	26
27	GROUND	GDA17	28
29	GDA18	GDA19	30
31	GDB0	GROUND	32
33	GROUND	GDB1	34
35	GDB2	GDB3	36
37	GDB4	GROUND	38
39	V (I/O)	GDB5	40
41	GDB6	GDB7	42
43	GDB8	GROUND	44
45	GROUND	GDB9	46
47	GDB10	GDB11	48
49	GDB12	GROUND	50
51	GROUND	GDB13	52
53	GDB14	GDB15	54
55	GDB16	GROUND	56
57	V (I/O)	GDB17	58
59	GDB18	GDB19	60
61		GROUND	62
63	GROUND		64

Status and Control registers implemented on the mother board:

Control register:

Reset - one bit.

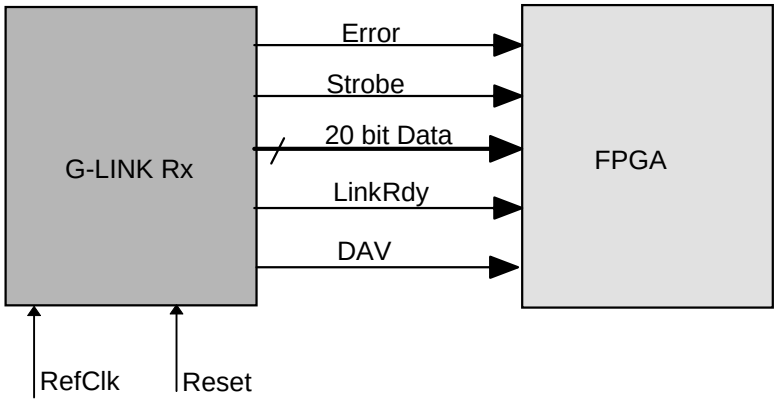
Status register:

LinkRdy - four bits

PromDone - one bit

G-Link Destination Board (GRx) Connector P1

Pin	Signal	Signal	Pin
1	GLinkRESET* (Common Reset)	-12V	2
3	GROUND	GLinkRdyA* (Channel A Status)	4
5	DBID-1	GLinkRdyB* (" B ")	6
7	Busmode1#	+5V	8
9	DBID-2	GLinkRdyC* (" C ")	10
11	GROUND	GLinkRdyD* (" D ")	12
13	GLinkRefClk	GROUND	14
15	GROUND	GLinkDAVA* (Channel A Data Ready Flag)	16
17	DBID-3	+5V	18
19	V (I/O)	GLinkDAVB* (" B " " ")	20
21	GLinkErrA	GLinkDAVC* (" C " " ")	22
23	GLinkErrB	GROUND	24
25	GROUND	GLinkDAVD* (" D " " ")	26
27	GLinkErrC	DBID-4	28
29	GLinkErrD	+5V	30
31	V (I/O)	DBID-5	32
33	GDD0	GROUND	34
35	GROUND	GDD1	36
37	GDD2	+5V	38
39	GROUND	GDD3	40
41	GDD4	GDD5	42
43	GDD6	GROUND	44
45	V (I/O)	GDD7	46
47	GDD8	GDD9	48
49	GDD10	+5V	50
51	GROUND	GDD11	52
53	GDD12	GDD13	54
55	GDD14	GROUND	56
57	V (I/O)	GDD15	58
59	GDD16	GDD17	60
61	GDD18	+5V	62
63	GROUND	GDD19	64



Data Interface between the G-Link receivers and FPGAs

G-Link Destination Board (GRx) Connector P2

Pin	Signal	Signal	Pin
1	+12V	DisMotherProm1	2
3		DisMotherProm2	4
5	PromDONE	GROUND	6
7	GROUND	PromDATA	8
9	PromINIT	DIV0	10
11	Busmode2#	+3.3V	12
13	EQEN_A	Busmode3#	14
15	+3.3V	Busmode4#	16
17	EQEN_B	GROUND	18
19	GLinkStrbA	GLinkStrbB	20
21	GROUND	EQEN_C	22
23	GLinkStrbC	+3.3V	24
25	EQEN_D	Ser_En	26
27	+3.3V	GLinkStrbD	28
29	GDC0	GROUND	30
31	GDC2	MOD20SEL	32
33	GROUND	GDC1	34
35	PromCCLK	+3.3V	36
37	GROUND	GDC3	38
39	GDC4	GROUND	40
41	+3.3V	GDC5	42
43	GDC6	GROUND	44
45	GDC8	GDC7	46
47	GROUND	GDC9	48
49	GDC10	+3.3V	50
51	GDC12	GDC11	52
53	+3.3V	GDC13	54
55	GDC14	GROUND	56
57	GDC16	GDC15	58
59	GROUND	GDC17	60
61	GDC18	+3.3V	62
63	GROUND	GDC19	64

G-Link Destination Board (GRx) Connector P3

Pin	Signal	Signal	Pin
1	GDA0	GROUND	2
3	GROUND	GDA1	4
5	GDA2	GDA3	6
7	GDA4	GROUND	8
9	V (I/O)	GDA5	10
11	GDA6	GDA7	12
13	GDA8	GROUND	14
15	GROUND	GDA9	16
17	GDA10	GDA11	18
19	GDA12	GROUND	20
21	V (I/O)	GDA13	22
23	GDA14	GDA15	24
25	GDA16	GROUND	26
27	GROUND	GDA17	28
29	GDA18	GDA19	30
31	GDB0	GROUND	32
33	GROUND	GDB1	34
35	GDB2	GDB3	36
37	GDB4	GROUND	38
39	V (I/O)	GDB5	40
41	GDB6	GDB7	42
43	GDB8	GROUND	44
45	GROUND	GDB9	46
47	GDB10	GDB11	48
49	GDB12	GROUND	50
51	GROUND	GDB13	52
53	GDB14	GDB15	54
55	GDB16	GROUND	56
57	V (I/O)	GDB17	58
59	GDB18	GDB19	60
61		GROUND	62
63	GROUND		64

Status and Control registers implemented on the mother board:

Control register:

Reset - one bit.
DIV0 - one bits.
EQEN - four bits
MOD20SEL - one bit

Status register:

Linkready - four bits
Linkerror - four bits
Config. Prom Done - one bit

R.W.Hatley.