ATLAS Calorimeter First Level Trigger

LVDS source CMC daughter boards for Data Source and Sink (DSS) Module

PC3144M/2

Design Specification

(Version 3.1)

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Purpose

Originally used for evaluating LVDS serialisers and cable assemblies, this version of the Source card is intended to drive data into the CPM test system. The card has a new connector which matches the termination of the AMP cable assemblies that were chosen after the original cards were made.

Source and sink modules plug into a DSS Module which will provide data generator and error detector functions as appropriate.

Related documents

Draft Standard for CMC. IEEE P1386. IEEE.

DSS Specification. V.Perera.

DS92LV1023 Data Sheet. National Semiconductor.

The above documents can be found in electronic format from the following address:

www.ep.ph.bham.ac.uk/user/staley/

Schematics for this and previous cards are available from the RAL Drawing Office with the following numbers:

Sink board:	CMC format LVDS Receiver	PC3143M/1 PC3143M/2
Source board:	CMC format LVDS Transmitter	PC3144M/1 PC3144M/2

Functional Requirements

Conforms to Common Mezzanine Card (CMC) format, IEEE P1386 ,
except for Front panel Bezel.

Source module will contain 8 LVDS serialisers (National DS92LV1023).

Pre-compensation for long cables.

Cable connector will use AMP part 1-106012-1 (or similar) that matches the Halogen free minature cable assembly from AMP , part: 1370754-1.

Series termination as appropriate for DSS I/O.

Monitoring points for all clock signals.

Configuration PROM for XILINX FPGA on DSS module.

Front panel indicator for CMC power.

Document changes

Version 3.0 <= previous

Cable Connector type changed to AMP 2mm male
Pre-compensation added
JTAG EEPROM added
40MHz - 66MHz LVDS parts used

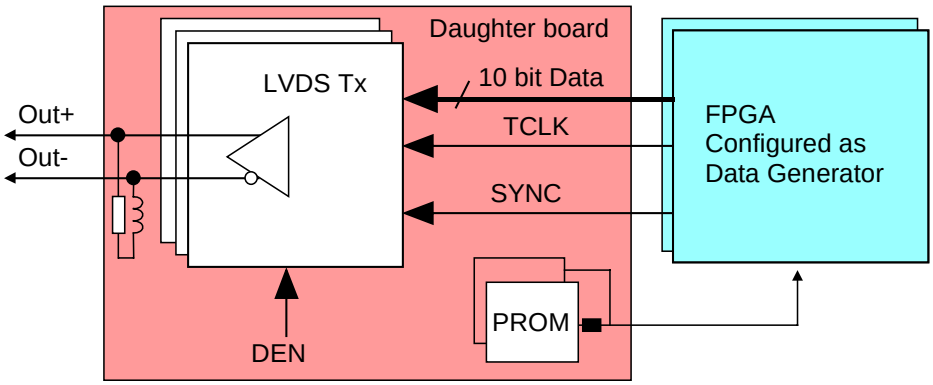
Version 3.1 <= 3.0

Cable pinout and memory map changed to aid layout.

Functional Description

The DSS interface to each daughter board uses a number of FPGAs. On power-up the FPGAs load their configuration data from a PROM on the daughter board to implement fuctions as required by that particular daughter board.
In the case of the Source board the FPGA is configured as a data generator, but for the Sink board the FPGA becomes an error detector. The PROM will have been programmed previously from data generated by FPGA design and synthesis tools.

Source Configuration



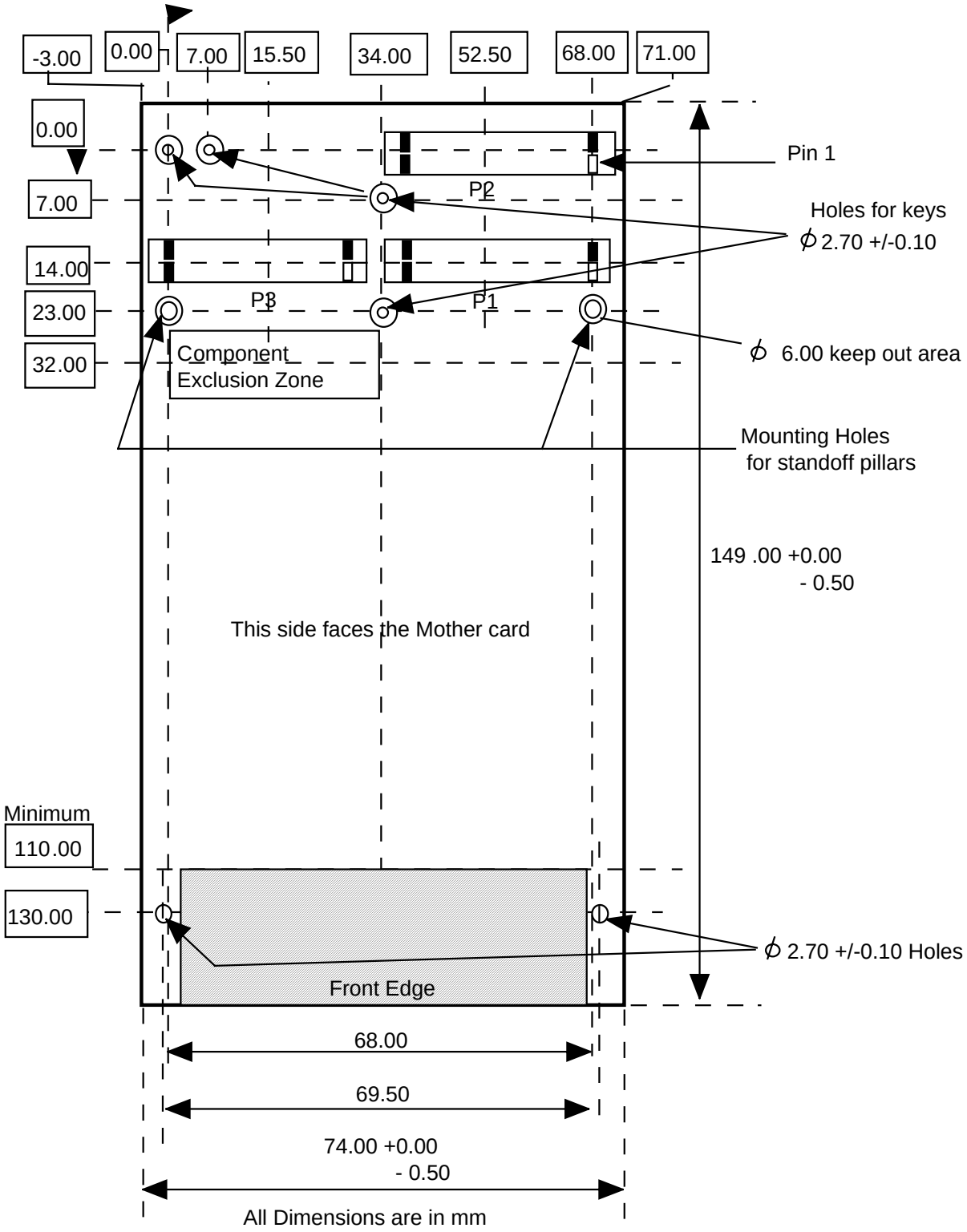
The installed pre-compensation will be for 15m - 20m of cable of type similar to AMP part# 1370754-1. The pre-compensation R & L are easily changed to accommodate different cable lengths and types.

A XILINX XC18V01 EEPROM is fitted as the default option and is programmed via the JTAG connector.
There is also a 20 pin socket for an EEPROM type AT17LV010 as on the original PCB, which may be used, providing a link on the Xilinx part is removed.
Both PROMS are 3.3V types.

Physical Dimensions and Component Placement.

Component height towards the motherboard is restricted to 4.7mm.

The following diagram shows the physical dimensions for the daughter board.
(from DSS Spec. Draft 5 Section 3.3.3.)



Front panel Cable connector

- Mechanical

The 2mm cable connector is too large for the standard CMC bezel. **To this end a non-standard double-width VME front panel for the DSS is needed** , and the cable connectors will be mounted on the side facing away from the motherboard.

The boards will take either the male or the female versions of the Free Board connectors.

- Electrical

Front panel connector Pin-out (LVDS serial data)

Connector PL3 (5x11 grid)	Column a	Column b	Column c	Column d	Column e
Row 1			GND		
Row 2			GND		
Row 3	DL+	DL-	GND	DH+	DH-
Row 4	CL+	CL-	GND	CH+	CH-
Row 5			GND		
Row 6			GND		
Row 7			GND		
Row 8	BL+	BL-	GND	BH+	BH-
Row 9	AL+	AL-	GND	AH+	AH-
Row 10			GND		
Row 11			GND		

This pinout maps onto the CPM rear connector as:

	Column a	Column b	Column c	Column d	Column e
Row n+1	RL+	RL-	GND	RM+	RM-
Row n	QL+	QL-	GND	QM+	QM-

RL,RM,Ql and QM are the four input channels to one serialiser on the CPM

The cable has a differential impedance of 100Ω.

AMP part numbers:

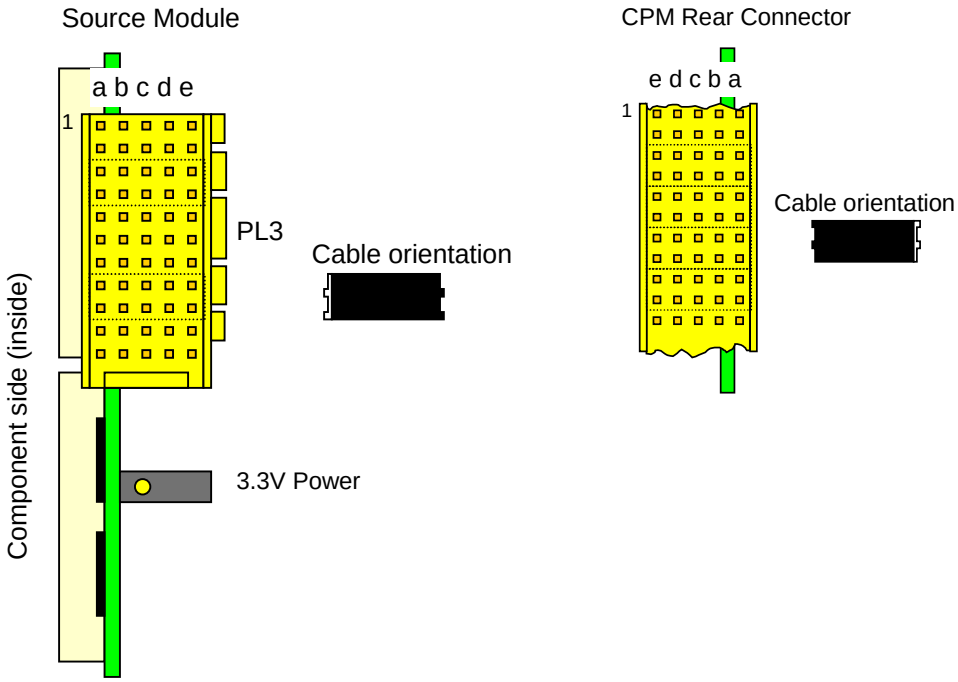
Right angle male Z-Pack 2mm connector; 1-106012-1

Custom cable assembly , 15m 1370754-1

Source board front panel Indicators

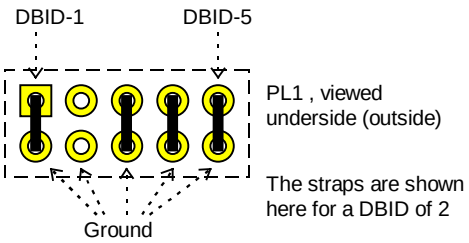
+3.3V Power	Yellow

Front panel layout



DaughterBoard ID links on PL1

These links convey the board serial number to the motherboard using the DBID-[1..5} signals. A link will set a ‘0’ , otherwise the DBID lines will be pulled high to a ‘1’.



Electrical interface with DSS Motherboard

Module will use +3.3V supply for the LVDS and other logic.

I/O levels are compatible with 3.3V logic, ie LVTTL with 1.5V thresholds, V_{IL} @ 0.8V , V_{IH} @ 2.0V.

Signals operating at 40MHz will be series terminated with trace impedances and matching terminators of around 80Ω. (80Ω is about the maximum obtainable for a 6-layer board with 0.006" wide tracks on the inner layers)

Source board connector pinouts

Source Board Connector P1

Pin	Signal	Signal	Pin
1	User Defined	-12V	2
3	GROUND		4
5	DBID-1		6
7	Busmode1#	+5V	8
9	DBID-2		10
11	GROUND		12
13		GROUND	14
15	GROUND		16
17	DBID-3	+5V	18
19	V (I/O)		20
21			22
23		GROUND	24
25	GROUND		26
27		DBID-4	28
29		+5V	30
31	V (I/O)	DBID-5	32
33	LDD0	GROUND	34
35	GROUND	LDD1	36
37	LDD2	+5V	38
39	GROUND	LDD3	40
41	LDD4	LDD5	42
43	LDD6	GROUND	44
45	V (I/O)	LDD7	46
47	LDD8	LDD9	48
49	LDD10	+5V	50
51	GROUND	LDD11	52
53	LDD12	LDD13	54
55	LDD14	GROUND	56
57	V (I/O)	LDD15	58
59	LDD16	LDD17	60
61	LDD18	+5V	62
63	GROUND	LDD19	64

Source Board Connector P2

Pin	Signal	Signal	Pin
1	+12V	DisMotherProm1	2
3	LVDS-PWDN*	DisMotherProm2	4
5	PromDONE	GROUND	6
7	GROUND	PromDATA	8
9	PromINIT		10
11	Busmode2#	+3.3V	12
13	LVDSSYNCA	Busmode3#	14
15	+3.3V	Busmode4#	16
17	LVDSSYNCB	GROUND	18
19	TCLKA	TCLKB	20
21	GROUND	LVDSSYNCC	22
23	TCLKC	+3.3V	24
25	LVDSSYNCD	SEREN*	26
27	+3.3V	TCLKD	28
29	LDC0	GROUND	30
31	LDC2	User Defined	32
33	GROUND	LDC1	34
35	PromCCLK	+3.3V	36
37	GROUND	LDC3	38
39	LDC4	GROUND	40
41	+3.3V	LDC5	42
43	LDC6	GROUND	44
45	LDC8	LDC7	46
47	GROUND	LDC9	48
49	LDC10	+3.3V	50
51	LDC12	LDC11	52
53	+3.3V	LDC13	54
55	LDC14	GROUND	56
57	LDC16	LDC15	58
59	GROUND	LDC17	60
61	LDC18	+3.3V	62
63	GROUND	LDC19	64

Source Board Connector P3

Pin	Signal	Signal	Pin
1	LDA0	GROUND	2
3	GROUND	LDA1	4
5	LDA2	LDA3	6
7	LDA4	GROUND	8
9	V (I/O)	LDA5	10
11	LDA6	LDA7	12
13	LDA8	GROUND	14
15	GROUND	LDA9	16
17	LDA10	LDA11	18
19	LDA12	GROUND	20
21	V (I/O)	LDA13	22
23	LDA14	LDA15	24
25	LDA16	GROUND	26
27	GROUND	LDA17	28
29	LDA18	LDA19	30
31	LDB0	GROUND	32
33	GROUND	LDB1	34
35	LDB2	LDB3	36
37	LDB4	GROUND	38
39	V (I/O)	LDB5	40
41	LDB6	LDB7	42
43	LDB8	GROUND	44
45	GROUND	LDB9	46
47	LDB10	LDB11	48
49	LDB12	GROUND	50
51	GROUND	LDB13	52
53	LDB14	LDB15	54
55	LDB16	GROUND	56
57	V (I/O)	LDB17	58
59	LDB18	LDB19	60
61		GROUND	62
63	GROUND	LVDS-DEN	64

Description of above signals.

The LVDS devices are grouped into four pairs; (A,B,C & D), with each pair connected to a FPGA on the mother board.The upper half of each pair (H) will use data bits numbered 19..10, and the lower half (L) will use data bits numbered 9..0.

Signal	**Description**	**Direction**
LVDS-PWDN*	Power down	from DSS
LVDSSYNC[A..D]	Send Sync code (for each LVDS serialiser pair)	from DSS
TCLK[A..D]	Tx clock in (for each LVDS serialiser pair)	from DSS
DBID-[1..4]	Board Serial number. 'Jumperd' to ground.	to DSS
User Defined	Used by other modules	to/from DSS
DisMotherProm[1,2]	Tied together	to/from DSS
PromDATA	FPGA DIN	to DSS
PromDONE	FPGA DONE	from DSS
PromINIT	FPGA INIT	from DSS
PromCCLK	FPGA CCLK	from DSS
SEREN*	EEPROM write enable	from DSS
+3.3V	Power	from DSS
LD[A..D][0..19]	Tx Data in	from DSS
LVDS-DEN	Enable Tx Driver	from DSS
+5V	Power (not used)	from DSS

Link start-up sequence

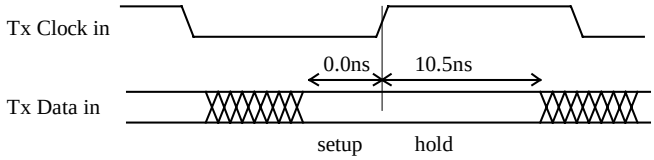
LVDS-DEN must be active with LVDSTxCLK running before
LVDS-PWDN* signals are taken high at least 1us after power up.

LVDSSYNC forces the transmitter to send Sync patterns and must be active for 1024 clock cycles or until the associated receiver indicates it's alignment with the transmitter by asserting it's LVDSLock* signal.

LVDS-PWDN* signals may be pulsed low for 1us to reset the devices.

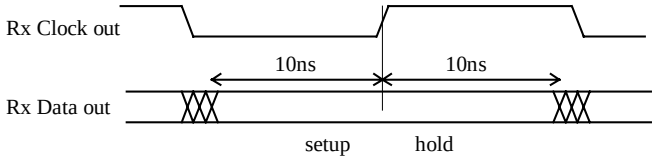
Timing Requirements for DSS Module / DSS FPGA

Tx Data and clock must be supplied to meet the following minimum requirements:



Rx Data from the LVDS deserialisers will be out of phase with the receiving DSS module clock, and such timing will be a function of cable length. The DSS should account for any such arbitrary but fixed timing by using the associated Rx clock signal provided by each deserialiser. (The timing may be determined by scanning each clock using one of the TTC clocks which are programmable in 1ns steps)

Rx Data and clock will be presented to the motherboard as follows:



Configuration PROM for XILINX FPGA.

A 20pin PLCC socket is provided for either a XILINX XC1701L OTP PROM or an ATMEL AT17LV010 EEPROM. The EEPROM may be reprogrammed from the DSS VME interface. The four Motherboard FPGAs are loaded in parallel with the same configuration data, and so only require about 0.6 Mbit of storage. Note the ATMEL AT17LV010A EEPROM has a different pinout.

LVDS device clock control signals

RCLKF/R and TCLKF/R clock control will hardwired on the Daughter Cards. (The G-Link devices do not have this function.)

V(I/O) supply

Not used.

Busmode Signals

Not used.

Estimated Power Consumption

Source Module: < 500mA @ 3.3 V

CPM Testing with DSS module

The LVDS modules and DSS modules will be used inside the existing CPM test system at Birmingham:

Concurrent Technology CPU crate running Linux and HDMC test environment.
Bit3 VME - VME Adapter D16 A24 into 9U CPM crate
TTCVi / Rx system providing sychronous clocks to CPM and DSS.

A single CPM receives 80 LVDS links. Each LVDS daughter card drives 8 such links. Therefore , 10 LVDS source cards are needed , mounted on 5 DSS mother boards.

Software

The cable connection to the CPM provides the following arrangement within the DSS memory.

	Bits 19..10	Bits 9..0
Memory A	AH - Serialiser input QM	AL - Serialiser input QL
Memory B	BH - Serialiser input RM	BL - Serialiser input RL
Memory C	CH - Serialiser input QM	CL - Serialiser input QL
Memory D	DH - Serialiser input RM	DL - Serialiser input RL

Acronyms used.

LVDS	Low Voltage Differential Signalling
OTP	One Time Programmable
EEPROM	Electrically Erasable Programmable Read Only Memory
FPGA	Field Programmable Gate Array
CMC	Common Mezzanine Card
JTAG	Joint Test Action Group