Requirements for the LVDS Transmitter and Receiver Daughter Cards for the DSS Module

Draft 2.0

1. Scope

This document outlines the requirements and specification for a CMC card to level translate between CMOS and LVDS signals. This card will be compatible with the GTM and the DSS modules.

2. Related Documents.

2.1 DSS and GTM at http://www.te.rl.ac.uk/esdg/atlas-flt/

3. Requirements and Specifications

- 33 differential I/O pairs (32 data + one clock) or 66 single ended
  - Termination between the pair of signals (see figure 2)
  - Track impedance differential 100 Ω or two 50 Ω transmission lines
- The design will be based on Xilinx Virtex-E FPGA (XCV300E-BGA432)
  - This allows the card to be a transmitter or receiver
  - Can generate other I/O standards (LVCMOS, PECL, BLVDS, etc)
    - Use I/O banks 4 and 5 with an option to supplying 3V3, 2V5 or 1V8 for Vcco
- Series terminated signals (47 Ω) driving the DSS FPGAs via the CMC connector
  - Track impedance 75 Ω
- 3 x CMC connections (J1 to J3) as per DSS specification
  - http://www.te.rl.ac.uk/esdg/atlas-flt/
- J4 CMC as per GTM specification (direct VME access)
  - http://www.te.rl.ac.uk/esdg/atlas-flt/
- I/O between FPGA and CMC connectors to be PCI compliant
- One EEPROM (XC18V01VQ44C) for DSS FPGA configuration
- One EEPROM (XC18V01VQ44C) for the on board (CMC) FPGA configuration
- JTAG access to program the EEPROMs in-system + access to the FPGA
- Power
  - 5V and 3V3 from the CMC connectors
  - 1V8 and 2V5 from on board linear regulators using the 3V3 supply

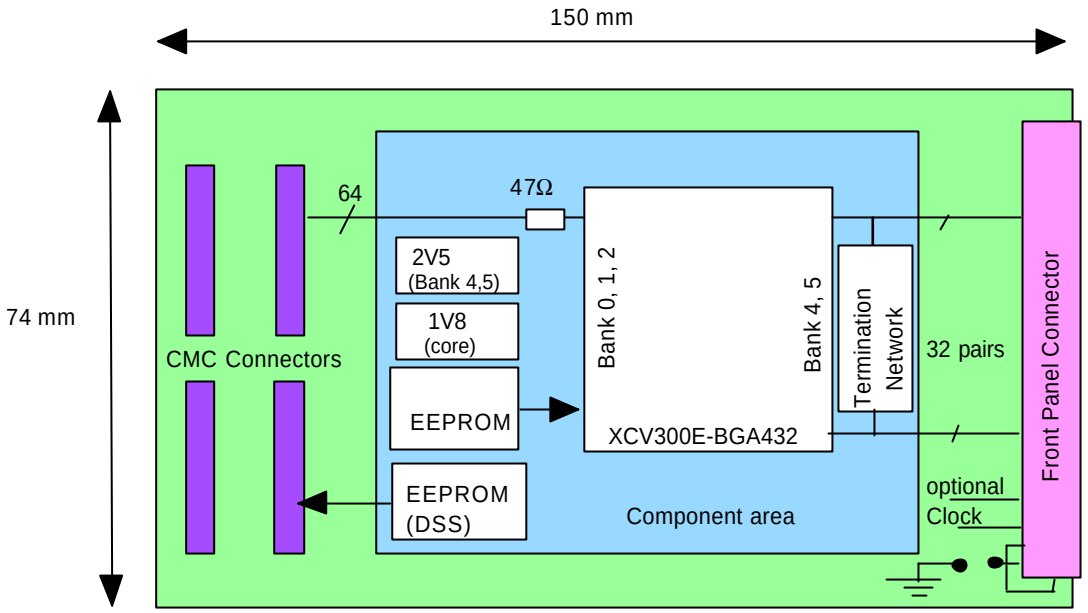


Figure 1: Block diagram of the I/O CMC card

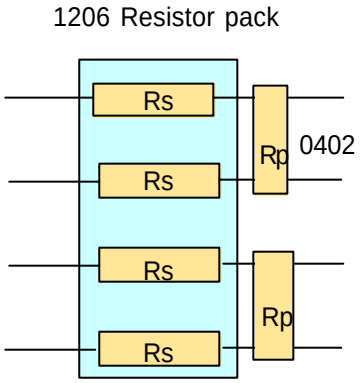


Figure 2. Termination networks

Assemble appropriate network depending on transmitter/receiver or CMOS, LVDS, PECL etc. Use type 1206 resistor pack with type 0402 resistors across for the termination network. Table below shows the resistor values for different I/O standards.

I/O Type	**Rs** W	**Rp** W
LVDS Receiver	0	100
LVDS Transmitter	165	140
BLVDS	47	100
Single ended CMOS, LVTTL	47	open
PECL Receiver	0	100
PECL Transmitter	100	187

Table 1: Resistor Values

4. Front Panel Connector and display

- Standard 68 way SCSI III connector (AMP 787190-7)
  - See following page for pin definition
- LEDs (green)
  - Three power LEDs (3V3, 2V5 and 1V8)
  - FPGA configuration Done
  - LVDS
  - CMOS
  - Tx
  - Rx

5. Benefits using a FPGA

- One PCB design for different I/O standards, receivers and transmitters
- Can load fixed test patterns from the FPGA on the CMC card instead of the DSS if required.
- Can introduce delays in different paths to test synchronisation issues
- Implement PCI interface with a PCI core

6. Number of cards required (10 ?)

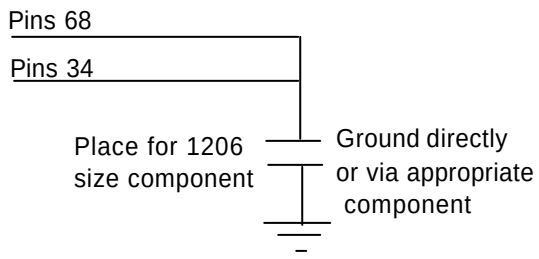
- Two of each LVDS transmitter and receiver?
- Two of each CMOS transmitter and receiver?
- Two spares

68-Conductor SCSI Connector Differential Pin Pairs

PIN #	Signal	PIN#	Signal	PIN#	Signal	PIN#	Signal
1	+Signal 0	35	-Signal 0	18	+Signal 17	52	-Signal 17
2	+Signal 1	36	-Signal 1	19	+Signal 18	53	-Signal 18
3	+Signal 2	37	-Signal 2	20	+Signal 19	54	-Signal 19
4	+Signal 3	38	-Signal 3	21	+Signal 20	55	-Signal 20
5	+Signal 4	39	-Signal 4	22	+Signal 21	56	-Signal 21
6	+Signal 5	40	-Signal 5	23	+Signal 22	57	-Signal 22
7	+Signal 6	41	-Signal 6	24	+Signal 23	58	-Signal 23
8	+Signal 7	42	-Signal 7	25	+Signal 24	59	-Signal 24
9	+Signal 8	43	-Signal 8	26	+Signal 25	60	-Signal 25
10	+Signal 9	44	-Signal 9	27	+Signal 26	61	-Signal 26
11	+Signal 10	45	-Signal 10	28	+Signal 27	62	-Signal 27
12	+Signal 11	46	-Signal 11	29	+Signal 28	63	-Signal 28
13	+Signal 12	47	-Signal 12	30	+Signal 29	64	-Signal 29
14	+Signal 13	48	-Signal 13	31	+Signal 30	65	-Signal 30
15	+Signal 14	49	-Signal 14	32	+Signal 31	66	-Signal 31
16	+Signal 15	50	-Signal 15	33	Clock1	67	Clock1
17	+Signal 16	51	-Signal 16	34	Ground [2]	68	Ground [2]

Note 1. Optional clock (can be selected via solder blobs on board)

Note 2. Ground



Note 3. Connector Screen also should have a grounding (chassis ground) scheme similar to pin 68, 34.