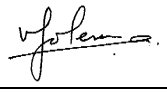
Project Specification

Project Name: Generic Test Module

Version 1.0

June 2000

Approval	Name	Signature	Date
Project Manager	**V. Perera**		**01 June 2000**

Distribution for all updates:

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1. Scope

A general-purpose motherboard will be designed to test the ATLAS and CMS trigger algorithms implemented on FPGAs. The module can be used stand-alone or data can be brought onto the motherboard via daughter boards to meet different requirements.

2. Related Projects and Documents

2.1 DSS specification version 2d, http://www.te.rl.ac.uk/esdg/atlas-flt/
2.2 Draft Standard for a Common Mezzanine Card Family: CMC, P1386/Draft 2.0 April 4, 1995.
2.3 TTCrx Reference Manual, J. Christiansen, *et al*, CERN-ECP/MIC, Version 3.0, October 1999
2.4 Specification of the 'G-Link' Daughter Boards for the 'DSS' Test Platform, R.Hatley
2.5 LVDS Source and Sink CMC Daughter Boards for the DSS Module, R. Staley.
2.6 20-85 MHz Channel link with FPGA for I/O processing, A. J. Maddox

3. Technical Aspects

The motherboard will be a 6U VME module with daughter card positions for two single CMC standard daughter cards and a timing daughter card

3.1 Requirements and Specifications

The generic test module will comprise of a motherboard and daughter card (see section 3.3) combination. The motherboard will be 6U VME form factor, and the daughter cards will comply with the Common Mezzanine Card (CMC) Family form factor.

3.2 Motherboard

The 6U VME motherboard will implement functions such as:

- Timing and trigger control via TTCrx module (CERN TTCrx Test Board compatible)
- VME functions (A32/A24, D32/D16, interrupt etc) implemented on Xilinx Virtex XCV 300E — VME functions implemented as required by the application.
- Two blocks of 64Kx 128 Dual-port RAMs for source of test data and to sink test data or to be used as look-up tables.
  To test the algorithms, the on board dual-port RAMs can be used as a source of test data and to record the results. Alternatively appropriate daughter cards can be used to transfer data in and out of the module.
- Two Xilinx Virtex-E (600-2000) FPGAs for Algorithm evaluation (Processor FPGA)
  - to evaluate the 160 Mbit/s Serialiser (ATLAS)
  - to evaluate the CP algorithm (ATLAS)
  - to evaluate the sort algorithm (CMS)
- Status and Control registers implemented on FPGAs as required
- FPGA configuration via EEPROM or other in-system methods (see 3.2.7.8)
- Four CMC connectors per CMC position (see pin definitions in section 3.2.10)
- Appropriate Power (5V, 3V3, 1V8)
- Appropriate test points and ground points

3.2.1 Signal Connectivity

Figure 1 shows a block diagram of the Generic Test Module showing connectivity between various devices on the motherboard.

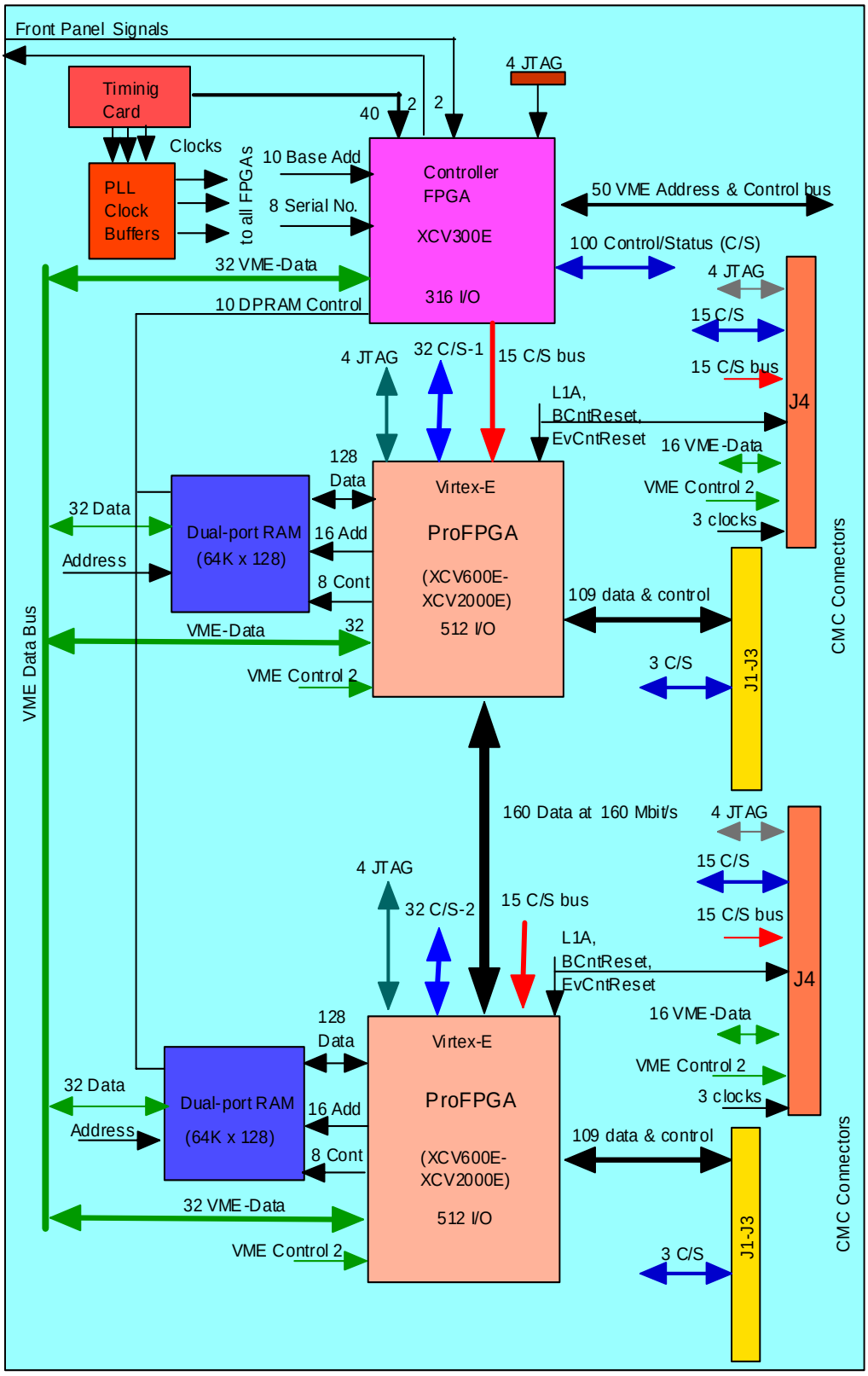


Figure 1. Generic Test Module - Motherboard Block Diagram

3.2.1.1 Controller FPGA

1. 40 signals (see appendix A) from the CERN TTCrx Test Board are fed on to this FPGA and any signal can be made available to the two other FPGAs and on the fourth CMC connector via C/S lines or the C/S-bus signals.
2. 100 Control and status register enable signals (C/S) are distributed onto the two FPGAs as well as the CMC connectors point-to point.
3. 15 control and status signals are bused (C/S bus) to ProFPGAs and to the daughter cards.
4. 10 controls for dual-port RAMs
5. 50 VME bus signals (see appendix B) are used for decoding and controlling the module
6. 10 Base address and 8 for Serial number
7. 3 clocks from the TTCrx (Clock40, clock40Des1, clock40Des2)
8. 2 inputs and 2 outputs from front panel. One input could be used as an external clock
9. 32 bit VME data is available for registers within the FPGAs
10. Connection to JTAG (4)

3.2.1.2 Processor FPGAs (ProFPGA)

1. 152 signals (16 address, 8 control, 128 data) interfacing to dual-port RAM
2. 109 I/O signals interfacing to the CMC connectors
3. 32 bit VME data & 2 VME controls for implementing status and control registers
4. 160 signals between the two processor FPGAs at 160 Mbit/s. A subset of this (an I/O block) will connected to the appropriate I/O reference voltage to evaluate different I/O technologies.
5. 3 signals directly from TTCrx (L1A, BCntRest, EvCntReset)
6. 4 clock signals (three from TTCrx one from front panel)
7. 47 signals (32 C/S, 15 C/S bus) from controller FPGA
8. Connection to JTAG (4)

3.2.1.3 CMC connectors

1. Connection to JTAG (4)
2. 16 VME data + two controls
3. 18 control and status (C/S) from Control FPGA
4. 109 data, control/status lines to ProFPGA
5. 15 control status bused signals (C/S bus)
6. 3 signals directly from TTCrx (L1A, BCntRest, EvCntReset)
7. 4 clock signals (three from TTCrx one from front panel)

3.2.1.4 Other Connections

1. Front Panel (see section 3.2.8)
2. JTAG (see section 3.2.8.7)

3.2.2 FPGA Implementation

There are three FPGAs on the module. One will be implementing the VME functions (controller FPGA), and the other two will be used for 'data processing' (evaluating algorithms) functions.
The controller FPGA will be XCV300E, BG432 device with a common footprint to upgrade to a XCV600E device if required for a future application.
Depending on the application, the two data processing FPGAs (proFPGAs) could be any device from XCV600E to XCV2000 with FG680 foot-print.

3.2.3 Dual-port RAM

Two blocks of 64K x 128 (made up of 64K x 16) wide dual-port memory will be used for test data buffers or as look-up tables. One port will be interfaced to VME and the other to a ProFPGA. The maximum operating frequency of these devices will be 100 MHz.

3.2.4 VME Logic

All VME related logic such as; address decoding, memory addressing, and any other controls and status functions required will be implemented on the controller FPGA.
All the signals required for implementing A32/A24, D32/D16, interrupts, block transfers etc will be routed to the controller FPGA, however initially only A24, D32 will be implemented

3.2.5 Clock Distribution

A plug-in daughter card (CERN TTCrx Test Board) will generate the TTC signals by using a TTCrx chip.
A custom timing card (same footprint as the CERN TTCrx Test Board) is also available which will generate the clocks for initial tests if required.
The clock signals will be fanned out using PLL clock buffers with clock jitter better than 100 ps peak-peak to each of the FPGA.
For flexibility, one of the user defined inputs (3.2.8) will also be connected to a dedicated clock input of the FPGAs if an external clock is required. (See Figure 2)

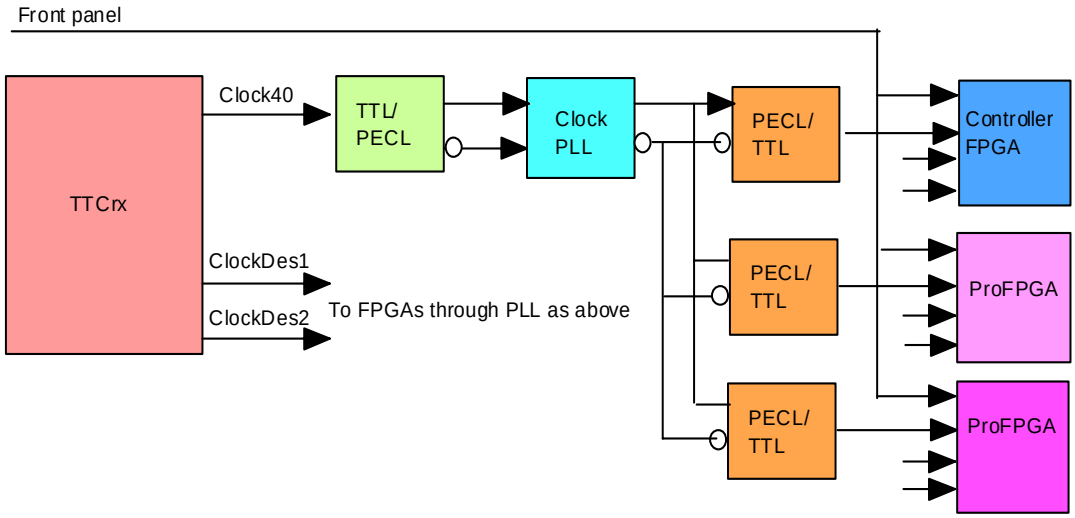


Figure 2. Clock Distribution to FPGAs

3.2.6 Component Height Restrictions on the Motherboard

The component height restrictions and exclusion zones are shown in figure 3.

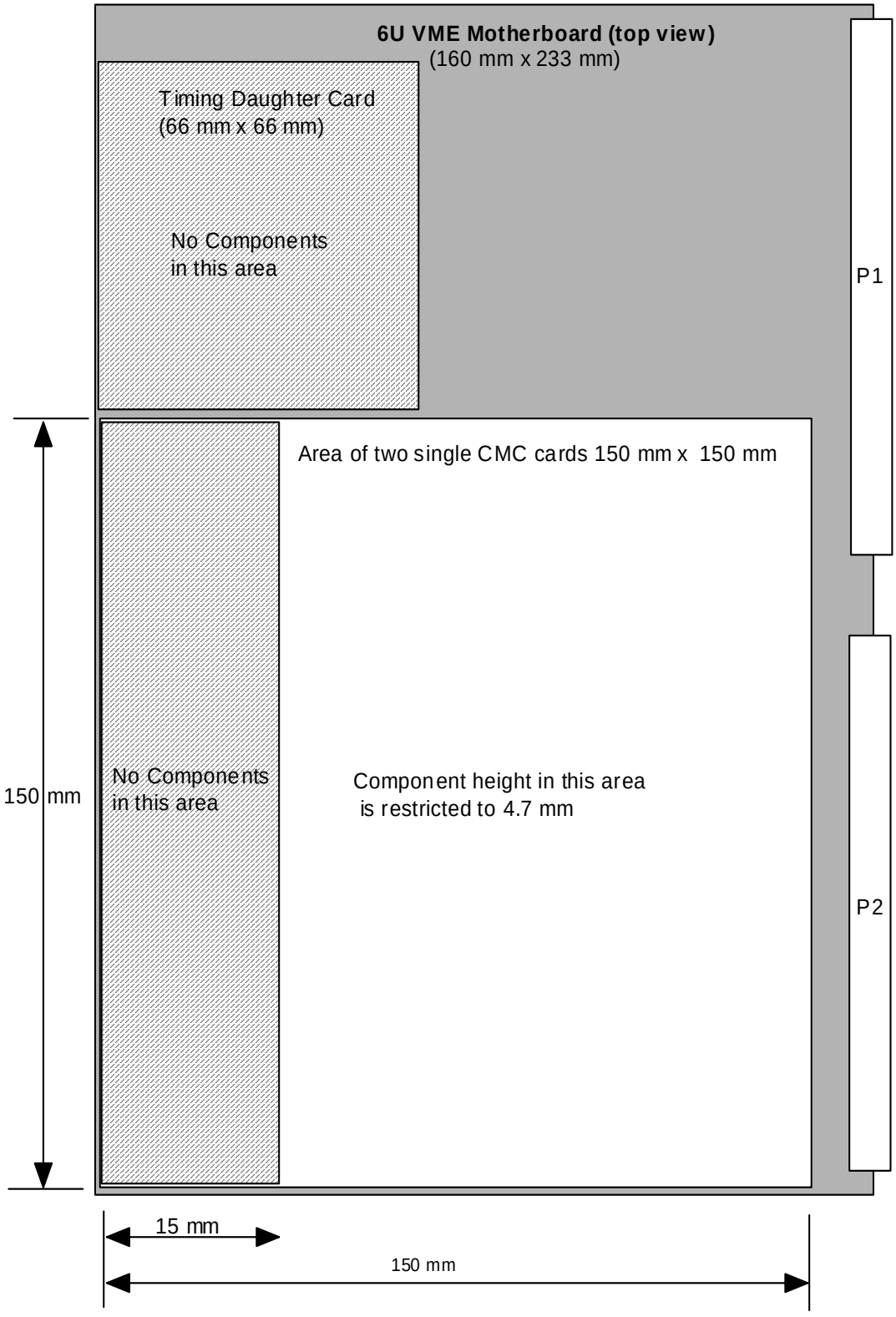


Figure 3. Motherboard Component Placement Restrictions (not to scale)

3.2.7 Signal Handling on the Motherboards

The source modules will terminate the signals using series termination (Rs) for a 75 Ω track impedance. Since the same pins of the FPGA are used when in sink mode or in source mode, the series resister (Rs) at the FPGA end will be present in both modes.

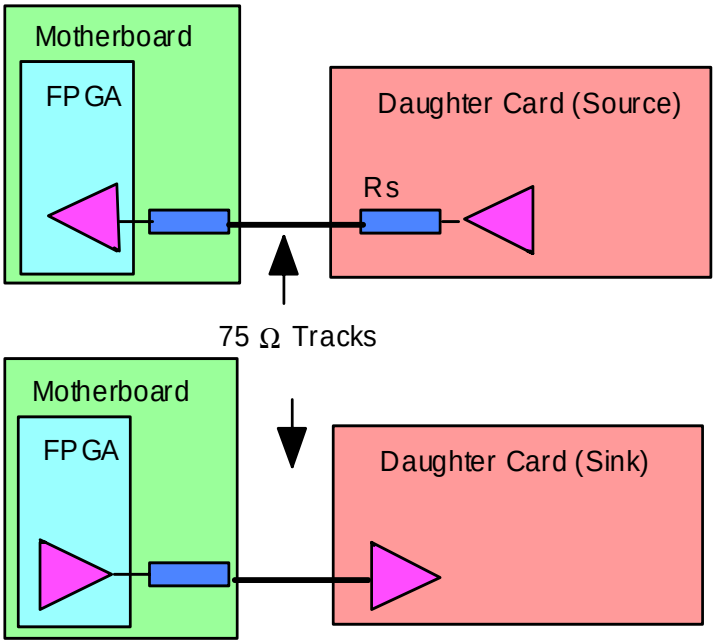


Figure 4. Source Termination

The following table indicates the minimum and maximum values of the signal through the CMC connectors. All signals are TTL compatible

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Drive Low/High	I_{OL}/I_{OH}			24	mA
Output Low Voltage	V_{OL}			0.4	V
Output High Voltage	V_{OH}	2.4			V
Input Low Voltage	V_{IL}			0.8	V
Input High Voltage	V_{IH}	2.0		3.3	V
Clock	CLK	-	-	40	MHz

Table 1. Operating Conditions

3.2.8 Front Panel Input and Outputs

3.2.8.1 Front Panel Inputs

Four signals (two inputs and two outputs) are routed from the front panel to the controller FPGA. Signal levels will be selectable between low voltage PECL (LV-PECL) and LVDS.

Description	Logic	Connector
TTCin	Optical	ST
User defined input-1	Balanced LV-PECL/LVDS	2 Pin Harwin or similar
User defined input-2	Balanced LV-PECL/LVDS	2 Pin Harwin or similar

3.2.8.2 Front Panel Outputs

Description	Logic	Connector
User defined output-1	Balanced LV-PECL/LVDS	2 Pin Harwin or similar
User defined output-2	Balanced LV-PECL/LVDS	2 Pin Harwin or similar

3.2.8.3 Front Panel Monitoring (LEDs)

The LEDs will be located at the top of the front panel.

Description	Signal name	Colour
+5 Volts		Green
+3.3 Volts		Green
+1.8 Volts		Green
System clock is active	SYSCLK	Green
Controller FPGA Loaded	ControllerDone	Green
FPGAs Loaded	PromsDone	Green
VME active	ModuleSel	Yellow
User defined input-1		Red

Note: 1 Fast signals must be stretched so that they will light the LEDs for long enough to be seen.
2. PromsDone will be logical AND of all Done signals except for the Controller FPGA Done signal

3.2.8.4 Rear Panel Input and Outputs

1) VME P1 Connector
2) VME P2 Connector

3.2.8.5 Power Requirements

3V3 and 1V8 are derived from the +5V rail.

Voltage rail	Maximum. Current
+5V	9A

3.2.8.*6 Ground Points*

Ground points will be provided for scope probe grounding in exposed areas of the motherboard.

3.2.8.7 Test and Set-up Points

1. There will be logic analyser probe points on various data paths to aid in debugging the module.
2. JTAG boundary scan port **- a** single JTAG chain through all JTAG compatible devices will be provided for testing the module via boundary scan as well for configuring the FPGAs (See Figure 5).

3.2.7.8 Configuring the FPGAs

Configuration is the process of loading the design bit-streams into the FPGA internal configuration memory

The FPGAs on this module can be configured in at-least six different ways:

1. Serial EEPROM
2. JTAG boundary scan
3. Individually via Xchecker cable
4. Xchecker chain (See figure 6)
    1. Put FPGAs to slave serial mode
    2. Link A-B
    3. Link C-D
    4. Connect PC download cable to Xchecker-C connector
5. Via VME register in serial mode
    1. Put FPGA to slave serial mode
    2. Link E-F
    3. Use the appropriate bits form the register to control Prog, Init, Done, Clk and D0
6. Via VME register in parallel mode (figure 7)
    1. Put FPGA to selectMAP mode
    2. Link E-F
    3. Use the appropriate chip select (CS) to enable device for configuration
    4. Use the appropriate bits form the register to control Write, Busy, Prog, Init, Done, Clk and D0-D7

Notes: 1. For all methods except for configuration via serial EEPROM, the EEPROMs must be removed from the boards.
2. For 5 and 6 , the software drivers must be developed by the users

The FPGA Mode pin M0, M1 and M2 must be set as shown below.

Configuration Mode	M2	M1	M0
Serial EEPROM (Master Serial)	0	0	0
JTAG boundary scan	1	0	1
Xchecker (Slave Serial)	1	1	1
VME serial (Slave Serial)	1	1	1
VME parallel (SelectMAP)	1	1	0

Table 2. Mode Pins on FPGAs

3.2.7.8.1 Controller FPGA

The controller FPGA can be configured via the JTAG chain (see figure 5), Xchecker port or via an EEPROM

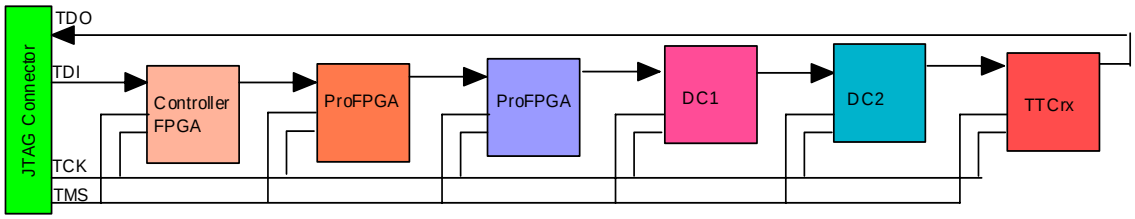
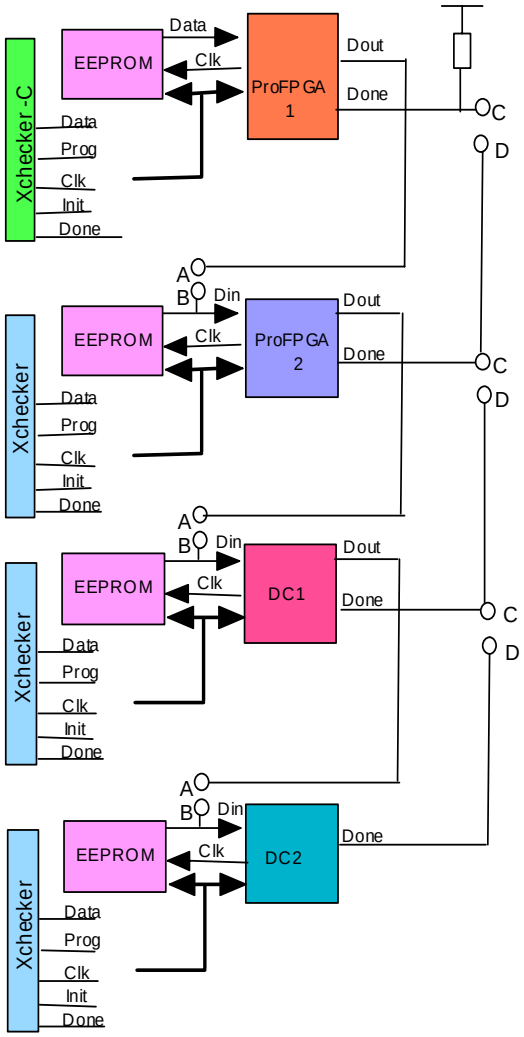


Figure 5. JTAG Chain

3.2.7.8.2 ProFPGAs and the FPGA the Daughter Cards

The ProFPGAs as well as the FPGA on the daughter card can be configured in any of the above methods.



Done, Init, clk, Prog signals should be common

Figure 6. Xchecker Port/Chain

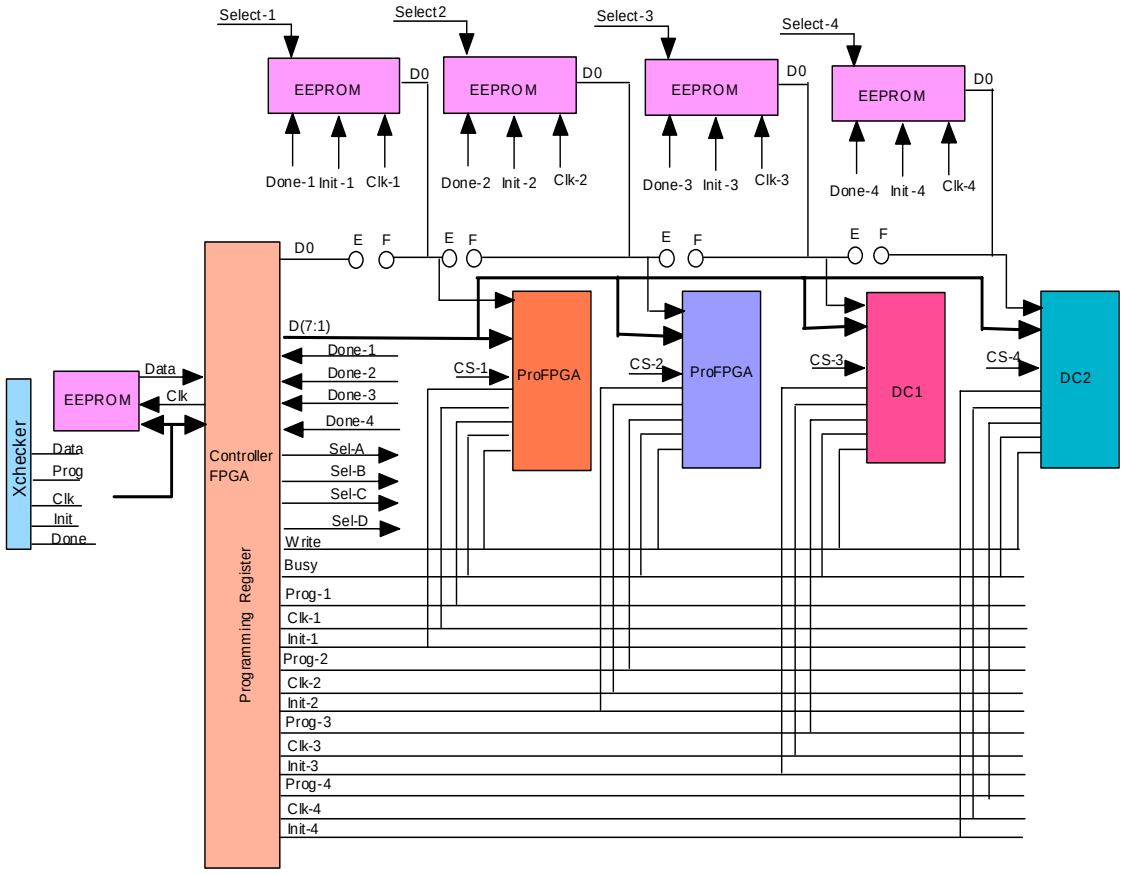


Figure 7. EEPROM and VME Programming Mode

Note: 1. Details of the programming register is given in section 3.2.9.3.7
2. Make sure D0-D7 uses the dedicated pins on the Xilinx for parallel programming, signals and they are allocated within the C/S- Bus signals

3.2.7.8.3Programming the EEPROMs

All EEPROMs other than the EEPROM associated with the Controller FPGA can be programmed in system via the VME program register by controlling the appropriate pins such as the data, clk, CE* (Int), OE* (Done), and the Select pin.

3.2.9 Programming Model

3.2.9.1 Guidelines

These are to aid the software control of the module.

1. All registers can be read by the computer, hence there are no 'write only' registers.

   1.1 All Status Registers shall be Read-Only registers.
   1.2 All Control Registers shall be Read/Write registers.

2. If the computer tries to read or write a value, which the module itself is able to modify at the same time, the data integrity cannot be guaranteed. The only exception been the Control Register and the Status Register. Therefore it is recommended that before any software tries to read or write to any registers the status of the module should ascertained by reading the Status Register.

3. When the address space occupied by the module is accessed, it will always respond with a handshake to avoid a bus error.

4. The power-up condition of all registers will be all zeros, unless otherwise stated.

3.2.9.2 Notation

The names of the registers and bit fields within them are written in *italic*. The names of the signal lines are *underlined italic*. Bit fields are labelled Input to Card and Output from Card rather than Write and Read to make it clear whether it is the card or the computer which is doing the writing.

In this document data fields are defined as follows:
A byte is always an 8-bit field, a word is always 16 bits and a long-word is always 32 bits.

Setting a bit field means writing a 1 to it, clearing it means writing a 0.

3.2.9.3 Memory Map

The module is addressed using an A24 address bus. It uses the addresses up to and including A21 of the A32 address bus. This corresponds to 4096 kilobytes per module. The most significant bits of the address bus can be pre-set by switches to allow the 4096 kilobyte memory space required to sit at any convenient 4096 kilobyte boundary within the four Giga byte A32 address space.

The map shown below may change during the design phase to accommodate any design requirements not foreseen at the time of writing this document. For similar reasons the byte addresses are not allocated at this stage.

All memory on the board is directly mapped into VME address space so as to be conveniently accessible by the computer

Byte Address	Regis ter type	Register Name	Size in bytes	Description
000000	RO	*MotherID*	4	RAL ID, serial number & revision of motherboard
	RW	*MotherCR*	4	Control Register
	RO	*MotherSR*	4	Status Register
	RW	*Timing_Reg*	4	Clock Phase adjustment
	RW	*Pulse Register*	4	Generates pulses
	RW	*Programming_Reg*	4	VME 'ISP' programming
	RO	*ContFPGA_Rev*	4	Controller FPGA revision
	RO	*ProFPGA1_Rev*	4	Revision register
	RO	*ProFPGA2_Rev*	4	Revision register
	RW	*Interrupt_Reg*	4	Interrupt Vector
			512	User defined for C/S
			64	User defined for C/S-Bus
		DCData Buffer 1-12	128K (64K x 16) x 12	Reserved for daughter card memory
	RW	*MBData Buffer 1*	256K (64 K x 32)	DC1_Data[127:96]
	RW	*MBData Buffer 2*	256K (64 K x 32)	DC1_Data[95:64]
	RW	*MBData Buffer 3*	256K (64 K x 32)	DC1_Data[63:32]
	RW	*MBData Buffer 4*	256K (64 K x 32)	DC1_Data[31:0]
	RW	*MBData Buffer 5*	256K (64 K x 32)	DC2_Data[127:96]
	RW	*MBData Buffer 6*	256K (64 K x 32)	DC2_Data[95:64]
	RW	*MBData Buffer 7*	256K (64 K x 32)	DC2_Data[63:32]
	RW	*MBData Buffer 8*	256K (64 K x 32)	DC2_Data[31:0]

RO means that the computer can only read the value of this register, writing has no effect either to the value or the state of the module.

RW means that the computer can affect the state of the module by writing to this register.

The module responds to the following VME Address Modifier codes.

AM code	
39	Standard (A24) non-privileged data access
3D	Standard (A24) supervisory data access

3.2.9.3.1 Mother ID Register

The module identification register is used to uniquely identify the module.

Register Bits	Assignment	Description
0-15	RAL ID (2416)	Same for each module type, number recorded in RAL register
16-23	Module Serial number	an unique number assigned to each module
24-27	Issue	Issue number
28 -31	-	Unused

3.2.9.3.2 Mother Control Register

All bit fields are inputs to board. Power-up condition will initially set all control register bits to 0 unless otherwise stated.

Bit	Descriptive Name	Signal name	
0 (LSB)	*Start/Stop Test*	*Start-Test*	
1			
2			
3			

3.2.9.3.3 ***Start/Stop Test***

Bit 0

When a 1 is written to this bit it will start the test sequence.

0 Stops the test sequence
1 Starts the test sequence

This bit will be combined (OR) with a broadcast start signal which will be received from the TTC system and decoded by the TTCrx chip (Brcst[7:6])**.**

Brcst[7]	Brcst[6]	Function
0	0	stop
0	1	start

3.2.9.3.4 Mother Status Register

This is a read-only register.

Bit	Descriptive Name	Signal name	
0 (LSB)	*ProFPGA-1 Loaded*	*Prom1Done*	
1	*ProFPGA-2 Loaded*	*Prom2Done*	
2	*Module Status*	*Start/Stop*	
3	*TTC Status*	*BroadcastStart*	
4	*TTC Ready*	*TTCReady*	
5			
6			
7			
24-31			Not used

3.2.9.3.4.*1 FPGA Loaded*

Bits 0-2

0	FPGA ‘n’ not loaded
1	FPGA ‘n’ successfully loaded

3.2.9.3.4.2

Bit 3

0	Testing stopped
1	Testing started

3.2.9.3.4.3

Bit 4

0	Testing stopped via TTC broadcast
1	Testing started via TTC broadcast

3.2.9.3.4.4

Bit 5

0	TTCrx is not ready
1	TTCrx is ready

3.2.9.3.4.5

Bit 6 - 31 Not defined

*3.2.9.3.5 Timing_Reg (***only used with a clock source other than the TTCrx)**

Bits 0 - 4 Adjust the phase of the 40 MHz clock, clock40Des 1 in 1 ns steps*
Bits 5 - 9 Adjust the phase of the 40 MHz clock, clock40Des 2 in 1 ns steps*
Bits 10 - 15 Not used

3.2.9.3.6 Pulse Register

Bit	Descriptive Name	Signal name	
0 (LSB)	*Motherboard Reset*	*MBReset*	Pulse (200ns)
1	*TTC Reset*	*TTCReset*	Pulse (200ns)
2	*Reset daughter card 1*	*DC1-RESET*	Pulse (200ns)
3	*Reset daughter card 2*	*DC2-RESET*	Pulse (200ns)
4			
5			

3.2.9.3.6.1 FPGA Reset

Bit 0

When a 1 is written to this bit, a single pulse will reset ProFPGAs to a known power-up state. *FPGA Reset* is always read 0, and writing 0 has no effect.

0	Read value, no effect on writing
1	Resets the module to the initial power-up state

3.2.9.3.6.2 TTC Reset

Bit 1

When a 1 is written to this bit, a single pulse will reset the TTCrx chip to power-up state. *TTC reset* is always read 0, and writing 0 has no effect.

0	Read value, no effect on writing
1	Resets the TTCrx chip

3.2.9.3.6.2 Reset Daughter Card 1,2 (C/S 0)

Bit 2, 3

When a 1 is written to this bit, a single pulse will reset the daughter card to power-up state. *Reset* is always read 0, and writing 0 has no effect.

0	Read value, no effect on writing
1	Resets the daughter card

3.2.9.3.7 Programming_Reg

This register is used to program the two ProFPGAs via VME

Bit 0	Serial data to FPGA (D0)
Bits 7-1	Reserved for parallel configuration (D7-D1)
Bit 8	Sel-A
Bit 9	Sel-B
Bit 10	Sel-C
Bit 11	Sel-D
Bit 12	Done-1
Bit 13	Prog-1
Bit 14	Clk-1
Bit 15	Init-1
Bit 16	Done-2
Bit 17	Prog-2
Bit 18	Clk-2
Bit 19	Init-2
Bit 20	Done-3
Bit 21	Prog-3
Bit 22	Clk-3
Bit 23	Init-3
Bit 24	Done-4
Bit 25	Prog-4
Bit 26	Clk-4
Bit 27	Init-4
Bit 28	Write
Bit 29	Busy
Bit 30	Reserved
Bit 31	Reserved

Sel-A to Sel-D from the VME programmming register will select the appropriate device for programming as follows

Sel-A	Sel-B	Sel-C	Sel-D	Device selected for programming
0	0	0	0	None selected
0	0	0	1	Select-1 (ProFPGA1 EEPROM)
0	0	1	0	Select-2 (ProFPGA2 EEPROM)
0	0	1	1	Select-3 (Daughter Card 1 EEPROM)
0	1	0	0	Select-4 (Daughter Card 2 EEPROM)
0	1	0	1	CS-1 (ProFPGA1)
0	1	1	0	CS-2 (ProFPGA 2)
0	1	1	1	CS-3 (Daughter Card 1 FPGA)
1	0	0	0	CS-4 (Daughter Card 2 FPGA)

3.2.9.3.8 Controller FPGA Revision Register

Specifies the current version loaded into the Controller FPGA

Bits 31-24 Version (Starts at 01)
Bits 23-16 Function code.(see below)
Bits 15-0 "2416" module ID

3.2.9.3.9 ProFPGA Revision Registers (ProFPGA1, Pro FPGA2)

Specifies the current version loaded into the ProFPGA

Bits 31-24 Revision number (Starts at 01)
Bits 23-16 Function code.
Bits 15-0 "2416" (used with the generic test module, therefore this should match with the module ID).

3.2.9.3.9.1 Function Codes (Bits 23-16)

Code (Binary)	FPGA function
"10000000"	VME TYPE
"0100nnn1"	ATLAS source
"0100nnn0"	ATLAS sink
"1100nnn1"	CMS source
"1100nnn0"	CMS sink

nnn provides eight different types of cards, e.g LVDS, G-Link, Channel link, etc.

3.2.9.10 Interrupt Vector

This register is reserved for generating the interrupt vector when interrupts are used

3.2.9.3.11 User defined for C/S

These are user-defined signals mapped from the Controller FPGA to all devices. For example these can be used for enabling daughter card ID register, Control register, Status register, etc.

3.2.9.3.12 User Defined for C/S-Bus

These are user-defined signals mapped from the Controller FPGA and are bussed to all devices. For example these could be used for Parallel Configuring the FPGAs, distributing appropriate TTC signals such as BCID if required.

3.2.9.3.13 DCData Buffers

Reserved for accessing the daughter card memory

3.2.9.3.14 MBData Buffers

Access to motherboard dual-port RAM blocks

3.2.10 CMC Connector Definitions.

3.2.10.1 Connector J1

Pin	Signal	Signal	Pin
1	C/S-0 *(DC-RESET)*	-12V	2
3	GROUND	ProFPGA-18	4
5	ProFPGA-1	ProFPGA-19	6
7	Busmode1#	+5V	8
9	ProFPGA-2	ProFPGA-20	10
11	GROUND	ProFPGA-21	12
13	RefCLK (PCI) or ExtClk	GROUND	14
15	GROUND	ProFPGA-22	16
17	ProFPGA-3	+5V	18
19	V(I/O)-1	ProFPGA-23	20
21	ProFPGA-4	ProFPGA-24	22
23	ProFPGA-5	GROUND	24
25	GROUND	ProFPGA-25	26
27	ProFPGA-6	ProFPGA-26	28
29	ProFPGA-7	+5V	30
31	V(I/O)-1	ProFPGA-27	32
33	ProFPGA -8	GROUND	34
35	GROUND	ProFPGA_28	36
37	ProFPGA_9	+5V	38
39	GROUND	ProFPGA_29	40
41	ProFPGA 10	ProFPGA_30	42
43	ProFPGA_11	GROUND	44
45	V(I/O)-1	ProFPGA_31	46
47	ProFPGA_12	ProFPGA_32	48
49	ProFPGA_13	+5V	50
51	GROUND	ProFPGA_33	52
53	ProFPGA_14	ProFPGA_34	54
55	ProFPGA_15	GROUND	56
57	V(I/O)-1	ProFPGA_35	58
59	ProFPGA_16	ProFPGA_36	60
61	ProFPGA_17	+5V	62
63	GROUND	ProFPGA_37	64

Table 2. CMC Connector J1 pin-out

Note 1. The ProFPGA signals on J1 and J2 connector must be mapped to the PCI signals for pin locking the FPGA pins to implement PCI interface if required for future designs.

3.2.10.2 CMC Connector J2

Pin	Signal	Signal	Pin
1	+12V	PromEnable	2
3	PromCLK	PromProg	4
5	PromDONE	GROUND	6
7	GROUND	PromDATA-D0	8
9	PromINIT	ProFPGA-54	10
11	Busmode2#	+3.3V	12
13	ProFPGA-38	Busmode3#	14
15	+3.3V	Busmode4#	16
17	ProFPGA-39	GROUND	18
19	ProFPGA-40	ProFPGA-55	20
21	GROUND	ProFPGA-56	22
23	ProFPGA-41	+3.3V	24
25	ProFPGA-42	ProFPGA-57	26
27	+3.3V	ProFPGA-58	28
29	ProFPGA-43	GROUND	30
31	ProFPGA-44	ProFPGA-59	32
33	GROUND	ProFPGA-60	34
35	ProFPGA-45	+3.3V	36
37	GROUND	ProFPGA_61	38
39	ProFPGA-46	GROUND	40
41	+3.3V	ProFPGA_62	42
43	ProFPGA_47	GROUND	44
45	ProFPGA_48	ProFPGA_63	46
47	GROUND	ProFPGA_64	48
49	ProFPGA_49	+3.3V	50
51	ProFPGA_50	ProFPGA_65	52
53	+3.3V	ProFPGA_66	54
55	ProFPGA_51	GROUND	56
57	ProFPGA_52	ProFPGA_67	58
59	GROUND	ProFPGA_68	60
61	ProFPGA_53	+3.3V	62
63	GROUND	ProFPGA_69	64

Table 3. CMC Connector J2 pin-out

Note 1. Busmode [4:2]# signals are driven by the motherboard, Busmode 1# is returned by the daughter card to indicate presence of the card.

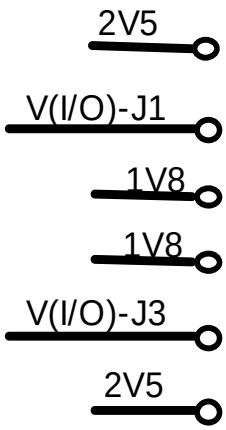
Note 2. The ProFPGA signals on J1 and J2 connector must be mapped to the PCI signals for pin locking the FPGA pins to implement PCI interface if required for future designs

3.2.10.3 CMC Connector J3

Pin	Signal	Signal	Pin
1	ProFPGA_70	GROUND	2
3	GROUND	ProFPGA_90	4
5	ProFPGA_71	ProFPGA_91	6
7	ProFPGA_72	GROUND	8
9	V(I/O)-2	ProFPGA_92	10
11	ProFPGA_73	ProFPGA_93	12
13	ProFPGA_74	GROUND	14
15	GROUND	ProFPGA_94	16
17	ProFPGA_75	ProFPGA_95	18
19	ProFPGA_76	GROUND	20
21	V(I/O)-2	ProFPGA_96	22
23	ProFPGA_77	ProFPGA_97	24
25	ProFPGA_78	GROUND	26
27	GROUND	ProFPGA_98	28
29	ProFPGA_79	ProFPGA_99	30
31	ProFPGA_80	GROUND	32
33	GROUND	ProFPGA_100	34
35	ProFPGA_81	ProFPGA_101	36
37	ProFPGA_82	GROUND	38
39	V(I/O)-2	ProFPGA_102	40
41	ProFPGA_83	ProFPGA_103	42
43	ProFPGA_84	GROUND	44
45	GROUND	ProFPGA_104	46
47	ProFPGA_85	ProFPGA_105	48
49	ProFPGA_86	GROUND	50
51	GROUND	ProFPGA_106	52
53	ProFPGA_87	ProFPGA_107	54
55	ProFPGA_88	GROUND	56
57	V(I/O)-2	ProFPGA_108	58
59	ProFPGA_89	ProFPGA_109	60
61	C/S-1	GROUND	62
63	GROUND	C/S-2	64

Table 4. CMC Connector J3 pin-out

Note: The V(I/O) pins on J1 and J3 should be tracked as shown below for selecting additional voltage pins if necessary for the daughter card use



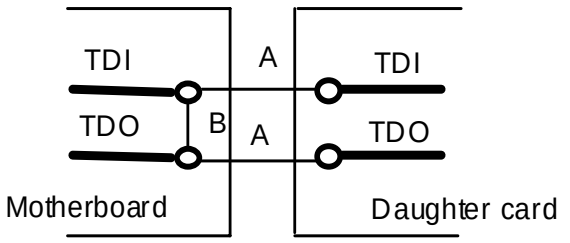
3.2.10.4 CMC Connector J4

Pin	Signal	Signal	Pin
1	VME-DATA_0	VME-DATA_1	2
3	VME-DATA_2	VME-DATA_3	4
5	VME-DATA_4	VME-DATA_5	6
7	VME-DATA_6	VME-DATA_7	8
9	VME-DATA_8	VME-DATA_9	10
11	VME-DATA_10	VME-DATA_11	12
13	VME-DATA_12	VME-DATA_13	14
15	VME-DATA_14	VME-DATA_15	16
17	GROUND	GROUND	18
19	VME-Write*	VME-DS	20
21	L1A	EvCntReset	22
23	BCntReset	C/S-Bus1 (Prog Data-D1)	24
25	C/S-Bus2 (Prog Data-D2)	C/S-Bus3 (Prog Data-D3)	26
27	C/S-Bus4 (Prog Data-D4)	C/S-Bus5 (Prog Data-D5)	28
29	C/S-Bus6 (Prog Data-D6)	C/S-Bus7 (Prog Data-D7)	30
31	C/S-Bus8	C/S-Bus9	32
33	C/S-Bus10	C/S-Bus11	34
35	C/S-Bus12	C/S-Bus13	36
37	C/S-Bus14	C/S-Bus15	38
39	GROUND	GROUND	40
41	Clock40	Clock40Des1	42
43	TDI	TDO	44
45	TMS	TCK	46
47	C/S-4 (DC ID Reg)	C/S-3 (DC Status Reg)	48
49	C/S-6 (DC Control Reg)	C/S-5 (DC DPRAMCE1)	50
51	C/S-8 (DC DPRAMCE2)	C/S-7 (DC DPRAMCE3)	52
53	C/S-10 (DC DPRAMCE4)	C/S-9 (DC DPRAMCE5)	54
55	C/S-12 (DC DPRAMCE6)	C/S-11	56
57	C/S-14	C/S-13	58
59	C/S-16	C/S-15	60
61	GROUND	GROUND	62
63	Clock40Des2	C/S-17	64

Table 5. CMC Connector J4 pin-out

Note 1. ProgData D1-D7 must be used for FPGA parallel configuration.

2. The JTAG chain must be terminated on the motherboard if a daughter card is not in use



Link A for daughter card use
Link B if no daughter card

3.3 Daughter Cards

The daughter cards will implement the physical layer to transmit/receive data up to 80/84 bits wide. The following daughter cards developed for the DSS can be used on this module:

- 960 Mbaud G-link [2.4]
- LVDS 480 Mbit/s serialiser/ de-serialiser [2.5]

New daughter card designs [2.6] must conform to the daughter card connector specification as given in this document (see section 3.2.10)

The new daughter card will have VME access (D16) via the CMC P4.

The recommended registers such as the daughter ID, daughter control register and the daughter status registers will be implemented on the daughter cards, and will be controlled by the motherboard controller FPGA (see section *3.2.9.3)*

The daughter cards can configure the motherboard if required.
When a daughter card is plugged onto the motherboard, the motherboard EEPROM handling the daughter card data will be automatically disabled and the EEPROM on the daughter card will automatically configure the motherboard.

3.3.1 Daughter Card Standard

The daughter card designs must comply with the IEEE P1386/Draft 2.0, 4 April-1995, standard for a Common Mezzanine Card (CMC) family.
The connector definitions and the physical description of the cards are given below.
Figure 8 shows the daughter card dimensions and the connector positions.

The connectors used in these modules will be: (10 mm stand-off)
1. Plug (P) (Molex 53483-0649) on the daughter cards
2. Socket (J) (Molex 52763-0649) on the motherboards

3.3.2 Physical Dimensions

The following diagram shows the physical dimensions for the daughter card.

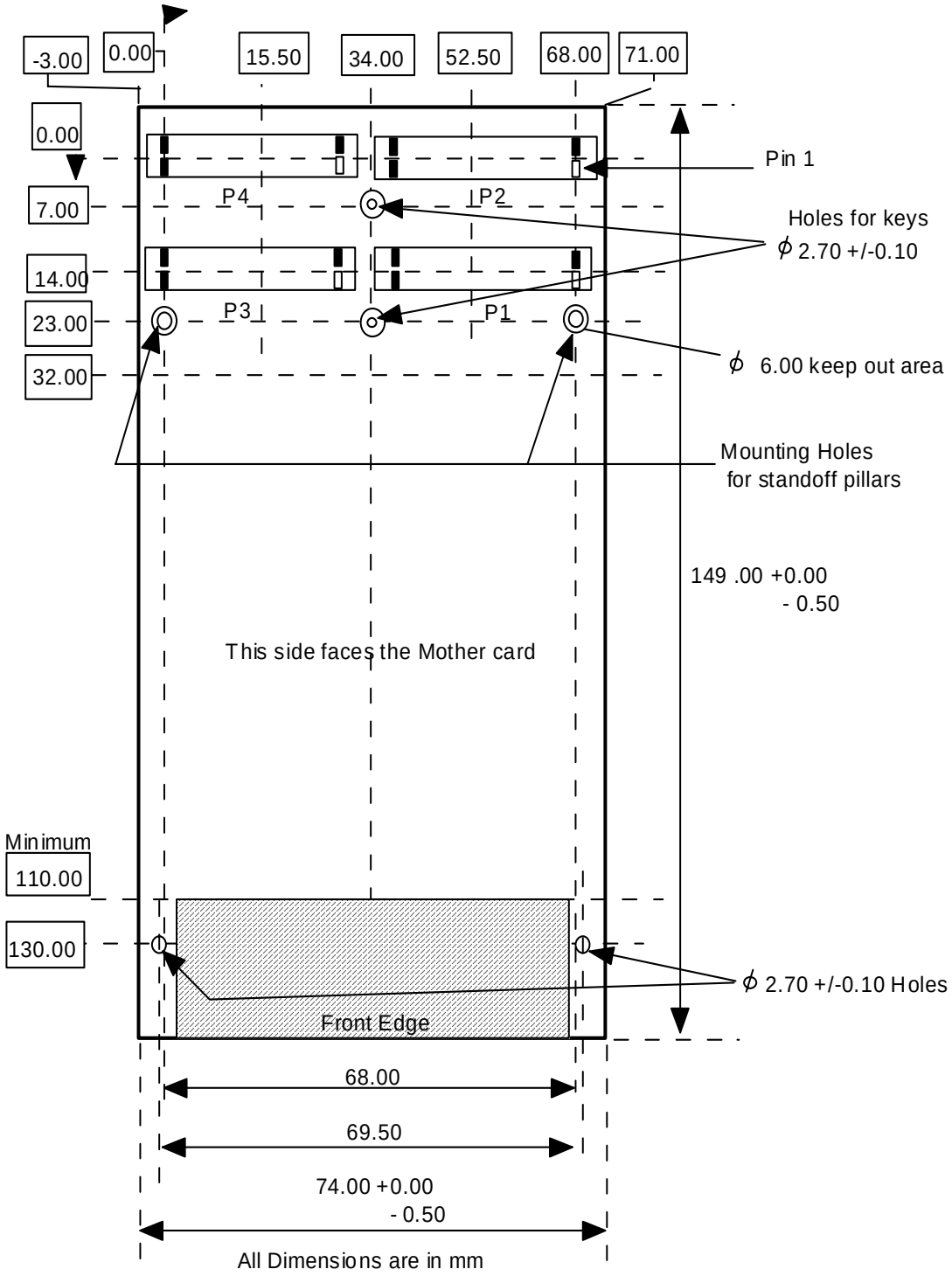


Figure 8. Dimensions for the CMC Daughter cards (not to scale)

3.3.3 Component Height Restrictions

On the side facing the motherboard the component height is restricted to 4.7 mm, except:
1. Where there is an exclusion zone of 34 mm x 6 mm.
2. In the shaded area (68 mm x 33 mm) the component height could be up to 9.8 mm.
On the top side of the card the component height restriction is 3.50 mm including the card thickness (for a VME single width module).

3.3.4 CMC Bezel

For the front bezel and for other mechanical details refer to the IEEE P1386/Draft 2.0, 4 April-1995, standard for a Common Mezzanine Card family.

3.3.5 Signal Handling on the Daughter Cards

Since the signals between the daughter cards and the FPGAs on the motherboard have to travel long distances, the tracks carrying the signals have to be transmission lines and must be terminated appropriately to the characteristic impedance (75 Ω) of these tracks.

3.3.6 Daughter Card EEPROMs

The EEPROMs on the daughter cards should be in a socket.

3.3.7 *Ground Points*

At least one ground point must be provided for scope probe grounding.

3.3.8 Front Panel Input and Outputs

The front panel inputs/outputs to the daughter card will be through the front bezel and will differ from module to module.

3.3.8.1 Front Panel Monitoring (LEDs)

A minimum set of LEDs is recommended for the daughter card. Example VCC, Clock.

Description	Signal name	Colour
Vcc		Green
System clock is active	SYSCLK	Green

3.4 Testing

3.4.1 Test Strategy

1.Stand alone test of the motherboard using the dual-port RAMs
2.Transmitting and receiving data via appropriate daughter cards

3.4.2 Test Equipment

(1) VME crate
(2) 32 bit VME interface
(3) Computer to run software
(4) Logic analyser
(5) Oscilloscope
(6) VME Extenders

3.5 Software

A test engineer from the System Support Group will develop the LabView test software.

Application specific software has to be developed by the customer.

3.6 Manufacturing

An outside manufacturer will carry out the manufacture of the PCBs and the component assembly.

3.7 Installation

The motherboard is designed to be operated in a standard 6U VME crate with a VME P1, P2 backplane. The module will be provided with a front panel containing sockets and monitoring LEDs as described in section 3.2.8, and two slots for CMC modules.

The customer will require a 6U VME crate with backplane, appropriate power and fan-tray to operate the Generic Test Module.

3.8 Maintenance and further orders

This module is expected to be used in testing various prototype and production modules, and may be required by the other collaborating institutes. In the first instance a minimum of four modules will be required, two each for ATLAS and CMS.

4. Project Management

4.1 Personnel

		Telephone	Location
Customer:			
ATLAS	A. Gillman	5521	RAL R1, 1.54
CMS	G.Heath	0117 928 8947	Bristol University
Project Manager:	V. Perera	5692	RAL R68, 2.31
Project Engineer	A. Shah	5030	RAL R68, 2.14

4.2 Deliverables

4.2.1 *To the Customer:*

1. Two modules per customer including appropriate FPGA firmware
2. Specification document
3. Schematics

4.2.2 From the Customer:

None

4.3 Project plan **(Milestones)**

1. Preliminary Design Review (PDR)	start	Q2 2000
2. Final Design Review (FDR)	end	Q2 2000
3. Start Testing	start	Q3 2000
4. Concluding Review (CR)	end	Q4 2000

4.4 Design Reviews

The customer must be present at the PDR and the CR. If the customer wishes, he may attend the FDR.
The progress of the project will be reported on a monthly basis on project monitor forms.

4.5 Training

Training will be carried out as required on the job.

4.6 CAE

Cadence for schematic capture, VHDL and FPGA design tools and LabView for test software.

4.7 Costs and Finance

All manufacturing, assembly and component costs will be charged to FK40000TDD (ATLAS) and FK 65000TDD (CMS)
Staff costs and the component costs will be shared equally between ATLAS and CMS.

4.8 Intellectual Property Rights (IPR) and Confidentiality

All background and foreground Intellectual Property Rights in this project will remain with CLRC. The customer will have unrestricted rights to items listed under deliverables (4.2). If the customer requires other data, then an appropriate protective agreement should be in place before releasing such data.

4.9 Safety

General laboratory safety codes apply.

4.10 Environmental impact

4.10.1 Disposal

If required RAL will dispose of the modules at end of their life.

4.10.2 EMC

Since these are test modules and only to be used in a test environment by the collaborating institutes, the modules will not carry a CE mark. However since the electronics must function as designed, without malfunction or unacceptable degradation of performance due to electromagnetic interference (EMI) within their intended operational environment, the electronics shall comply with specifications intended to ensure electromagnetic compatibility.

4.11 Handling Precautions

Anti-static precautions must be taken when handling the module to prevent damage to components.

Appendix - A

TTCrx signals (40)connected to the Controller FPGA

Signal name	Signal name
Reset* (from The controller FPGA)	dout(7)
bcnt_reset	dout_strb
brcst(2)	dq(0)
brcst(3)	dq(1)
brcst(4)	dq(2)
brcst(5)	dq(3)
brcst(6)	evcnt_hstrb
brcst(7)	evcnt_lstrb
brcst_strb1	evcnt_reset
brcst_strb2	L1a
bcnt_strb	sberr_strb
Clk_L1a	sub_addr(0)
dberr_strb	sub_addr(1)
dout(0)	sub_addr(2)
dout(1)	sub_addr(3)
dout(2)	sub_addr(4)
dout(3)	sub_addr(5)
dout(4)	sub_addr(6)
dout(5)	sub_addr(7)
dout(6)	Ready

Appendix - B

VME signals (50) connected to Controller FPGA

Signal Name	Signal Name
AM0	VME_ADDR(7)
AM1	VME_ADDR(8)
AM2	VME_ADDR(9)
AM3	VME_ADDR(10)
AM4	VME_ADDR(11)
AM5	VME_ADDR(12)
DS (Decoded output signal)	VME_ADDR(13)
DS-DEL (Input to the controller)	VME_ADDR(14)
IACK_OUT	VME_ADDR(15)
IRQ3	VME_ADDR(16)
AS*	VME_ADDR(17)
LWORD	VME_ADDR(18)
BRDSEL* (Decoded board select output)	VME_ADDR(19)
WRITE	VME_ADDR(20)
DS0	VME_ADDR(21)
DS1	VME_ADDR(22)
IACK*	VME_ADDR(23)
IACK_IN*	VME_ADDR(24)
RESET*	VME_ADDR(25)
VME_ADDR(1)	VME_ADDR(26)
VME_ADDR(2)	VME_ADDR(27)
VME_ADDR(3)	VME_ADDR(28)
VME_ADDR(4)	VME_ADDR(29)
VME_ADDR(5)	VME_ADDR(30)
VME_ADDR(6)	VME_ADDR(31)