Report of the Production Readiness Review

JET/ENERGY MODULE

Abstract

The Production Readiness Review of the Level-1 Calorimeter Trigger **Jet/Energy Module (JEM)** was held at Mainz on 14 December 2005. There were presentations and discussion of the module design improvements, performance in a variety of tests, implementation of the recommendations made at the Final Design Review, and plans for the production and testing of final modules and the JEP subsystem.

The reviewers approved production of the JEM following the plans presented, subject to several recommendations.

A list of editorial corrections to the JEM specification document is provided.

Prepared by :	***Checked by :***	***Approved by :***
Eric Eisenhandler, Queen Mary, Univ. of London	**Philippe Farthouat**, CERN **Tony Gillman**, RAL **Kambiz Mahboubi**, Heidelberg **Gilles Mahout**, Birmingham **Richard Staley**, Birmingham	

for information, you can contact :	**Eric Eisenhandler**	Tel. +44 (0)1235 445562 +44 (0)20 7882 5056	Fax. +44 (0)1235 446733	E-Mail e.eisenhandler@qmul.ac.uk

Distribution: EB Members, TDAQ Members, all participants mentioned in the report.

PURPOSE OF THE REVIEW

The purpose of this review was to check that:

- The recommendations of the Final Design Review have been carried out satisfactorily
- Problems arising since the FDR have been addressed, and any resulting design changes are acceptable
- Production planning and quality assurance are adequate, including checks at critical stages
- A comprehensive test plan for production modules has been prepared
- The module is adequately documented

The overall goal was to approve production of the Jet/Energy Module.

PARTICIPANTS IN THE REVIEW

Review Committee	Jet/Energy Module team
Eric Eisenhandler, Queen Mary, London *(chair)*	Uli Schäfer, Mainz
Philippe Farthouat, CERN	Rainer Stamen, Mainz
Tony Gillman, RAL	Attila Hidvégi, Stockholm
Kambiz Mahboubi, Heidelberg	Sam Silverstein, Stockholm
Gilles Mahout, Birmingham	
Richard Staley, Birmingham	
Ex officio	For information

AGENDA AND DOCUMENTATION

The review agenda, with links to all the talks given at the review, is at:

http://agenda.cern.ch/fullAgenda.php?ida=a057784

All the documents for the PRR can be found via the 'documents' link near the top of the agenda; they can also be accessed directly via:

http://agenda.cern.ch/askArchive.php?base=agenda&categ=a057784&id=a057784/documents

The main document for the review was the **JEM Specification** version 1.1d, by Uli Schäfer and Samuel Silverstein. Two other important documents are **JEMtests** version 1.0, which gives details of the tests done since the FDR, and **JEMPlan** version 1.1, which describes the proposed production process and plans for testing the final modules. There is also **Programming Model** version 1.1. The documents page also contains links to design material, circuit diagrams, and information about the firmware, as well as some of the initial comments from the reviewers.

REVIEW OUTCOME

1 INTRODUCTION

The Production Readiness Review for the Jet/Energy Module (JEM) of the ATLAS Level-1 Calorimeter Trigger was held at the University of Mainz on 14 December 2005. The reviewers were Eric Eisenhandler (Queen Mary, London; chair), Philippe Farthouat (CERN), Tony Gillman (RAL), Kambiz Mahboubi (Heidelberg), Gilles Mahout (Birmingham), and Richard Staley (Birmingham). Unfortunately, Stefan Haas (CERN) could not participate. Talks were given by:

- Uli Schäfer (Mainz) on the response to points raised at FDR, post-FDR problems and design changes, and module and system test results
- Attila Hidvégi (Stockholm) on the jet algorithm, its performance, and test results
- Uli Schäfer on plans for production, initial tests, and quality assurance checks on the production modules
- Rainer Stamen (Mainz) on higher-level connectivity and system tests on production modules, and software for carrying out these tests and documenting them

The talks were clear, and answered directly almost all of the points raised at the Final Design Review, which was held in April 2005 (ATC–RD–ER–0028). The reviewers had submitted a number of questions and comments in advance of the review by e-mail. Further points came up during the talks, and during the helpful and constructive discussion that followed. Firm conclusions were reached, leading to a list of recommendations — none very serious — to be carried out as part of the production and testing of the final JEMs. An order for the JEM production can be placed immediately, on the understanding that full production is held off until there are satisfactory test results on the four pre-production modules.

The JEM specification document has been very thoroughly updated. There are a few corrections and improvements needed, and they are specified in detail in Appendix A to this report. It was felt that the description of the jet algorithm could be strengthened with the addition of diagrams and a few technical details; these are included in Appendix A. Appendix B contains a comment on the Programming Model document.

2 SUMMARY OF PRESENTATIONS AND DISCUSSION

2.1 DESIGN CHANGES, TESTING, AND FDR RESPONSES

Uli Schäfer gave a detailed presentation of the design changes and the extensive testing programme since the FDR, as well as a detailed point-by-point description of how the conclusions and recommendations of the FDR have been implemented.

The main design changes were made to reduce noise and crosstalk visible on fan-in/fan-out (FIO) lines on JEM version 1.1, a problem that only became apparent after the FDR. Although this did not actually cause data transmission errors during tests, the level of noise and crosstalk was uncomfortably close to signal thresholds, and there were concerns that full crates of JEMs in a noisier environment might well have errors. The re-designed JEM 1.2 motherboard has increased the number of PCB layers to 14, increased the spacing of the FIO and merger tracks on the board, improved the grounding of the input daughter card connectors, and upgraded the Jet FPGA chip to XC2V3000 in order to allow use of an external voltage reference for the jet FIO lines. The Jet FPGA now uses HSTL sensing instead of CMOS. These measures

have succeeded in reducing the noise and crosstalk to acceptable levels. In addition, as suggested at the FDR, unused LVDS inputs are now left open, and unused TTC bunch-counter bus drivers in the TTCrx chip are turned off.

There were also some changes to the daughter card designs. Minor changes to the Input Module include improved grounding, to help with the noise problems mentioned above. The Readout Module now has a LED indicating link-ready, and has become a 4-layer PCB with controlled-impedance tracking. The Control Module is now a 6-layer PCB and includes the standard Calorimeter Trigger CANbus microcontroller configuration for monitoring voltages and temperatures.

The production design, JEM 1.3, is very similar to JEM 1.2. A couple of minor errors will be corrected, including a misunderstanding concerning the orientation of the mounting holes for the TTC decoder daughter card. More robust extraction handles will be used.

Uli then described the tests that have been done. System tests requested at the FDR included the LVDS input signals with a large number of inputs and heavy FIO traffic on the backplane, and the FIO backplane signals under similar conditions. In addition, other tests were to be repeated with more 'stressful' data patterns. This programme was carried out in the system test rig at RAL, and overnight runs were error-free with very impressive statistics on bit-error rate limits.

The main limitation of these tests is that only one of the JEMs tested was version 1.2, but for FIO testing versions 1.1 and 1.0 are compatible. However, in order to be very sure that the new design is safe, it is proposed to build four pre-production modules (JEM 1.3) and do a test with as full a crate as possible (including some CPMs) before proceeding to full production, as recommended at the FDR.

The latency has been measured to be 182 ns for the energy-sum logic and 257 ns for the jet logic, to be compared with specified 'envelopes' of 200 ns and 250 ns, respectively. However, the jet latency can probably be reduced — see sect. 2.2.

One test requested at the FDR, using final jet firmware in the Common Merger Module (CMM) downstream of the JEM, has not yet been done because the required CMM firmware is still not finished. This test is planned for January/February 2006, when the firmware is expected to be available.

A grounding scheme has been mutually agreed between the PreProcessor Module, Cluster Processor Module and the JEM, but it has not yet been checked by Georges Blanchot.

Power inrush is a maximum of 8 A and the power turn-on is sequenced. Power usage during FPGA configuration is not as high as when the JEM is working. The total power consumption of a JEM is less than 60 W.

2.2 JET CHAIN PERFORMANCE

Attila Hidvégi described the jet logic chain. He mentioned high-statistics tests of the jet algorithm, and also said that in extensive system tests done at various times no errors had been found in the jet processing.

Attila said there are at least two points in the chain where it would be relatively easy to make significant reductions in the latency. This had not been seen as important until recently because the Cluster Processor latency was longer, but the CP latency has now been reduced so it would be good to get the jet latency well inside its envelope. A reduction of up to 1.5 or 1.75 ticks will soon be tested.

The mapping of FCAL channels into the jet algorithm is very complex and needs to be brought up to date.

2.3 PRODUCTION AND QUALITY ASSURANCE ISSUES

Uli Schäfer then talked about production plans, quality assurance, and low-level acceptance tests of production modules.

The module files will now be sent to the manufacturer (Rohde and Schwarz) in ODB++ format, which is claimed to be more reliable. The JEMs will be made under a 'one-stop shop' arrangement in which the manufacturer procures components, makes the PCBs, and assembles the modules. If a module fails the acceptance tests, it will be returned to the manufacturer and repaired at the manufacturer's expense. Components can be re-worked by the manufacturer but with a limit of one re-work per component.

Four pre-production modules will be built and the full-crate test (see sect. 2.1) carried out. When that is successful, full production will be ordered. The full number of modules might be at CERN as early as May 2006, though this was a topic for discussion (see sect. 2.5).

Uli distributed a cost estimate for producing the JEMs. He also discussed the total number of modules to build. The trigger system will use 32 JEMs, and our spares policy demands at least 10% spares. In addition, a few JEMs are needed for test rigs. However, Uli proposed having more than 10% spares in order to avoid the need to re-work modules later on in case of problems — experience so far with re-working JEMs has not been very good. The number proposed is 45 JEMs. Enough Input Modules would be built to fully populate the spares, so Uli proposed making 180. Similar considerations would apply to the other daughter cards.

The quality assurance checks to be done by the manufacturer were described, followed by JTAG checks after delivery of modules to Mainz. The motherboard and Input Module have been designed to include a very large coverage of JTAG-testable nets.

Uli listed in detail the steps from the time a JEM arrives until it is deemed ready for crate tests. Daughter cards were included in this description. Finally, a list of equipment needed for all the tests was presented.

2.4 CONNECTIVITY TESTS, SYSTEM TESTS, AND SOFTWARE

Rainer Stamen discussed higher-level testing of the JEMs and the software needed to do it. Connectivity tests would check the LVDS inputs, routing through to the Jet and Sum FPGAs, fan-in/fan-out of data to and from neighbouring modules, and G-link outputs to RODs. These tests would be checks, not exhaustive tests, so they would not be unusually stressful or run long enough to get very high statistics.

The LVDS connectivity tests would use LVDS Source Modules (LSMs) for input test data. FIO tests would use JEM internal playback memories for their test data. Readout G-link tests would use ramp data from the JEM FPGAs and send it to Data Source/Sink test modules.

After all the connectivity tests are passed, JEMs would then undergo system tests. These might be at RAL, Birmingham or CERN, see the discussion in sect. 2.5. The first phase of these tests would be the full-crate test that will be done with the four pre-production JEMs, together with six older prototypes, CMMs and CPMs. Similar tests would later be done with the final production modules.

As he went through these various tests, Rainer mentioned the current status of the necessary software and test vectors. In general, a lot of the basic software exists but easy-to-use standalone test programs must be produced and test vectors still need some work.

A final issue here is storage of the results. How elaborate a scheme we need depends on how much information we want to store, and this needs to be discussed and decided. Options include Excel if there is

not too much data, or the Heidelberg database if there is a lot — the database would need improvements to do this.

2.5 SUMMARY OF COMMENTS RECEIVED AND OPEN DISCUSSION

The panel were very appreciative of the way the talks gave direct responses to the comments and recommendations of the FDR, and the specification document had been edited to incorporate almost all of suggested corrections. Detailed corrections and improvements suggested for the JEM specification document are listed in Appendix A. The description of the jet algorithm could be clearer without adding much extra material. The document on production and tests was felt to be somewhat lacking in detail, but more was said in the talks.

A slot keying system using plastic inserts to prevent plugging trigger modules (of all types) into the wrong slots in the crates is planned for the trigger system, including the JEM. Sam Silverstein had said he would devise the details of this, and offered to do it by the end of December 2005.

The cabling from PPM to JEM uses inconsistent nomenclature in the two modules. A table for converting one to the other needs to be prepared.

There was some concern that sufficient acceptance tests will not be done on the Control and Readout daughter cards before testing them on a JEM, so there is some risk of damage to the JEM. At the very minimum they should be powered up first.

There was a discussion of where to do the system tests. On the timescale presented it is not likely that there will yet be a fully functional test rig at CERN. Birmingham is one possibility but at present does not have a ROD or the expertise to run one, though it would be useful to learn how to do that. The situation at RAL is time dependent, as people will be moving to CERN early in 2006. This will have to be discussed further, probably when more is definitely known about when JEMs will be available for the full crate test.

JEM firmware will ultimately be stored in a CVS archive.

The desirability of testing with high temperatures, low supply voltages, and different clock frequencies was discussed; it had also been raised at the FDR. The temperature issue partly concerns TTCrx timing drift, but the JEM is not as sensitive to small timing shifts as, for example, the CPM. Varying the supply voltages is not straightforward because of the large number of on-board voltage regulators. (The Input Module had ‘accidentally’ been tested with low supply voltage without problems.) As for frequency, the LVDS receivers used on the JEM are working in the middle of their frequency range, unlike the ones on the PPM and the CPM.

There was a general feeling among the reviewers that the proposed timetable for production testing was too aggressive, particularly the system tests. For administrative reasons it was important to place the production order immediately after the PRR, but on the timetable presented (assuming no delays) the JEMs would actually arrive at CERN before the other trigger subsystems. Therefore, it was suggested that the system tests should be done in a more thorough and less rushed way.

The spares level proposed is very generous, but there was no way to compare the cost of that with the cost of re-working faulty modules. Re-work costs should be estimated. In addition, some spare FPGAs should be purchased.

3 CONCLUSIONS AND RECOMMENDATIONS

The reviewers concluded that the JEM can now be approved for production. The design changes already implemented and the few remaining ones proposed are accepted. Tests, including the ones requested at the FDR, have been carried out with satisfactory results. The noise and crosstalk problems observed after the FDR appear to have been fixed by the design changes in JEM 1.2. The proposals for pre-production, full-crate test and full production, quality assurance and acceptance tests should be followed, subject to the recommendations below.

- The overall grounding scheme for the PPM, CPM and JEM must be checked by Georges Blanchot
- The slot keying system should be worked out and presented soon
- The jet algorithm must be tested with completed CMM jet firmware as soon as possible
- The jet logic latency should be reduced as described, and the algorithm re-tested thoroughly
- The FCAL jet-channel mapping must be brought up to date
- The cost of re-working faulty modules needing repair should be ascertained
- Some spare FPGAs should be purchased
- Daughter cards should first be tested on their own for faults, at minimum to a point where it is unlikely they would damage a JEM when plugged in
- System tests of pre-production and production JEMs should place more emphasis on thoroughness and be less concerned with rapid execution
- The location for doing the system tests needs to be decided
- A suitable way to store production test results must be agreed
- The JEM specification document should be corrected, especially the jet algorithm description
- A table for converting cabling nomenclature between PPMs and JEMs should be prepared

APPENDIX A: DETAILED EDITORIAL COMMENTS ON JEM SPECIFICATION, V.1.1d

Sect. 1.2

Footnote 2 could be expanded to be a bit more explicit, for example: ‘Allows for partial cancellation of missing-energy sums at crate level since the components have opposite signs, and so fewer bits are needed.’

Sect. 1.2.1

Somewhere there should be a comment that the jet algorithm for FCAL is still an open question with several options.

Fig. 3 includes "JMM" and "SMM", not explained anywhere. Easiest is to change the labels to Jet CMM and Sum CMM. Also, label which is front and rear of module.

Sect. 2.3

The text or a footnote could indicate that the number of sine and cosine coefficients needed on geometrical grounds is 8 in phi and 8 in eta, plus 4 for FCAL (just to give an idea of how much data is needed), and say they come from the database.

Sect. 2.5

Jet algorithm (with its different window sizes) would be much clearer if there were a diagram. Selection of window size should be described more clearly. (See algorithm document for a diagram)

Explain that thresholds are > not >=, so if threshold is set to full scale (10 bits) it is turned off.

There should also be a diagram of how the local minimum is found when two adjacent sums are equal, i.e. > for half the neighbours and >= for the other half. Also which way that works in eta and phi.

Add something like: "Details of the FCAL jet algorithms and data may be subject to change as a result of future studies."

Sect. 2.6
Para 1 line 1 - a bit confusing, might not be clear what data is on long backplane links. How about "All real-time data crossing board boundaries that comes in on cables (input data from the PreProcessor) or leaving on long backplane links (jet hit and energy-sum results to the Common Merger Modules) are captured ..."

Sect. 3
Add a drawing of the board overall layout, including daughter cards

Sect. 3.1
Title should be "Input data reception", it's NOT just JET data

Sect. 3.2
Title should be "Input data conditioning", it's NOT just JET data

Sect. 3.3
Para 1 line 8 - For FCAL it is FOUR threshold sets, not 8

Para 2 line 2 - For FCAL it is FOUR threshold sets, not 8

Para 3 - Here again, it should be pointed out explicitly that thresholds are 10 bits and if they are set to full scale they don't produce hits or RoIs.

Sect.3.4
Para 1 line 1 - "from each OF"

Footnote 17 - "shown" not "show"

Sect. 4.1
Add a drawing of the front-panel layout

Glossary
Add "R-ROD" and "D-ROD" (or be more explicit in fig. 3)

APPENDIX B: COMMENT ON PROGRAMMING MODEL, V.1.1

Sect. 1.1
Mention of VME block transfers and broadcast operation. These are not supported by VME--, so remove.