ATLAS Level-1 Calorimeter Trigger

Jet / Energy Processor Module

Programming Model

Version 1.2 (post PRR)

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In the following a programming model for VME access to registers and memories of the JEM and its components is described. The description relates to the current FPGA firmware. The register model is likely to change for future firmware revisions. Each JEP crate will have a local CPU directly accessing the VME part of the crate backplane and thus an entirely self-contained VME address space. A suitable documentation of the programming model will be provided to accompany the final modules.

Guidelines

- The standard access is VME A24/D16.
- There are no write-only registers except for pulse and configuration registers. All registers can be read by the crate CPU via VME.
- The register bits generally have the same meaning for reads as for writes.
    - All Status Registers are read-only register
    - All Control Registers are read/write or pulse registers
    - Reading back a register will generally return the last value written
- Attempts to write to read-only registers or undefined portions of registers will not change the contents of the non-modifiable fields.
- Fully synchronous design protects all VME registers from being read via crate CPU while being altered by the JEM itself at the same time.
- When the address space occupied by the JEM is accessed, it will always respond with a handshake (DTACK*) to avoid a bus error.
- The power-up condition of all registers and BlockRAMs will be all zeros, unless otherwise stated.

Notation

- RO means that the computer can only read the value of this register; writing has no effect either to the value or the state of the module.
- RW means that the computer can affect the state of the module by writing to this register.
- PR means the register is a pulse register. Writing a '1' triggers an action.

1 Memory Map

In the following an overview of the address scheme for a JEP crate and its subsystems is given. Detailed register descriptions are given below. The jet processor programming model is so far available as a separate document only.

Address Line	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Use	**1**	JEM Base address				mode		FPGA sub address				Register address space for each FPGA											

1.1 Mode

VME Address (binary)	**Device**
00	VME registers
10	configuration

Address bit 18 selects FPGA configuration download. The configuration space is defined as a write only block memory that returns 0xFFFF when read. The FPGAs selected for configuration are defined by bits 16 and 15 according to 1.2 .

1.2 Sub Base Address

VME Address (Hex)	**Device**
0	VME CPLD
2	SystemACE
4	Sum FPGA
8	JET FPGA
C	Input FPGA R

D	Input FPGA S
E	Input FPGA T
F	Input FPGA U

2 VME CPLD register map

VME Address (Hex)	Type	Name	Description
00	RO	MOD_ID_A	Module ID A: module type
02	RO	MOD_ID_B	Serial number & Module Revision number
04	RO	VERSION_REG	Firmware version number
06	RO	STATUS_REG	Status register
10	RW	CFG_MASK_REG	Mask FPGAs for configuration
12	PR	FPGA_RESET_REG	Reset FPGA

2.1 MOD_ID_B

A register containing module identifiers.

Bit	Description
0 - 7	Serial number
8-15	Revision number

2.2 STATUS_REG

A register containing module status information.

Bit	Description
0	TTC clock available
1	Sum Processor Configuration done

2.3 CFG_MASK_REG

A register for enabling FPGA to be configured via VME.

Bit	Description
0	Configure Sum-FPGA

2.4 FPGA_RESET_REG

A register for resetting FPGA.

Bit	Description
0	Reset Sum-FPGA

3 SystemACE register map

The SystemAce chip is mapped into the VME address space. For SystemACE registers see http://direct.xilinx.com/bvdocs/publications/ds080.pdf, p. 18. 16-bit wide access possible only. The registers are correctly mapped to even VME addresses.

4 Sum processor register map

VME Address (HEX)	Type	Name	Description
00	RO	VERSION_REG	Firmware version number
02	RO	STATUS_REG	Status Register
04	RW	CONTROL_REG	Control Register
06	PR	PULSE_REG	Pulse Register
10	RW	CFG_MASK_REG	Configuration mask
12	PR	FPGA_RESET_REG	FPGA reset
14	RO	DONE_REG	FPGA configuration status
40	RW	TTC_CONTROL_REG	I2C control register of TTCrx chip
42	RO	TTC_STATUS_REG	I2C status register of TTCrx chip
60	RW	READ_REQUEST_DELAY_REG	Delay read request signal
62	RW	ROC_SLICE_REG	Slice count register
64	RW	BC_PRESET_REG	Bunch counter correction
A0	RO	SPY_MEM_EXY_PORT	Port to 256 deep spy memory [1]
A2	PR	RESET_SPY_MEM_EXY_COUNTER	Reset pointer to Exy spy memory
A4	RO	SPY_MEM_ET_PORT	Port to 256 deep spy memory
A6	PR	RESET_SPY_MEM_ET_COUNTER	Reset pointer to Et spy memory

4.1 STATUS_REG

A register containing module status information.

Bit	Description
0	Lock status of DLL

4.2 CONTROL_REG

A register containing modul controls.

Bit	Description
0-3	reserved
4	Enable spy mode

4.3 PULSE_REG

A register containing pulsed module controls. Writing zero has no effect.

Bit	Description
0	Module reset
1	Simulate short broadcast (reset playback/spy pointers)
10	Simulate Level1Accept

4.4 CFG_MASK_REG

Enable configuration download of processors via VME.

Bit	Description
0	Enable jet processor configuration
4	Enable configuration of input module R
5	Enable configuration of input module S
6	Enable configuration of input module T
7	Enable configuration of input module U

[1] Consecutive read accesses are used to read spy memory.

4.5 FPGA_RESET_REG

Clear configuration of processors.

Bit	Description
0	Reset jet processor configuration
4	Reset configuration of input module R
5	Reset configuration of input module S
6	Reset configuration of input module T
7	Reset configuration of input module U

4.6 DONE_REG

Indicate configuration status (DONE line) of processors.

Bit	Description
0	jet processor configuration done
4	configuration of input module R done
5	configuration of input module S done
6	configuration of input module T done
7	configuration of input module U done

4.7 TTC_STATUS_REG

Read out TTCrx status and data via I2C. Data are valid only if neither busy nor error bit are asserted.

Bit	Description
0-7	Data read from I2C
13	I2C busy
14	I2C error

4.8 TTC_CONTROL_REG

Control TTCrx chip via I2C. Access to this register is allowed only if I2C controller not busy. See 4.7. To read/write TTCrx registers specify sub-address and data to be written. For TTCrx address map see TTCrx reference manual.

Bit	Description
0-7	Data to be written to I2C
8-12	I2C sub-address
13	Write control ‘1’= write to I2C device
15	Reset I2C controller

4.9 READ_REQUEST_DELAY_REG

A register containing the latency correction for the READ_REQUEST signal . The READ_REQUEST signal initiates DAQ readout on all Input-FPGAs and on the Sum Processor.

Bit	Description
0-5	Latency correction, up to 63 ticks

4.10 ROC_SLICE_REG

The slice count register contains the number of consecutive slices which will be read out after a L1A signal. The maximum number is five.

Bit	Description
0-2	Slice count, up to 5 ticks

4.11 BC_PRESET_REG

A register containing the timing correction for the local bunch crossing counter. This value is used to pre-set the bunch counter upon reception of a BC_RESET signal from the TTCrx.

Bit	Description
0-11	Bunch counter preset

4.12 SPY_MEM_EXY_PORT

A register serving as a port to the 256 deep spy memory. After each register read operation the pointer to the spy memory location is incremented. Pointer reset via 4.13.

0-7	Ex data. Copy of the data sent to the energy sum merger, quad linear encoded.
8-15	Ey data. Copy of the data sent to the energy sum merger, quad linear encoded.

4.13 RESET_SPY_MEM_EXY_COUNTER

Reset for spy memory pointer (pulse register)

Bit	Description
0	Set spy memory pointer to 0 location

4.14 SPY_MEM_ET_PORT

A register serving as a port to the 256 deep spy memory. After each register read operation the pointer to the spy memory location is incremented. Pointer reset via 4.15.

0-7	Et data. Copy of the data sent to the energy sum merger, quad linear encoded.
8	Odd parity bit as sent to merger along with the data

4.15 RESET_SPY_MEM_EXY_COUNTER

Reset for spy memory pointer (pulse register)

Bit	Description
0	Set spy memory pointer to 0 location

5 Input FPGA register map

Registers relating to the FPGA as a whole are starting at subaddress 0. Input channel related registers are located from Address 0x1000.

VME Address (Hex)	Type	Name	Description
0000	RO	VERSION_REG	Firmware version number
0002	RO	STATUS_REG	Status register (currently not in use)
0004	RW	CONTROL_REG	Control register
0006	W	PULSE_REG	Pulse register
0008	RW	THRESHOLD_LOW	Jet element low threshold register (Ex,Ey)
000A	RW	THRESHOLD_HIGH	Jet element high threshold register(Et)
0010	RW	PLAYSPY_REG	R/W port for playback and spy, auto increment
0011	PR	RESET_PLAYSPY_COUNTER	Reset pointer to playback/spy memory location
1000			Sub-address space for input channels. 24 individual channels spaced 0x40.

5.1 PULSE_REG

A register containing pulsed module controls. Writing zero has no effect.

Bit	Description
0	Reset link error counters
1	Reset Parity Error counters
2	Reset Test Pattern Error Counters
4	Reset counter for Playback/Spy Memory access

5.2 CONTROL_REG

A register containing module controls.

Bit	Description
0	Enable playback mode
1	Enable spy mode

5.3 THRESHOLD_LOW , THRESHOLD_HIGH

A set of 2 control registers (10 bit wide) setting a low threshold, applied to jet elements before calculation of missing energy, and a high threshold applied to jet elements to be summed up in the total transverse energy summation tree.

5.4 PLAYSPY_REG

A port to the playback/spy memory array of 24 words × 256 deep. Pointer to the playback/spy memory location is incremented after each write or read operation. Looping over data words first, then depth. Pointer reset via 5.5. Raw data words are transmitted, the meaning of which is different in playback or spy mode.

Bit	Description
0-9	Playback / spy raw data word

5.5 RESET_PLAYSPY_COUNTER

A register to reset the pointer to the playback/spy memory.

Bit	Description
0	Reset pointer to playback/spy memory

5.6 Channel Space

For each input channel (electromagnetic or hadronic) a set of registers is mapped. Please note that some registers may carry jet element control functions. Those registers are found in every other channel space only (even or odd).

VME Address (Hex)	Type	Name	Description
0	RO	Ch_Status	Status Register
2	RW	Ch_control	Control Register
4	RO	Ch_Link_err	Link error counter, 12 bit saturating counter
6	RO	Ch_Par_err	Parity error counter, 12 bit saturating counter
8	RO	Ch_Test_Pat_err	Test pattern detection error counter, 12 bit
A	RW	Ch_mult	Ex/Ey coefficient on even/odd channel

5.6.1 Ch_status

Bit	Description
0	Link error bit (current status)

5.6.2 Ch_control

Bit	Description
0	Phase control bit (+1/2 tick)
2:1	Delay control bit field (+ n ticks)
3	Mask bit : '1' = off

5.6.3 Ch_Link_err

12-bit saturating counter. Counts the transitions of the link status line. Large values indicate instable rather than broken link. The link error bit in the status register needs to be read out to determine current link status.

5.6.4 Ch_Par_err

12-bit saturating counters. Counts parity errors.

5.6.5 Ch_Test_Pat_err

12-bit saturating counters. Counts pattern errors. Used for firmware based analysis of linear ramp patterns generated by the upstream module.

5.6.6 Ch_mult

12-bit coefficient for calculation of E_X, E_Y from the jet element which is built from one electromagnetic and one corresponding hadronic channel. CH_mult of electromagnetic channels (even channel numbers) is the X-coefficient, CH_mult of hadronic channels (odd) is the Y-coefficient.

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Change log:
2005-12-09 Change wording of SystemACE register description to reflect hardware modifications on JEM1.3 agreed with L1Calo community on Dec. 08 (16-bit access to ACE only).
2005-12-05 Extract from FDRed JEM specifications and implement corrections in response to FDR comments. Add some register descriptions. Add SystemACE