LVDS Source Module. (LSM)

Design Specification v 2.1

Contents:

Design Requirements

LVDS source module will provide 480Mb/s LVDS serial data signals for testing CPM and JEM processor modules.

Similar in function to the DSS/LVDS combination, but driving many more LVDS links. To do this, the LSM will use FPGAs for the data source and serialisation. The serial format will match that of the existing LVDS links.

The LSM will use the new TTCdec daughter-card to provide the master clocks for the module. TTC commands will be decoded, to synchronise the playback with other modules, as done on the CPM.The TTC input will be electrical via front panel.

There will be provision for a high quality PLL to be inserted after the TTCdec, should the jitter of the TTC clock prove troublesome.

ALTERA Cyclone FPGAs will host the serialisation and memory functions.

DC/DC converters will provide the onboard supplies

JTAG connections will be used for testing the PCB assembly.

Module size

6U VME.

CPU interface

A24 / A32 , D16 VME Slave. Base address set by rotary hex switches.

Pattern Generator Memory.

Depth is restricted by the desire to place the memory and serialisation within an FPGA. 1k deep 10 bit words can be provided for each of the 16 links within an ALTERA EP1C12 FPGA. Six such FPGAs will give the 96 links / LSM.

The memories are not dual-port, so any access to the memory from VME will have priority and override the contents currently being output to the links.

During playback the memories may wrap-around at other than the full depth. The value is set by a 16 bit (12bit?) register which covers the Orbit value of 3564 (0xDEC). Should the playback cycle exceed the memory depth , the remaining data will be taken from memory location0 until the playback counter returns to 0.
Thus memory location0 is unique as it supplies the link 'idle' value.

The Pattern memory will power-up with defined values. The initial design will place 0x001 (the link idle value) in all locations.

LVDS serial links + Cable Pre-compensation

The Pre-processors use National LVDS serialisers into Virtex2 FPGAs to drive the cable. These outputs are voltage drivers using series RC compensation circuit. (Note that the existing DSS/LVDS uses LR pre-compensation across line).The LSM output will be similar to that of the Pre-Processor.

Cable connectors.

These will be compatible with our 2mm grid cable assemblies.

Pin layout will match that of the signals on the processor backplane, similar to the DSS/LVDS front-panel connector.

Configuration memory

ALTERA EEPROM type EPCS4 programmed using Byteblaster download cable (Not JTAG protocol) from PC.

TTCRx Address:

0000 ssss 001000 where ssss are the lower 4 bits of the module serial number.

TTC Broadcast Commands:

Background:

00 mmmm xx.	Reserved for PPm/CMM/CPM/JPM , ignored by DSS
01 mmmm xx.	Global Start (+ reset pointer)
10 mmmm xx.	Global Stop (only used by DSS ?)
11 mmmm xx.	Reserved

Where mmmm = to be defined. Present use :

0010	PPM Stop LVDS Sync Pattern
0011	PPM Start LVDS Sync Pattern
1xxx	unused

The LSM will decode the following Broadcast Commands:

01 0000 xx.	Start Playback (+ reset pointer)
10 0000 xx.	Stop Playback (Used by DSS ?)

PCB Test Points

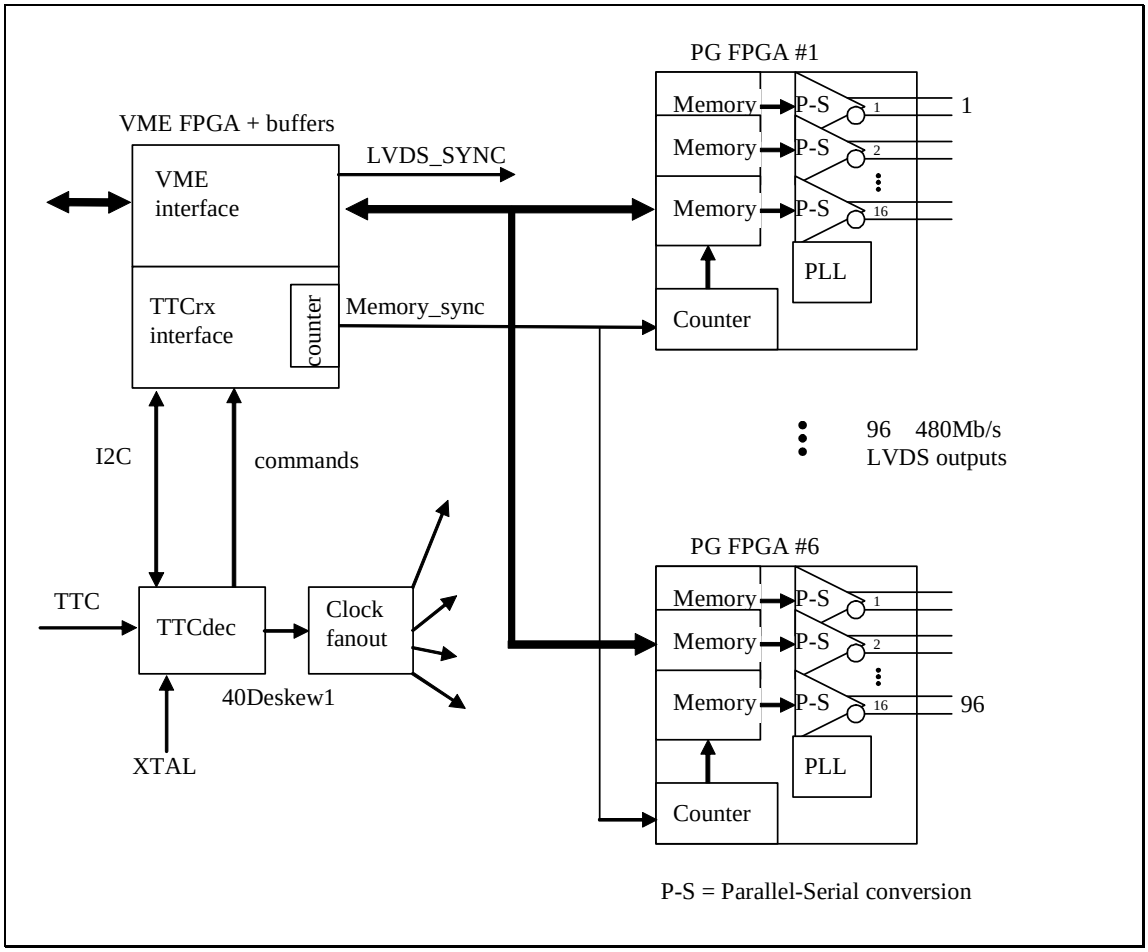
JTAG connector for access to all FPGAs.
All clocks
L1A
VME strobes , DTACK & 'Module access'
TTCrx strobes
Pattern Generator & Memory control + strobes
FPGA configuration signals
Spare connections to FPGAs

Other Inputs & Outputs

Electrical TTC input:, Differential ,100 Ω terminated then AC coupled to receiver.
Typicaly PECL 800mV inputs , sensitivity is 150mV..

Monitor out: 40MHz TTC clock or Custom Trigger, link selectable.
3V CMOS source terminated signal. Lemo? connector

Block Diagram



Front Panel indicators

Power

FPGA status
- Configured
- PLL locked

VME access

TTC Status

TTC Short broadcast bits

FP connectors

2 x type B (25 row)

Electrical TTC input.(From TTC-fanout module)

Clock output

Design Entry

The FPGA designs will be created and synthesised using the ALTERA Quartus tools. The top-level will be a Quartus schematic with lower-level blocks written in VHDL where possible.

PCB Schematics and Layout will drawn using Cadence tools.

Implementation

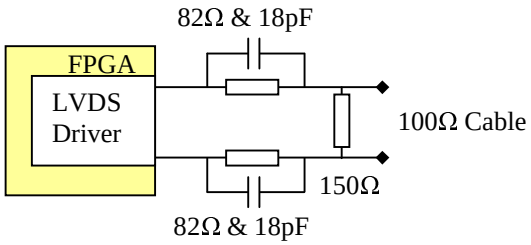
The VME registers and TTC interface will be combined into one Cyclone FPGA. The VME FPGA will be a Cyclone EP1C12F256C8 or EP1C12F324C8 , configured from it's own EPCS4 eeprom.

16 LVDS serialisers with memory will be another FPGA , called the Pattern Generator (PG FPGA). Cyclone EP1C12F256C8 or EP1C12F324C8 will also be used for this design. The 6 PG FPGAs will be configured together from a serial eeprom type EPCS4. The eeproms are programmed from PC with ByteBlaster cable.

The Cyclone FPGAs are chosen for LVDS serialisation as they have PLLs for internal clock distribution rather than DLLs as found in the Xilinx parts. PLLs are more tolerant of clock jitter. The Cyclone LVDS outputs are also voltage drivers, so will generate signals more like the Pre-processor combination,

DC/DC converters will provide the onboard supplies for 1.5V, 2.5V and 3.3V.

Cable Pre-Compensation Circuit



(The above values are copied from a Heidelberg circuit. These may need to be adjusted for ALTERA devices)

VME Address map

The module occupies 256KBytes of VME address space.
The base address is set by switches to match the upper 6 lines of the address bus.

Type	Function name	Size (16 bit Words)	VME Address Offset from Base (Hex)
RO	Module ID	1	000000
RO	Serial Number + Revision	1	000002
RO	Firmware revision	1	000004
RO	FPGA Status	1	000006
RO	Module Status	1	000008
RW	Module Control	1	00000A
RW	Pulse Register	1	00000C
RW	PG Control	1	000020
RO	PG Status	1	000022
RW	PG Playback Length	1	000024
WO	TTCRX Pulse	1	000030
RO	TTCRX Status	1	000032
RO	BCNT Counter	1	000034
RO	EVNT Counter	1	000036
RO	TTC FIFO Status	1	00003C
RW	TTC FIFO Data	1	00003E
RW	TTCrx I2C controller	2	000040
RW	Pattern Gen. 1 Memory	16K	008000
RW	Pattern Gen. 2 Memory	16K	010000
RW	Pattern Gen. 3 Memory	16K	018000
RW	Pattern Gen. 4 Memory	16K	020000
RW	Pattern Gen. 5 Memory	16K	028000
RW	Pattern Gen. 6 Memory	16K	030000
RW	Unused	16K	038000-03FFFE

Register Description:

Any location or bit not mentioned below will read as '0'.
Unless specified, writeable registers will power-up as '0'.

Module ID Register

A 16-bit register conforming to the LVL1 Calorimeter trigger module ID convention:

Bits <15:0> Module Type. = 2423 h.

The number is set within VME FPGA Firmware.

Serial Number + revision

A 16-bit register conforming to the LVL1 Calorimeter trigger module ID convention:

Bits <15:12> Unused - read as Zero.
Bits <11:8> Module Revision No
Bits <7:0> Serial Number in the range 0-255.

The serial number is set by links on the PCB, Module Revision is permanently etched.

Firmware Revision

Bits <15:0> Revision number of VME firmware.

FPGA Configuration Status Register

A 16-bit read-only register.
Bits <12:7> *unused
Bits <6:1> indicate PG FPGA unconfigured. Inverted DONE signal. Should read 0.
* due to a design error in the PCB, the PLL LOCK status is moved to the PG memory area, see below

Module Status

A 16-bit read-only register.

Bit <2> Memory cycling
Bit <1> TTCdec S2
Bit <0> TTCdec S1 = TTCrx Ready

Module Control

A 16-bit read-write register containing static (non-pulsed) module controls.

Bit <3> Reserved for TTCdecPD signal control. Pulled high on PCB.
Bit <2> TTCdec_XTAL. 1= select XTAL. Inverted TTCdecTX signal.
Bit <1> Reserved for VME Lockout – Disables VME access to memories.
Bit <0> LVDS Sync – Send LVDS synch frames over link . Set on Power-up or Reset.

Pulse Register

A 16-bit read-write register containing pulsed actions. Writing a '0' to individual bits has no effect. Readback as '0'.

Bit <7> Reset TTCRx.
Bit <6> TTCRx JTAG reset
Bits<5..2> Unused
Bit <1> PG PLL reset
Bit <0> PG_Reset

PG Control

A 8-bit read-write register for VME and TTC control of PG memory.
Memory Playback bit is synchronised to the TTC clock. Power-on and Reset to 0.

Bit <2> Memory Playback. 1 = Cyclic Playback, begining from location 0.
Bit <0> Select either TTC Commands(=1) or VME(=0) to control playback.

PG Status

Bit <2> 1 = Memory Playback/Cycling. 0 = Frozen.

PG Playback Length

A 16-bit read-write register holding the maximum pointer value = cycle length-1. If this value exceeds the memory depth, each Pattern Generator will source the remaining data from location(0).
On power-up this value is set to the full memory size ie 1023.

TTCRX Pulse

Bit <0> Clear SER DER flags

TTCRX Status

Bit <6> TTCrx SER flag
Bit <5> TTCrx DER flag
Bit <4..1> Reserved
Bit <0> TTCrx Ready = TTCdecS1

EVNT Counter

Bits <15:0> A 16 bit counter incrementing on L1As , cleared by EVCNTRST.

BCNT Counter

Bits <11:0> A 12 bit counter incrementing every BC (ie 25ns), cleared by BCNTRST.

TTC FIFO Status

Bit <2> Dump FIFO full
Bit <1> Dump FIFO empty

TTC FIFO Data

Bits <11:8> TTCrx DQ Data from a 'TTCrx Dump' command.
Bits <7:0> TTCrx DOUT Data from a 'TTCrx Dump' command

TTCrx I2C Controller

Provides access to the 20 user-accessible internal registers of the TTCrx chip via the I2C interface.
Refer to the TTCrx Reference Manual version 3 page 13 for programming details.
This controller will be a copy of that used on the CPM.

(+0) R/W, Control

Bit <15> Reset Controller
Bit <13> Write / Read operation, 1 = Write.
Bits <12:8> TTCrx Register index
Bits <7:0> Data for TTCrx Register

(+1) RO, Status

Bit <14> I2C Error
Bit <13> I2C Busy
Bits <7:0> Data from TTCrx Register

Pattern Generators

Each Pattern Generator contains separate memories for each of 16 LVDS links. Memories are 1k deep, aligned to even addresses. Bits<9:0> 10bit wide memory , Bits<15:10> unused (except for the first location).

(+0000 to 07FE) Link A
(+0800 to 0FFE) Link B
(+1000 to 17FE) Link C
…
(+7800 to 7FFE) Link P

When connected to a CPM, via the 2mm cables, the serialiser mapping will show the following layout:

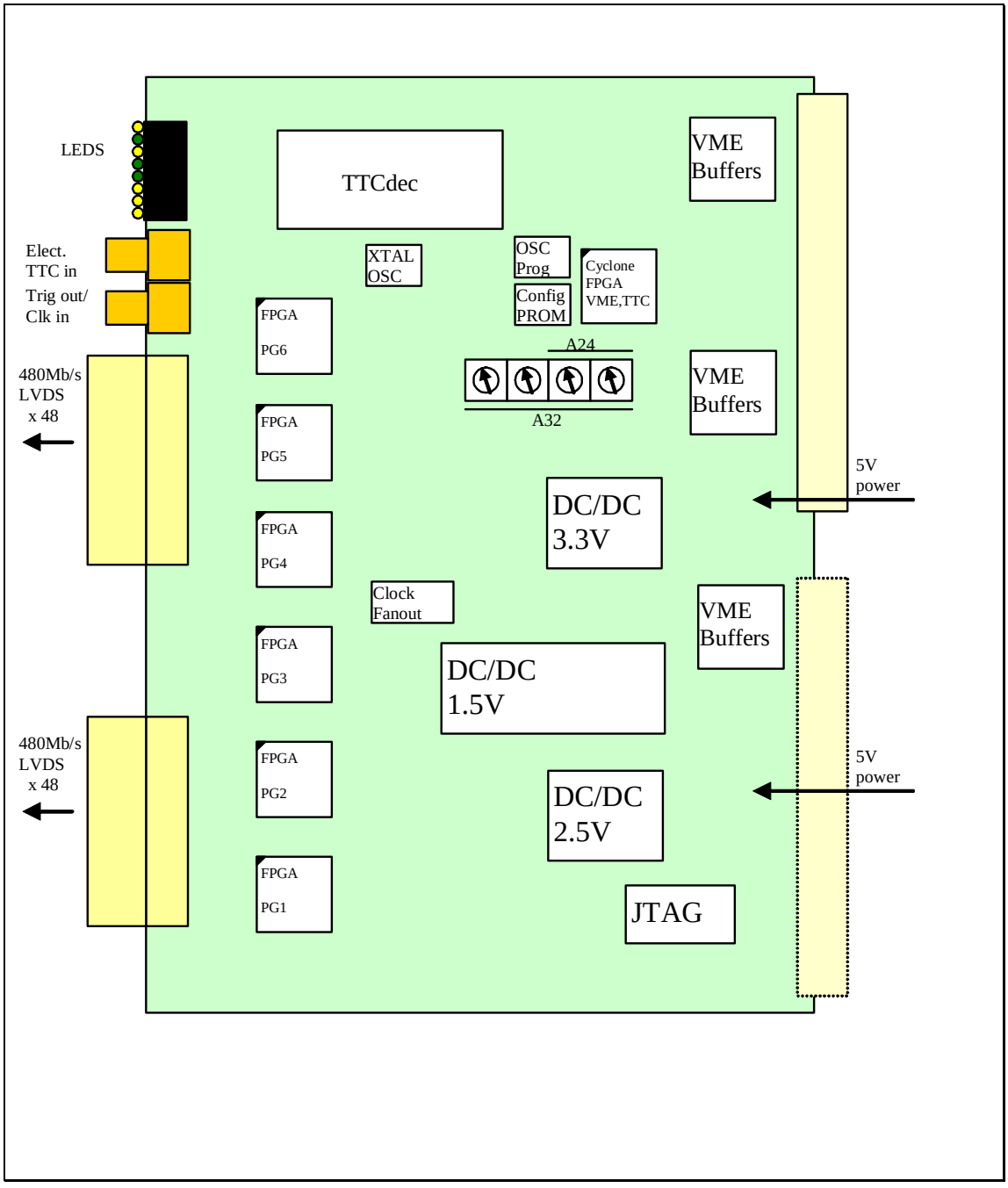
PG Memory	CP input	Serialiser name
A	**QL**	**XL**
B	**QM**	**XM**
C	**RL**	**YL**
D	**RM**	**YM**
E	QL	XL
…	…	…
P	RM	YM

During playback the data pattern may cycle with a period other than the full memory depth of 1024. The wrap-around point is set by a 16 bit register to include the Orbit value of 3564. When the playback length exceeds the memory depth , the remaining data will be played out from memory location0 until the playback counter cycles back to 0. Thus memory location0 is unique as it supplies the link 'idle' value.

The Pattern memory will power-up with the link idle value 0x001 in all locations.

The first location of each PG also shows the status of the internal PLL.
Bit<15> 1 indicates PLL fault.

LSM Layout:


LEDS
TTCdec
VME Buffers
Elect. TTC in
Trig out/ Clk in
XTAL OSC
OSC Prog
Config PROM
Cyclone FPGA VME,TTC
FPGA PG6
A24
A32
480Mb/s LVDS x 48
FPGA PG5
VME Buffers
5V power
FPGA PG4
DC/DC 3.3V
Clock Fanout
VME Buffers
FPGA PG3
DC/DC 1.5V
480Mb/s LVDS x 48
FPGA PG2
5V power
DC/DC 2.5V
FPGA PG1
JTAG

LSM Front panel LVDS Connector Pin-out

Upper connector

Cable Connector (5x25 grid)	Column a	Column b	Column c	Column d	Column e	
Row 1	O+	O-	GND	P+	P-	
Row 2	M+	M-	GND	N+	N-	
Row 3	K+	K-	GND	L+	L-	
Row 4	I+	I-	GND	J+	J-	PG6
Row 5	G+	G-	GND	H+	H-	
Row 6	E+	E-	GND	F+	F-	
Row 7	C+	C-	GND	D+	D-	
Row 8	A+	A-	GND	B+	B-	
Row 9	O+	O-	GND	P+	P-	
Row 10	M+	M-	GND	N+	N-	
Row 11	K+	K-	GND	L+	L-	
Row 12	I+	I-	GND	J+	J-	PG5
Row 13	G+	G-	GND	H+	H-	
Row 14	E+	E-	GND	F+	F-	
Row 15	C+	C-	GND	D+	D-	
Row 16	A+	A-	GND	B+	B-	
Row 17	O+	O-	GND	P+	P-	
Row 18	M+	M-	GND	N+	N-	
Row 19	K+	K-	GND	L+	L-	
Row 20	I+	I-	GND	J+	J-	PG4
Row 21	G+	G-	GND	H+	H-	
Row 22	E+	E-	GND	F+	F-	
Row 23	C+	C-	GND	D+	D-	
Row 24	A+	A-	GND	B+	B-	
Row 25			GND			

The LSM pinout maps onto the CPM module input signals via cable, as seen at LSM:

RL+	RL-	GND	RM+	RM-
QL+	QL-	GND	QM+	QM-

Note: Be aware of cable rotation.

Lower connector

Similarly for PG3 - PG1

Front panel LEDs

Green x 4 - Power +5.0,+3.3,+2.5,+1.5
Yellow - VME access
Yellow – Running
Green x 2 - FPGAs Configured
Yellow x 2 – TTC Ready + TTC Command

LED bar display – TTC Short Broadcast

Power supplies

DC/DC converters used to provide the onboard supplies:

1.5V FPGA core - PT6445A (6A) Switcher *1
2.5V LVDS I/O - PT5402A (6A) Switcher *2
3.3V CMOS/TTL -. PT5401A (6A) Switcher.

*1. This must provide the 900mA Power-up surge current for each of the 7 Cyclone devices, a total of 6.3A. The PT6445A has a short circuit threshold of 10A.. Once configured and running, the total current demand will fall below 1A.
The footprint will accept a PT6465A regulator rated to 14A if needed.
The regulator running at 85% efficiency, will be take 2.2A from the 5V supply to provide 1.5V @ 6.3A during the power-up phase.

The PT6465 will be fitted as the original is now obsolete.

*2. Each PG is estimated to draw 0.4A from the 2.5V rail, totalling 2.4A. The regulator running at 90% efficiency will take 1.3A from the 5V supply.

Power dissipation of a running PG is estimated to be 1.1W

Estimated Component Cost:

6 FPGAs type EP1C12F324C7 @ $ 82 = $ 492
VME & TTC interface FPGA $ 82
Configuration memory $13
PLL clock distribution $5
DC/DC converters $25

Updated quote for Components and Assembly , excluding PCB is £1152
(as of September 2004)

Testing requirements

Check the following functions:

Power-up voltage supplies

JTAG access to FPGAs

– The above will be covered by manufacturing JTAG tests

Clock distribution using onboard XTAL oscillator.

ByteBlaster2 access to configuration memory.

FPGA Configuration

VME access
- Control Registers
- PG memories

PG LVDS outputs – level & Jitter

PG Data and Sync Patterns

Clocks from TTC

Document changes

11.03.05 (Version 2.1)

- TTC Commands Added
- General Tidy-up

24/01/05 (Version2.0 created)

- LVDS cable connector change. Left and right columns swapped
- Reference to Pre-Processor use of Virtex2 corrected.