# *ATLAS Level-1 Calorimeter Trigger PreProcessor ASIC*
# *Final Design Review Summary*

The Final Design Review (FDR) for the ATLAS level-1 calorimeter trigger PreProcessor ASIC took place on Wednesday 14th June 2000 at the Kirchhoff-Institut für Physik in Heidelberg. The Review Panel consisted of:

Erik van Der Bij (CERN)
Paul Bright-Thomas (Birmingham University) - via audio link from Birmingham
Viraj Perera (Rutherford Appleton Laboratory)
Tony Gillman (Rutherford Appleton Laboratory) - Hardware Co-ordinator

Representing the Heidelberg group were:

Paul Hanke
Dan Husmann
Kambiz Mahboubi
Ullrich Pfeiffer
Cornelius Schumacher
Oliver Stelzer

The primary documentation available to the panel in advance of the review was the following:

"Specification of the PreProcessor ASIC (PPrASIC) for the ATLAS Level-1 Calorimeter Trigger" - July 1999
"Pre-Processor ASIC Design Guide" - Version 1.0, April 2000
"Pre-Processor ASIC User and Reference Manual" - Version 1.0, April 2000
(This and other documentation was at http://wwwasic.ihep.uni-heidelberg.de/atlas/projects/pprasic.html)

Based upon this documentation, the reviewers had submitted detailed lists of questions and comments to the designers several days before the review.

1. Agenda:

The review started at 09.15, with the first part consisting of a number of presentations by the Heidelberg group. These provided a detailed response to the majority of the points already raised by the reviewers in writing. In some areas, further clarification was given in response to questions. There was also some extended discussion of aspects of BCID functionality and performance. One or two suggestions from the reviewers for possible improvements to the design implementation, although of potential value, were felt to be too difficult to implement at this late stage.

The review continued with a line-by-line examination of a 33-point check-list, supplied by Viraj Perera, which listed the important questions to be asked prior to submitting a design for manufacture. Most of these points could already be ticked off satisfactorily, but a few must await the completion of the final layout simulations.

The afternoon session started with a discussion of a second list of written comments from Paul Bright-Thomas, to which the Heidelberg group had not yet had time to respond. Several of these points again related to BCID functionality, and some time was spent in discussing the important issue of correct handling of saturated pulses.

To ensure that all aspects of the design had been assessed, the following general topics were then discussed (although in some cases they had already been extensively covered in the morning session):

- Documentation
- Conformance with post-PDR specifications
- Environment and integration
- Simulation results
- QA programme
- Test strategy
- Schedule

At this stage, the reviewers spent some time in private discussion in order to draft their conclusions and recommendations, which were then presented to the Heidelberg group. The review closed at 17.00.

2. Conclusions and Recommendations:

The reviewers thank the Heidelberg group for their very thorough response to the long list of questions and comments which they were sent, and for being receptive to the majority of the suggestions.

In general, the reviewers felt that the PPrASIC design had been carried out systematically and thoroughly, and that there was an excellent probability it would be successful at the first submission without requiring a design iteration. This was especially important as some concern had been expressed initially at the omission of a small prototype batch of chips, although it had been explained that the relatively large die size (65mm2) indicated this to be preferable on economic grounds.

The following specific recommendations were made:

- Although the reviewers in general commended the documentation, they had found a number of instances where clear improvements should be made, both in text and figures. Particular attention should be paid to ensuring that details of the register formats and default values are correct. In addition, typographical errors and inconsistencies in notation should be removed.

- The User and Reference Manual should provide a clear definition and description of all interfaces to the ASIC. In addition, references to all associated external components should be supplied where appropriate.

- A number of differences between the post-PDR Specification Manual and the User and Reference Manual had been identified, so it is recommended that an Appendix be added to the User and Reference Manual listing and justifying all such changes.

- The reviewers were pleased to note that the specification of the inputs from the FADC chips had been modified to eliminate the resistors and provide for programmable inversion of the MSB. This would permit the ASIC to be used with other FADC chips.

- The implementation of the BCID algorithms should be described in more detail, with the aid of clear logic block diagrams. The overall BCID block should be shown in some

detail, with additional figures clearly illustrating the operation of the saturated and unsaturated pulse algorithms. The description of the BCID decision logic should be improved by the addition of a clear block diagram, and by extending the example table (Table 1.2) to include example LUT contents for the three BCID decision energy ranges.

- At present, the definition of the output data value from the BCID function in the case of saturated pulses is prone to error. An improved scheme, involving the addition of a writeable saturation-value register, should be adopted and documented clearly.

- Operation of the saturated-pulse BCID algorithm should be verified by simulation in the case of the (limited) data sample of LAr signals from Saclay, including its robustness against timing variations.

- It is recommended that the bit-allocation and pad ordering of the 10-bit output words from the ASIC to the CP and JEP modules ("ToCp" and "ToJp") be defined to present a sensible match to the LVDS serialiser input pins, without the need for any re-ordering on the MCM. The bit-allocations should be clearly and unambiguously shown, as this format cannot then be changed and will be used in the design of the CP and JEP modules.

- The use of the terms "DaisyIn" and DaisyOut" in the Serial Interface could create potential confusion when interfacing the ASIC on the host MCM. It is recommended that the option of cascading pairs of Serial Interfaces by means of external links on the host MCM should be avoided if possible.

- The possibility under consideration by the Heidelberg group of removing the ASIC internal scan path was considered risky. The recommendation is to retain it and to ensure that it spans the long (24-bit) counters.

- The reviewers were unclear about the exact status of the ASIC design simulations, as incremental design changes were still occurring. They therefore recommend that the design be frozen as soon as possible and then thoroughly simulated in that stable state before submission.

- Final design data should be entered into the CERN EDMS system.

The reviewers conclude that, subject to confirmation that the above points have been satisfactorily addressed and that the amended Check-List (attached) has been completed prior to submission, the design is approved for manufacture.

Tony Gillman