# A daughter-board with Line-Receivers (AnIn)

# on the Pre-Processor Module (PPM)

# of the

# ATLAS Level-1 Calorimeter Trigger

Version.1.2 (post-PDR)

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***Introduction.***

The design of the PreProcessor Module contains separate Daughter-Boards (AnIn_dPCBs) for receiving the analog calorimeter signals from the "Receiver Stations". The Receiver stations are placed in the proximity of the PreProcessor (PPr) system within the USA15 cavern housing the electronics racks for the Level-1 trigger system. Hence, the cable length to the PPr is moderate (a few meters). Nevertheless, the analog signals are transmitted differentially to minimise pick-up of noise.

The PPM receives signals on 4 connectors via its front-panel. This connector configuration is given by the "Receiver" design. Certain conditions are imposed there by the structure of the e.g. LAr calorimetry. Each cable carries 16 signals on twisted pairs. Hence, the PPM receives 64 analog signals in groups of 16 on four connectors.

It is logical to design one daughter-board corresponding to each connector. Exchangeability in case of electrical faults upstream is the main motivation. The exact functionality to be included in such a plug-on daughter-PCB shall be described in this document.

***The functionality of the "AnIn" daughter-board.***

The component content of the Pre-Processor-Module (PPM) shows the overall context in **Figure 1**. The AnIn-dPCBs shall, of course, be of the smallest size possible. The figure allocates an area of ca. 6cm width and 7cm height. These dimensions are not strictly fixed, but it is evident, that the four dPCBs must fit within the 366 mm height of the motherPCB (9 NIM-Units).

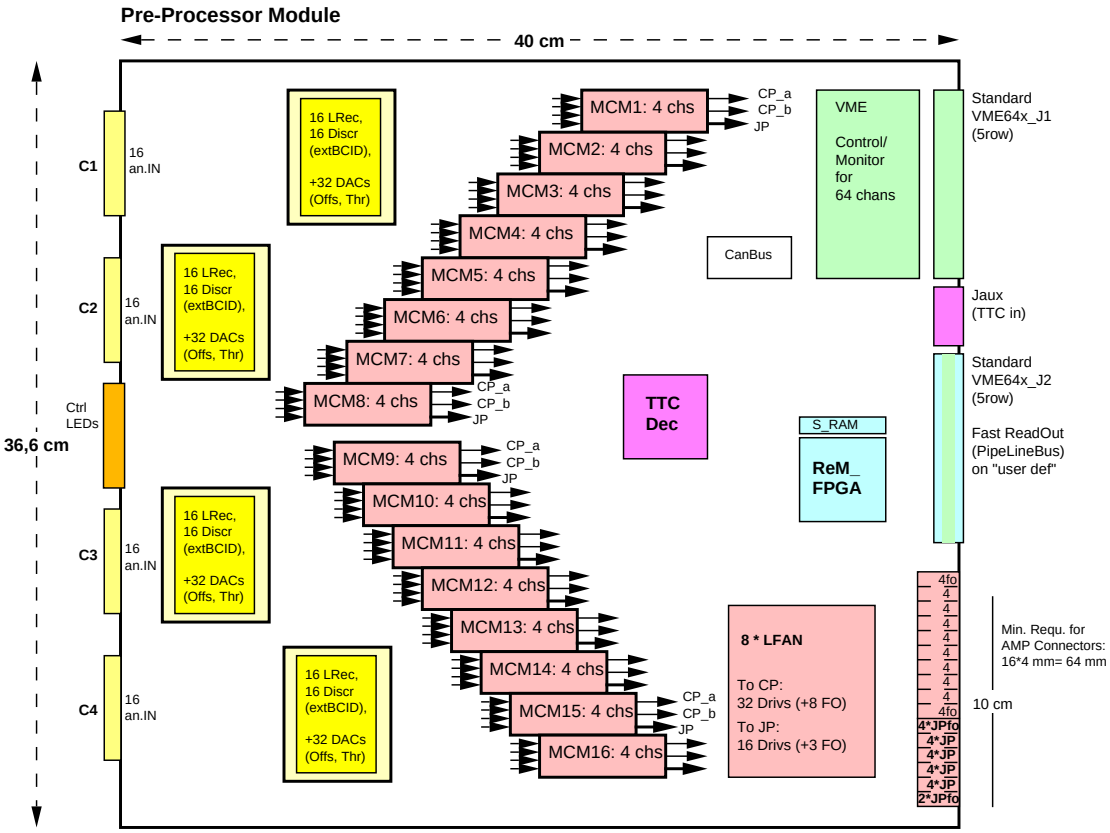


**Figure 1**

The functionality requirements for the AnIn_dPCB can be summarised as follows:

- Receive differential, analog signals from the input connector; adjust the gain on the uni-polar output to match the input-voltage window of the FADC (AD 9042; 1 Volt pp).
- The "Zero-line" offset must be adjustable via a DAC (8 bit, 2mV resolution giving 512 mV range looks sufficient).
- The uni-polar analog output to the PPrMCM (and the FADC thereon) should be of low impedance as done before on RD27 FADC_PCBs.
- 16 channels are required on ONE dPCB.
- The DAC(s) must be remotely programmable, i.e. it should interface to an I2C_Bus on the motherPCB.

Layouting of the AnIn_dPCB shall aim to cover more, namely "external BCID" shall be implemented in addition. This entails the following:

- The analog signal of each channel is fanned-out: first to the FADC, second to a discriminator.
- The discriminator is a simple "following comparator", i.e. it produces a logic "1" when the threshold is crossed by the input and goes back to "0" when the input falls below threshold (see also later).
- Another DAC sets the threshold for the discriminator. Again, a DAC with 8 bit, 4mV resolution giving 1024 mV range, is adequate.

- Also here, the DAC(s) must be remotely programmable, i.e. it should interface to an I2C_Bus on the motherPCB.

It should be noted, that the AnIn_dPCB can carry components on both sides of the board, which could make the extended functionality (Line Receiver and BCID discriminator) feasable.

***The design-idea and constraints for the "AnIn" daughterPCB.***

The approach to the physical outline, shown below in **Figure 2**, is a "most conventional" one. The height of the board is limited (four dPCBs of 7cm height require 280mm vertically on a motherboard of 366 mm height). The width could vary somewhat given the 400 mm width of the motherboard. However, it should also not exceed 7 cm, because of space needed for subsequent components on the PPM.

If component count, component placement and routing allow, the input/out pin grid spacing can be decreased. Technical implementation details (like choice of connector-type) are to be decided. However, the wide spacing of output pins shown, to separate FADC-outputs (analog) from ext.BCID-outputs (digital) by grounded copper, is a precaution to minimize the influence of a fast "digital" signal on the anlog signal to the FADC.

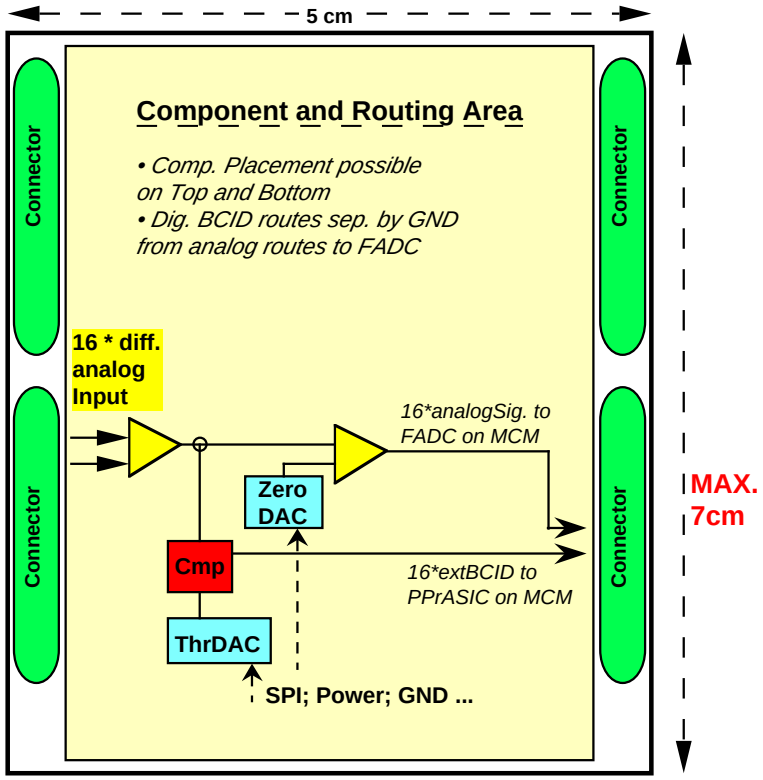


**Figure 2**

The functions to be implemented on the AnIn_dPCB are shown in **Figure 3**. The line-receiver **(1)** inverts the signal to be presented to the "extBCID" comparator **(2)**. The following Op. Amplifier decreases the signal (gain = 0.43) to match the input window of 1.0 Volt peak-to-peak for the AD9042 FADC **(3)**. The "Zero-line DAC" shall move the base-line to the nominal 20% level (e.g. 200 mV into the FADC range) to digitise the full bipolar swing of a LAr signal.

The scheme of "analog signal handling" is shown at the bottom of Figure 3.

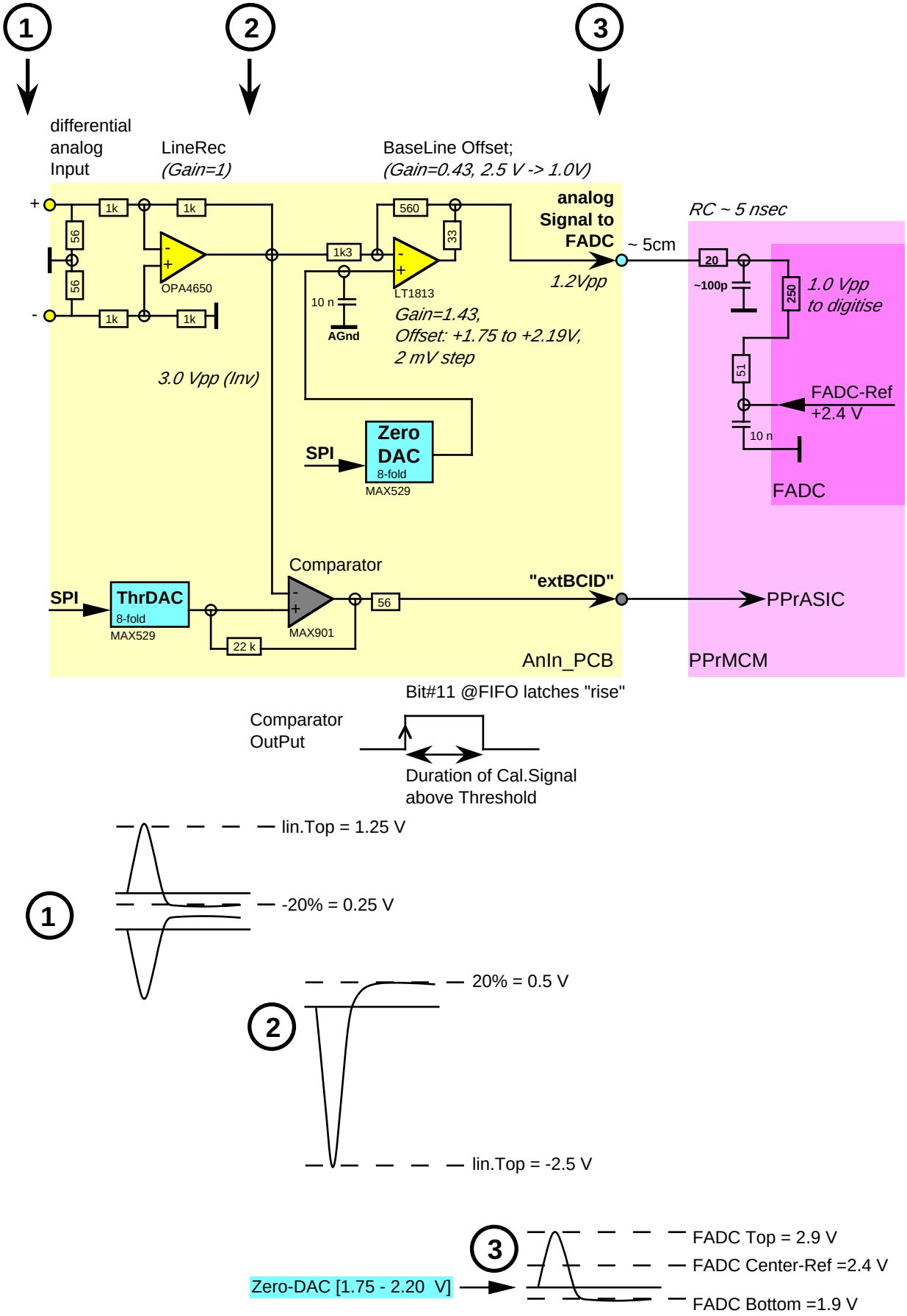
1
2
3
differential
analog
Input
LineRec
(Gain=1)
BaseLine Offset;
(Gain=0.43, 2.5 V -> 1.0V)
analog
Signal to
FADC
~ 5cm
RC ~ 5 nsec
1.2Vpp
1.0 Vpp
to digitise
OPA4650
LT1813
Gain=1.43,
Offset: +1.75 to +2.19V,
2 mV step
3.0 Vpp (Inv)
AGnd
SPI
Zero
DAC
8-fold
MAX529
FADC-Ref
+2.4 V
FADC
Comparator
"extBCID"
PPrASIC
SPI
ThrDAC
8-fold
MAX529
MAX901
AnIn_PCB
PPrMCM
Bit#11 @FIFO latches "rise"
Comparator
OutPut
Duration of Cal.Signal
above Threshold
lin.Top = 1.25 V
-20% = 0.25 V
20% = 0.5 V
lin.Top = -2.5 V
FADC Top = 2.9 V
FADC Center-Ref =2.4 V
FADC Bottom =1.9 V
Zero-DAC [1.75 - 2.20 V]

**Figure 3**

Some aspects of the design and their impact on the traversing signal deserve a more detailed description.

Handling of the analog signal.
The analog input signal from LAr Calorimeters is linear up to +( and - ) 3 Volt amplitude with a 20% (=600 mV) bipolar "undershoot'. The entire chain upstream from the trigger system is designed to ensure linearity over this range. None of the "analog" components on the Pre-Processor Module may clip this range to less. A maximum 3 Volt signal is carried linearly to the FADC input, where the range is mapped onto 1.2 Volt peak-to-peak. This is achieved by a signal-gain of 0.43 in the transmitting OpAmp (LT1813). The operation of the LT1813 -Amplifier with a gain significantly smaller than "1" will be tested in a prototype to be built immediately.

Only the FADC can clip (by Overflow) at an equivalent of 2.5 Volt input-amplitude. The FADC digitises within 1.0 Volt (2.4 Volt reference +- 0.5 Volt). Saturation is indicated only by the FADC, which overflows at its upper window-bound (FADC-value = 0x3FF).

The "offset", to reach the window, is given by a fixed voltage on top of which the input-level shift is achievd by an 8-bit DAC moving the "Zero-line" by appr. 500 mVolt. The tech. implementation gives in fact a range from +1.75 volt to +2.19 Volt to be compared to the lower bound of the FADC-window (= +1.9 Volt). The DAC-resolution (2 mV) is half of the FADC-resolution (1 Volt = 10 bit, i.e. 1 mV/count). The range is somewhat larger than needed. However, there might be "technical offsets" (e.g. OpAmp output offset) present, which require compensation.

Two cases shall be considered for clarity.

1. The positive LAr-signal and the 20% undershoot is mapped into the FADC by setting the appropriate "Zero-line offset". The LAr amplitude digitised will be +2.0 Volt to -0.5 Volt, where +2.0V corresponds to FADC-saturation (3FF).

2. The "offset" is chosen to put the "Zero-line" of the LAr-signal near the lower bound of the FADC-window. The LAr amplitude digitised will be +2.5 Volt to 0.0 Volt (minus epsilon), where +2.5V corresponds to FADC-saturation.

Adaption to properties of the input-stage of the AD9042-FADC.
The input gain may vary by +- 6% according to the AD9042 data-sheet. In addition, the input resistance of the FADC is 250 +- 50 Ohm. The latter, together with a series-resistor in the transmission-line results in an "ill-defined" voltage-divider. Hence, the series resistor should be of a smallest possible value. It can, however, not be "0", because of likely oscillation on the transmission line.

The technical implementation of the gain-calibration is achieved in the following way.
A default series resistor (e.g. 20 Ohm) is implemented on "external space" on the MCM. The gain of the FADC is measured in the production tests. The default resistor shall be modified by re-soldering to compensate the internal variation. Resistor values range between 5 Ohm and 35 Ohm to balance out the gain-variation and the variation of input-resistance.

The argument, that the individual calibration is not necessary, because such variations can be taken care of in the Look-Up Table downstream, is true. However, there are two valid reasons to do it nevertheless:

1. The number range availbale in the LUT is not partially used up by a "technical calibration", but is left for a true calibration of transverse particle-energy.

2. The Pre-Processor Multi-Chip-Module remains a "truely exchangable" hardware component. No recalibration is required after replacement. The argument for this fact is given in the specification of the "Pre-Processor Module".

Filtering (i.e. minimal cutting against "high" frequencies).
In discussion with LAr calorimeter representatives (W.Cleland), it was agreed to be useful to limit the bandwidth at the FADC input. A "simple" RC with a time-constant of 5-10 nsec was suggested. This is implemented by adding a capacitor on the "external space" at the MCM input.

However, variation of the resistor-value (see above) will inevitably lead to a variation of the RC time-constant relevant for band-width limitation. To keep RC fixed, also the capacitor is located on the "external space" of the MCM, where it can be changed by re-soldering.

Discrimination for "external BCID".
The "Technical Design Report" of 1998 contains a third option for a clock-independent BCID-mechanism to be realized as a free-running comparator on the "leading edge" of a calorimeter signal. This option shall be implemented on the AnIn_dPCB.

The signal is branched to a comparator, which simply "follows" the input, i.e. it produces a logical output as long as the input remains above threshold. However, pulses of amplitude just above the threshold produce an infinitesimal short output (glitch). This is not desirable. The phenomenon can be avoided by setting the energy-range (i.e. amplitude-range) in the BCID decision-logic of the PPrASIC. The working-range for this particular BCID-mechanism shall be chosen to start well above the comparator-threshold.

The comparator-result is sent across the motherboard to the PPrMCM input called "ext. BCID". The input circuit of the PPrASIC has a software-selectable latch working on the "rising" or "falling edge" of the LHC-clock.
Hence, the logic "1" of the comparator output is attributed to a time-slice with a resolution of half a clock-period. The correct bunch-crossing is then identified by timing the FIFO-depth accordingly.

Further Prototyping.
Following a small (3) number of prototypes, which can be tested with laboratory equipment (simple in-house made motherboard, pulse source, oscilloscope), a batch of e.g. 16 AnIn-dPCBs could be produced to cover the requirements for the four PreProcessor Module_0s.

***Appendix***

Signal Input-Output on the periphery of the AnIn plug-on board (input- and output-side are separated).

***Connector P1 ("Upper Input Side")***

| Pin# | Signal | | Pin# | Signal | |
|---|---|---|---|---|---|
| 1 | DataIN | | 2 | | G |
| 3 | | G | 4 | Ch1- | |
| 5 | free | | 6 | Ch1+ | |
| 7 | free | | 8 | | G |
| 9 | free | | 10 | | G |
| 11 | free | | 12 | Ch2- | |
| 13 | free | | 14 | Ch2+ | |
| 15 | free | | 16 | | G |
| 17 | free | | 18 | | G |
| 19 | free | | 20 | Ch3- | |
| 21 | free | | 22 | Ch3+ | |
| 23 | free | | 24 | | G |
| 25 | free | | 26 | | G |
| 27 | free | | 28 | Ch4- | |
| 29 | free | | 30 | Ch4+ | |
| 31 | free | | 32 | | G |
| 33 | free | | 34 | | G |
| 35 | free | | 36 | Ch5- | |
| 37 | free | | 38 | Ch5+ | |
| 39 | free | | 40 | | G |
| 41 | free | | 42 | | G |
| 43 | free | | 44 | Ch6- | |
| 45 | free | | 46 | Ch6+ | |
| 47 | free | | 48 | | G |
| 49 | free | | 50 | | G |
| 51 | free | | 52 | Ch7- | |
| 53 | free | | 54 | Ch7+ | |
| 55 | free | | 56 | | G |
| 57 | free | | 58 | | G |
| 59 | free | | 60 | Ch8- | |
| 61 | | G | 62 | Ch8+ | |
| 63 | CS | | 64 | | G |

***Connector P3 ("Lower Input Side")***

| Pin# | Signal | | Pin# | Signal | |
|---|---|---|---|---|---|
| 1 | CLK | | 2 | | G |
| 3 | | G | 4 | Ch9- | |
| 5 | free | | 6 | Ch9+ | |
| 7 | free | | 8 | | G |
| 9 | free | | 10 | | G |
| 11 | free | | 12 | Ch10- | |
| 13 | free | | 14 | Ch10+ | |
| 15 | free | | 16 | | G |
| 17 | free | | 18 | | G |
| 19 | free | | 20 | Ch11- | |
| 21 | free | | 22 | Ch11+ | |
| 23 | free | | 24 | | G |
| 25 | free | | 26 | | G |
| 27 | free | | 28 | Ch12- | |
| 29 | free | | 30 | Ch12+ | |
| 31 | free | | 32 | | G |
| 33 | free | | 34 | | G |
| 35 | free | | 36 | Ch13- | |
| 37 | free | | 38 | Ch13+ | |
| 39 | free | | 40 | | G |
| 41 | free | | 42 | | G |
| 43 | free | | 44 | Ch14- | |
| 45 | free | | 46 | Ch14+ | |
| 47 | free | | 48 | | G |
| 49 | free | | 50 | | G |
| 51 | free | | 52 | Ch15- | |
| 53 | free | | 54 | Ch15+ | |
| 55 | free | | 56 | | G |
| 57 | free | | 58 | | G |
| 59 | free | | 60 | Ch16- | |
| 61 | free | | 62 | Ch16+ | |
| 63 | | G | 64 | | G |

### *Connector P2 ("Upper Output Side")*

| Pin# | Signal | Pin# | Signal |
|---|---|---|---|
| 1 | + 5V (clean) | 2 | + 5V (clean) |
| 3 | + 5V (clean) | 4 | + 5V (clean) |
| 5 | G | 6 | G |
| 7 | ext,BCID_1 | 8 | G |
| 9 | G | 10 | An1 |
| 11 | ext,BCID_2 | 12 | G |
| 13 | G | 14 | An2 |
| 15 | free | 16 | G |
| 17 | VCC | 18 | VCC |
| 19 | free | 20 | G |
| 21 | G | 22 | An3 |
| 23 | ext,BCID_3 | 24 | G |
| 25 | G | 26 | An4 |
| 27 | ext,BCID_4 | 28 | G |
| 29 | G | 30 | G |
| 31 | free | 32 | free |
| 33 | G | 34 | G |
| 35 | ext,BCID_5 | 36 | G |
| 37 | G | 38 | An5 |
| 39 | ext,BCID_6 | 40 | G |
| 41 | G | 42 | An6 |
| 43 | free | 44 | G |
| 45 | VCC | 46 | VCC |
| 47 | free | 48 | G |
| 49 | G | 50 | An7 |
| 51 | ext,BCID_7 | 52 | G |
| 53 | G | 54 | An8 |
| 55 | ext,BCID_8 | 56 | G |
| 57 | G | 58 | G |
| 59 | free | 60 | free |
| 61 | G | 62 | G |
| 63 | G | 64 | G |

### *Connector P4 ("Lower Output Side")*

| Pin# | Signal | Pin# | Signal |
|---|---|---|---|
| 1 | G | 2 | G |
| 3 | G | 4 | G |
| 5 | G | 6 | free |
| 7 | ext,BCID_9 | 8 | G |
| 9 | G | 10 | An9 |
| 11 | ext,BCID_10 | 12 | G |
| 13 | G | 14 | An10 |
| 15 | free | 16 | G |
| 17 | VCC | 18 | VCC |
| 19 | free | 20 | G |
| 21 | G | 22 | An11 |
| 23 | ext,BCID_11 | 24 | G |
| 25 | G | 26 | An12 |
| 27 | ext,BCID_12 | 28 | G |
| 29 | G | 30 | G |
| 31 | free | 32 | free |
| 33 | G | 34 | G |
| 35 | ext,BCID_13 | 36 | G |
| 37 | G | 38 | An13 |
| 39 | ext,BCID_14 | 40 | G |
| 41 | G | 42 | An14 |
| 43 | free | 44 | G |
| 45 | VCC | 46 | VCC |
| 47 | free | 48 | G |
| 49 | G | 50 | An15 |
| 51 | ext,BCID_15 | 52 | G |
| 53 | G | 54 | An16 |
| 55 | ext,BCID_16 | 56 | G |
| 57 | G | 58 | G |
| 59 | - 5V (clean) | 60 | - 5V (clean) |
| 61 | - 5V (clean) | 62 | - 5V (clean) |
| 63 | - 5V (clean) | 64 | - 5V (clean) |