Specification of the Pre-Processor Multi-Chip Module (PPrMCM) for the ATLAS Level-1 Calorimeter Trigger

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Abstract

The smallest exchangeable electronics component in the Pre-Processor system will be the Pre-Processor Multi-Chip Module (PPrMCM). The PPrMCM contains most of the analogue and digital preprocessing of a group of four trigger tower signals. It integrates commercially available components with an Application Specific Integrated Circuit (ASIC) – the Pre-Processor ASIC (PPrASIC). The high degree of integration of the PPrMCM guarantees a physical size of the Pre-Processor system small enough to achieve the desired compactness in terms of printed-circuit boards, crates and racks. This specification document describes the PPrMCM in terms of implemented components. The input and output of signals is layed out as well as criteria for its design. Finally, the manufacturing and testing procedures are outlined. This document shall serve as base for the ATLAS-internal 'Preliminary Design Review' (PDR of the PPrMCM). Members of the panel for the Preliminary Design Review are: V.Perera, A.Gillman, C.Bohm, P.B-T.

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Introduction

The Pre-Processor system of the ATLAS Level-1 Calorimeter Trigger gets as input analogue trigger-tower signals from the calorimetry and it prepares digital data for pipelined processing in the subsequent Trigger Processors. One of the most important issues in ATLAS is the overall 'latency' of the trigger pipeline. This is the time required between a proton-proton collision in the LHC storage ring and the arrival of a Level-1 decision back at the front-end electronics of the different detector systems. Each component in the decision-making chain has to contribute as little as possible to the overall latency, because the holding time of detector data is limited to 2 μs. Most of this time is used by signal propagation to and from a central place, where the trigger is located. These considerations lead to a design of the Pre-Processor system, where a high degree of integration of electronics guarantees a compact layout. One compact component is the Pre-Processor Multi-Chip Module (PPrMCM), where commercial components in 'die' form as well as an Application Specific Integrated Circuit (ASIC) are grouped together.

1 The functional position of the PPrMCM in the Pre-Processor system

This specification describes a Multi-Chip Module (MCM), which plays an important role in the Pre-Processor system of the ATLAS Level-1 Calorimeter Trigger. The Pre-Processor MCM (PPrMCM) itself is actually the most essential building block of the Pre-Processor Modules

(PPMs). The modules are Printed-Circuit-Boards (PCBs) handling 64 signal channels. The Pre-Processor system comprises a 128 of such PPMs. Figure 1 shows a rough estimate of real estate on a PPM. Signal flow is from left (analogue input signals from the ATLAS calorimetry) to right (480 MBd[1] high-speed serial data output to the trigger processors as well as data read-out). The 16 pre-processing MCMs form the core of the module.

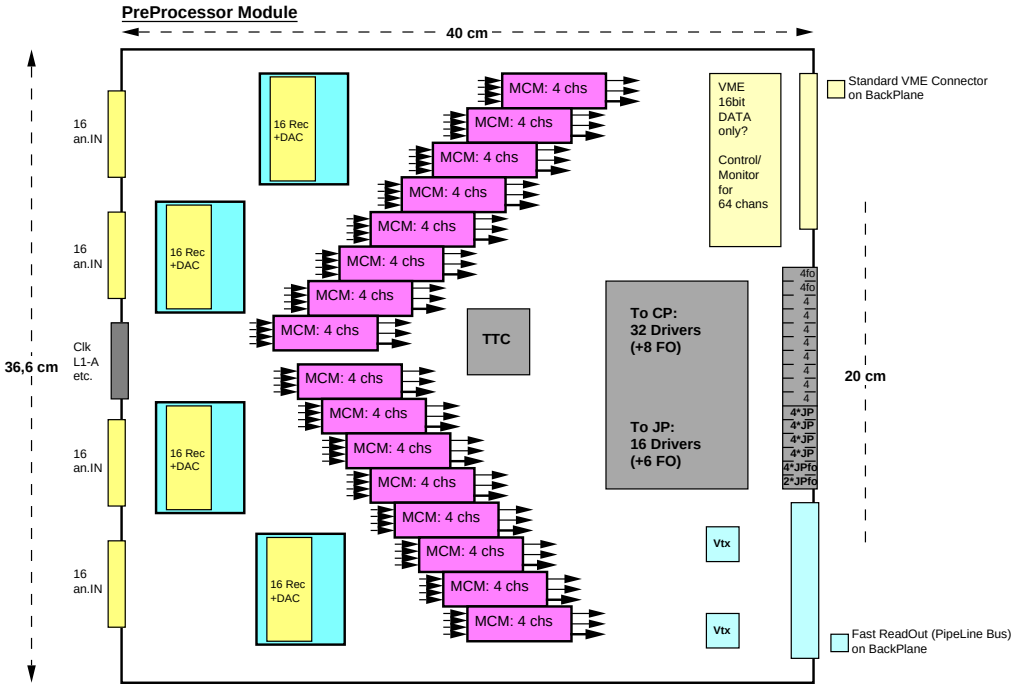

Figure 1: The position of the PPrMCM on the Pre-Processor Module..

1.1 Relevant documents

The documents of the ATLAS collaboration, on which this design is based, are: the ATLAS Level-1 Calorimeter Trigger User Requirements Document [URD98], and the ATLAS Level-1 Trigger Technical Design Report [TDR98]. The documents [Mah99], [Pfe99/1], [Pfe99/2], [PPr99], and [Sch99] are closely related to this document.

1.2 Requirements

The following summarizes the requirements for the PPrMCM: Four calorimeter channels are to be implemented on one MCM. Propagation of 'real-time' data must not exceed limits of latency

[1] The unit Bd (Baud) is the maximum number of the shortest codes (bits) per second in a transmission system, including protocol information. An LVDS link includes two protocol bits to a 10-bit data word.

outlined in the TDR for the Level-1 trigger. Power consumption of the PPrMCM should remain at the lowest possible value for reliable operation.

1.3 Functional description

A block diagram of the Pre-Processor Multi-Chip Module is shown in Figure 2. It will consist of 9 dies and it will be manufactured in a laminated MCM-L process, the same as investigated for the demonstrator Multi-Chip Module (PPrD-MCM). For details of the MCM-L production process see [Pfe99/2].

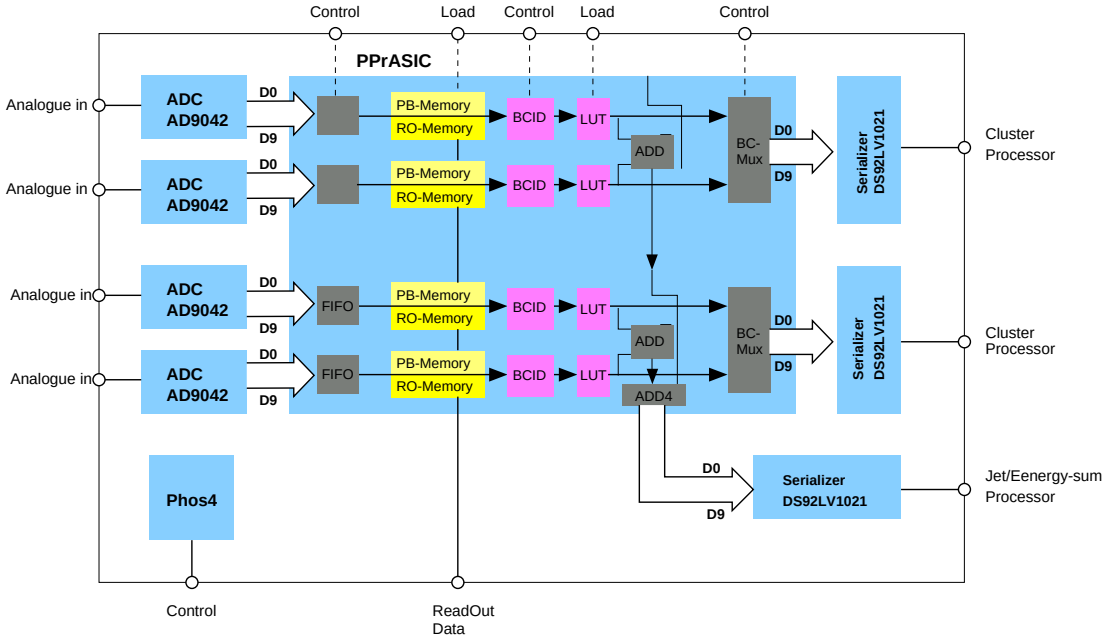

Figure 2: Block diagram of the Pre-Processor Multi-Chip Module.

The bock diagram of the PPrMCM contains four 12-bit ADCs (AD9042), one 4-channel Pre-Processor ASIC (PPrASIC), and serializers for the digital data transmission to the processors. Three LVDS chips will be used per MCM. A timer chip (Phos4) is needed for the phase adjustment of the ADC strobes with respect to the analogue input signals.

The design of the PPrMCM will benefit from the design experience established by the demonstrator project of the PPrD-MCM. The demonstrator MCM has a similar partition into dies and includes most of the preprocessing of four trigger tower signals. The main difference is that the demonstrator MCM digitizes only at 8-bit precision. It uses a former Pre-Processor ASIC prototype (FeAsic), and requires multiplexing of data and level-conversion to transmit four preprocessed trigger tower signals via one G-link device. The serial output data rate of the demonstrator MCM was 800 MBd or 1600 MBd. The serial data rate of the final PPrMCM will only be 480 MBd. The following is a short summary of the tasks of the PPrMCM. A summary of MCM design parameters is given in Table 1.

A: **Reception of analogue trigger tower signals:** The differential analogue trigger tower signals are received by a differential line receiver circuit. This circuit will be placed on the Pre-Processor Modules, as close as possible to the MCM input pins. The trigger tower voltage range is linearly mapped, with 0–2.5 V representing 0–250 GeV

PPrMCM parameter	
Analogue dies	4
Total number of dies	9
MCM area	∼14 cm^2
MCM form factor (width x length)	2 cm^2
Serial data rate	480 MBd
Power consumption	∼3 W
Temperature rise	∼+15 C°
Number of bonds	∼386
SMD connector pins	80
MCM thickness, inc. heatsink	12 mm

Table 1: Parameters of the PPrMCM. The MCM temperature assumes air cooling.

transverse energy (±10%). A programmable DAC with 10-bit resolution is used to adjust the zero baseline for each input signal. This DAC will be controlled by an I2C interface. The differential signals will be converted and attenuated to 1 V single-ended signals to match the ADC input range. The attenuation is achieved by a serial resistor and a capacitor to ground (low-pass). In order to optimize the crosstalk sensitivity of the analogue ADC input signals this circuit will be placed on the MCM close to the ADC bonding pads. The actual line receiver circuit is placed on the PPM.

B: **Digitization and phase adjustment:** Each analogue input signal will be digitized by an analogue-to-digital converter (ADC) with 10-bit resolution (12-bit ADC with the lowest two bits unused) [AD9042]. The time position of the sampling strobe with respect to the analogue input signal can be adjusted in steps of 1 ns within a range of 25 ns. This is required to perform the fine synchronization of each trigger tower signal and for sampling each pulse at its maximum. An ASIC (Phos4) developed by the CERN Microelectronics group will be used for this time adjustment [Phos4]. The programming of the Phos4 chip will be done through an I2C interface.

C: **Pre-Processing:** The pre-processing is done by a 4-channel PPrASIC. For a description of this essential part see [PPr99].

D: **Serial data transmission:** Preprocessed results will be sent to the downstream processors via high-speed serial links. A high-speed serial transmission is required to keep the number of data links to an acceptable value. The serial data rate is 480 MBd. Because of a prefered low power dissipation, LVDS serializer will be used [LVDS]. All differential LVDS signals from the MCM have to go to an LVDS buffer on the PPM. This buffer performs signal refreshing and fanout. After that buffer the signals are pre-compensated before send up to the differential cables for transmission.

1.4 Layout considerations for the PPrMCM

The motivation for the PPrMCM lies in the fact that the Pre-Processor system should be as compact as possible on one hand. The current design will allow an overall system size of 8 crates (9 NIM-units height), where failures due to e.g. power-supply problems should be minimal. On the other hand, the system should be as modular as possible. Failures of components or larger building blocks shall lead to minimal acceptance losses for a minimum of running time in the ATLAS experiment. Hence, good modularity for easy repair by exchangeable parts is an important issue.

The Pre-Processor is a primarily channel-oriented system, i.e. an analogue calorimeter input is processed and produces two digital output streams to the respective trigger processors downstream, namely the Cluster Processor (CP) and the Jet/Energy-sum Processor (JP).

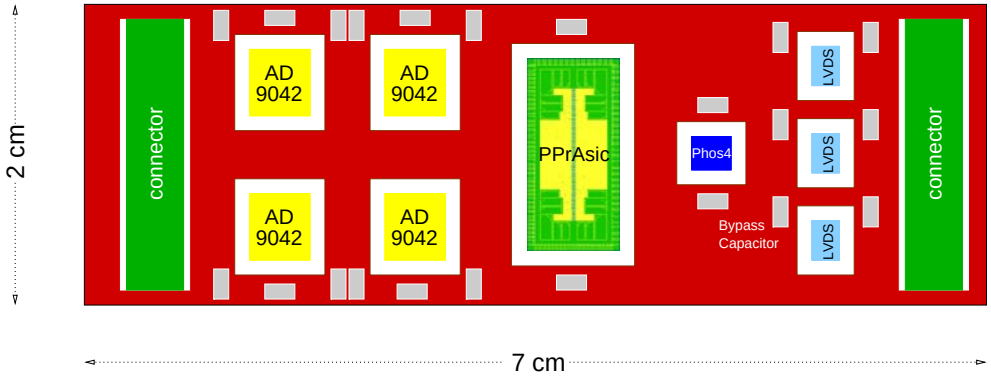

Figure 3: Pre-Processor Multi-Chip Module layout.

Figure 3 shows an outline of the PPrMCM layout. The signal flow is from the left (analogue input signals from the ATLAS calorimetry) to the right side of the device (480 MBd serial data output to trigger processors). The placement of dies shall take their power-consumption and removal of heat produced into consideration. These facts will be investigated quantitatively by simulations using appropriate tools in the Cadence design software. A lot of experience was gained during the development of the demonstrator MCM, where the signal processing was shown to work well on an 8-bit data path [Pfe99/2].

The choice of connectors as well as their reliability was proven by the demonstator MCM. The chosen analogue-to-digital converter (ADC) from Analog Devices [AD9042] has a 12-bit resolution, a 40 MHz sampling frequency, and a minimal 'latency' of 2.5 clock cycles (62.5 ns). The lowest two bits are unused to achieve the required 10-bit resolution for the PPrASIC inputs. The 4-channel delay ASIC [Phos4] was designed by CERNs Micro Electronics group. Production of 'dies' was done by Austria MicroSystems (AMS). A sufficient number of dies are tested at the facilities of KIP Heidelberg providing enough 'known good' dies for mounting on the PPrMCMs. The design and simulation of the PPrASIC is nearly finished. Production will proceed early 2000. Testing on the Wafer-Probe station at KIP Heidelberg shall also provide sufficient supplies of 'known good' dies for this essential component. Data serialization will be done by LVDS devices from National Semiconductor [LVDS] for the sake of reduced power-consumption. Fanning out, buffering, and pre-compensation of signals will be done on the PPM, close to the backplane connectors, to achieve a maximum drivable cable-length.

Information on exact foot-prints of the commercial dies (ADCs, LVDS serializers) is being obtained. It is needed for the MCM layout. Cut-outs for efficient heat transfer to the MCM substrate and estimation of routing space needed are important boundary conditions for layout work. The use of miniature connectors ensures exchangability of an PPrMCM without re-soldering. This allows several levels of repair in case of problems:

- PPM exchange during data acquisition time, which is fast for minimal loss of beam-time.
- PPrMCM exchange near the ATLAS experiment by trigger experts with minimal requirements for special tooling.
- PPM repair and re-test outside the ATLAS experimental area, which requires lots of special tooling.

A test-rig with ATLAS-like signal input/output and full software diagnosis will be required as well. These are practical points to contribute to maximum availability of the ATLAS trigger system. Another technical reason for the use of connectors is the life-time of the PPM motherboards. Solder/re- solder cycles will ruin a mother PCB faster than plug-on replacement.

2 Signal input/output of the PPrMCM

The number of signals in and out of the PPrMCM looks extremely small: Four analogue signals go in and 3 serial data streams of high-speed data leave the device. The following shall give the Input/Output requirements in detail and summarize the pin- allocation of the connectors. Most of the connector pins are used for control, clock, and power signals.

2.1 The real-time data path and supplies

- Four analogue inputs with accompanying grounds.
- Four analogue inputs for optional external BCID.
- Three (2 for CP, 1 for JP) high-speed serial outputs from LVDS transmitters, e.g. special routing to connector with accompanying ground potentials to provide matching impedance.
- Several 3.3 Volt supply lines from PPM level.
- Different ground references, e.g. analogue signal grounds for ADC.
- Digital grounds for subsequent devices, e.g. PPrASIC and LVDS serializers.

The ground potentials of the components shall be kept separated from each other also on the motherboard (PPM). Their connection to appropriate terminals ('clean earth', VCC ground) on the motherboard- and crate-level must be implemented.

2.2 Set-up/control and data readout

- I2C (to Phos4).
- LHC clock (40 MHz bunch crossing).
- Level-1 Accept (max. 100 kHz).
- Bunch crossing counter reset.
- Event counter reset.
- Synchronous start (for data playback and pipeline readout).
- Two serial interfaces for each 'pair of channels' from PPM level (eg. RemASIC/Xilinx-Virtex).
- Power-up signals for LVDS serializer.
- Analogue temperature monitoring signal from PPrASIC.
- JTAG from PPM level.

3 The design of the PPrMCM

Design flow, tools used and the manufacturing process are well described [Pfe99/2], Chapter 5. Experience gained in the demonstrator is, of course, highly valuable for this next step of design for a 'module 0' in ATLAS terminology. In fact, the current design is less demanding in several respects than the demonstrator. The most striking difference is the replacement of G-Links. Thermal management and signal handling become significantly simpler. The latter is due to the fact that conversion to PECL signal-levels is no longer necessary.

The effort to stay as fast as possible in terms of latency (less than 3 clock ticks for digital conversion) leads, however, to ADC candidates, which are rather demanding in terms of power (600 to 1000 mW). It must be pointed out though, that thermal handling of G-Link transmitters has been proven to be feasable on the demonstrator MCM. The total power dissipation of G-Links for 4 channels was 5 Watt, the handling of which was understood by simulation with the DF/Thermax tool and confirmed by measurements. This fact gives confidence, that four 'hot' ADCs together with 'low-power' LVDS serializers can be implemented on the PPrMCM.

3.1 The design process

The design process will closely follow the steps for the MCM demonstrator. All components (ADC, Phos4, PPrASIC, LVDS serializer) will have to be introduced into the libraries before schematics can be drawn. Also, simulation tools require careful definition of component properties in corresponding libraries.

The same MCM-L technology (DYCOstrate®) of the same manufacturer (Würth Elektronik, [Wue]) will be used. Experience with the software tools from the Cadence design suite, like the 'Advanced Package Designer (APD)' exists as well as knowledge of the design constraints imposed by the manufacturing process.

3.2 The simulation of the design (signal integrity and temperature)

An important role play the simulation tools in accompanying the development of the design. As for the demonstrator, thermal handling will be simulated with DF/Thermax as well as propagation of the high-speed serializer output with DF/SigNoise. Since simulation results were confirmed by measurements on the MCM demonstrator – or rather proved to be worst case estimations, the usefulness of these tools is beyond doubt.

4 Manufacturing and testing

4.1 The production process, component loading, bonding and encapsulation

Design documentation, emerging from the Cadence tool set, will be transmitted to the manufacturer for processing. After delivery of substrates, the bonding procedure will be started. It is not yet clear, whether component loading (positioning and fixation), wire-bonding and encapsulation for the 'module 0' prototypes will be done 'in-house' as for the demonstrator. In any case, the large number (ca. 2000) of MCMs for the final system will have to be handled by a contractor. It is probably worthwhile to search for, try out and establish the logistics for all three production steps at an outside company as early as possible.

4.2 The post-production testing to obtain 'known good' modules

Even though the PPrMCM is an exchaneable part on the Pre-Processor Module, testing of the produced MCMs as a stand-alone component is a necessary step before they are used on the module- (or system-) level. It is foreseen to devise a test procedure using analogue inputs and VME receivers for the LVDS outputs. The physical implementation of a test-PCB is not yet decided. A VME set-up using an 'open crate' (i.e. easily accessible) is one possibility. Test results will be recorded and cataloged in a computerized environment.

4.3 Summary tables for J1 and J2

The type used as connectors J1 and J2 provide 40 pins each. This connector allows a max. width of 20 mm for the PPrMCM substrate. The exact pin-allocation will be subject of the layout work. The following Table 2 and Table 3 shall only summarize the numbers of pins available to be used for their respective purpose. In order to minimize signal cross talk, analogue signals are located on J1 and digital signals are located on J2.

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12-Bit, 41 MSPS Monolithic A/D Converter
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DS92LV1021 and DS92LV1210 16-40 MHz 10-Bit Bus LVDS Serializer and Deserializer
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`http://www.national.com`

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A description of monitoring rates in hardware as well as "raw" transverse energy spectra
IHEP, Heidelberg, Germany 1999
`http://wwwasic.kip.uni-heidelberg.de/atlas/L1/DISCUSS/ppa_his_rate.pdf`

[Phos4] Phos4
PHOS4 – 4 Channel delay generation ASIC with 1 ns resolution
Datasheet, CERN — Microelectronics group

[Pfe99/1] Pfeiffer, U.
Bunch-Crossing Identification for saturated calorimeter signals
ATLAS Trigger/DAQ note, ATL-DAQ-99-009, University of Heidelberg, Germany 17 May 1999
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[Pfe99/2] Pfeiffer, U.
A Compact Pre-Processor System for the ATLAS Level-1 Calorimeter Trigger
PhD Thesis, Institut fuer Hochenergiephysik der Universitaet Heidelberg, Germany 19 October 1999
`http://wwwasic.kip.uni-heidelberg.de/atlas/publications.html`

Pin	Pad Name	Description	Signal
1	AIN1	analogue input ADC 1	analogue in
2	VCCA_ADC12	analogue power supply ADC 1 and 2	+5 V
3	VCC_ADC12	digital power supply ADC 1 and 2	+5 V
4	VDD_ADC12	digital power supply ADC 1 and 2, output stage only	+3.3 V
5	GNDA_ADC12	analogue ground ADC 1 and 2	gnd
6	GND_ADC12	digital ground ADC 1 and 2	gnd
7	AIN2	analogue input ADC 2	analogue in
8	AIN3	analogue input ADC 3	analogue in
9	VCCA_ADC34	analogue power supply ADC 3 and 4	+5 V
10	VCC_ADC34	digital power supply ADC 3 and 4	+5 V
11	VDD_ADC34	digital power supply ADC 3 and 4, output stage only	+3.3 V
12	GNDA_ADC34	analogue ground ADC 3 and 4	gnd
13	GND_ADC34	digital ground ADC 3 and 4	gnd
14	AIN4	analogue input ADC 4	analogue in
15	ExtBcid1	external BCID input channel 1	digital input
16	ExtBcid2	external BCID input channel 2	digital input
17	ExtBcid3	external BCID input channel 3	digital input
18	ExtBcid4	external BCID input channel 4	digital input
19	TempMeasure	temperature PPrASIC	analogue out, IOA 5P
20	GND_SUB	ground MCM substrate	gnd
21	GND_SUB	ground MCM substarte	gnd
22	GND_SUB	ground MCM substrate	gnd
23	GND_PHOS4	ground Phos4	gnd
24	VDD_PHOS4	power supply Phos4	+3.3 V
25	SDA	I2C data Phos4	input
26	SCL	I2C clock	input
27	A5	I2C address Phos4	input
28	A4	I2C address Phos4	input
29	A3	I2C address Phos4	input
30	A2	I2C address Phos4	input
31	CLK_Phos4	clock Phos4	input
32	CLK_ADC	clock to all ADCs	input
33-40	unused	common power/ground as required	power

Table 2: PPrMCM pin definition for connector J1.

[PPr99] Pre-Processor ASIC (PPrAsic)
Specification of the Pre-Processor Asic
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LVL1-Calo-URD-1.1.0, CERN, Geneva 10 April 1998
`http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/LEVEL1/L1CalURD.ps`

[Wue] Würth Elektronik
`http://www.wuerth-elektronik.de`

Pin	Pad Name	Description	Signal
1	GND_LVDS1	digital ground LVDS 1,2,3	ground
2	VCC_LVDS1	digital power supply LVDS 1,2,3	+3.3 V
3	VCCA_LVDS1	analogue power supply LVDS 1,2,3	+3.3 V
4	DOUT1+	non-inverted serial output LVDS 1	LVDS differential out
5	DOUT1–	complement of DOUT1+	LVDS differential out
6	TCK_LVDS1	transmit clock LVDS 1	40 MHz TTL input
7	GND_LVDS2	digital ground LVDS 1,2,3	ground
8	VCC_LVDS2	digital power supply LVDS 1,2,3	+3.3 V
9	VCCA_LVDS2	analogue power supply LVDS 1,2,3	+3.3 V
10	DOUT2+	non-inverted serial output LVDS 2	LVDS differential out
11	DOUT2–	complement of DOUT2+	LVDS differential out
12	TCK_LVDS2	transmit clock LVDS 2	40 MHz TTL input
13	DOUT3+	non-inverted serial output LVDS 3	LVDS differential out
14	DOUT3–	complement of DOUT3+	LVDS differential out
15	TCK_LVDS3	transmit clock LVDS 3	40 MHz TTL input
16	SerClk	clock serial interface PPrASIC	IB15P
17	SerFrame	frame select for serial interface PPrASIC	IB15P
18	SerIn1	serial interface input 1	IB15P
19	SerIn2	serial interface input 2	IB15P
20	SerDaisyOut1	daisy-chain serial interface output 1	OB33P
21	SerOut1	serial interface output 1	OB33P
22	SerOut2	serial interface output 2	OB33P
23	L1Accept	level-1 accept signal	IB15P
24	BcCntRes	bunch-crossing counter reset	IB15P
25	EvCntRes	event counter reset	IB15P
26	SyncPlayback	start synchronous playback	IB15P
27	SyncReadout	start synchronous readout	IB15P
28	Clk	PPrASIC clock	40 MHz
29	Reset	PPrAsic reset	IB15P
30	jtag_tdi	JTAG test data input	IB35P pull-up
31	jtag_tms	JTAG test mode select	IB35P pull-up
32	jtag_trst	JTAG test reset	IB35P pull-up
33	jtag_tck	JTAG test clock	IB15P
34	jtag_tdo	JTAG test data output	OB93P tri-state
35	GNDIO_PPRASIC	ground I/O pads only	gnd
36	VCC_PPRASIC	digital power supply core logic only	3.3 V
37	GND_PPRASIC	ground core logic only	gnd
38	VCCIO_PPRASIC	digital power supply I/O pads only	3.3 V
39	$\overline{\text{PWRDN12}}$	power down LVDS 1 and 2	TTL input
40	$\overline{\text{PWRDN3}}$	power down LVDS 3	TTL input

Table 3: PPrMCM pin definition for connector J2.