Specification of the Pre-Processor Multi-Chip Module (PPrMCM) for the ATLAS Level-1 Calorimeter Trigger

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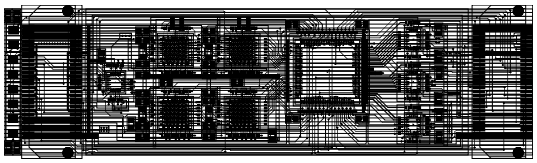

1:1 scaled view of the PPrMCM

Abstract

This specification will describe technical and electrical characteristics of the Pre-Processor Multi-Chip Module (PPrMCM) as required for its Final Design Review (FDR). Review Panel: x, x, x, x.

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1 Introduction

Most of the real-time signal processing and parts of the readout functionality of the Pre-Processor of the ATLAS Level-1 Calorimeter Trigger are integrated in a Multi-Chip Module (MCM). A MCM packaging technology is similar to hybrid circuits where many electronic components are mounted on a multi-layer substrate. In contrast to hybrids MCMs are encapsulated hermetically and hence are seen as a single module with hidden functionality from outside.

The Pre-Processor of the ATLAS Level-1 Calorimeter Trigger is a complex system which consists of many chips (dice). This makes it desirable to assemble many chips in a single package to reduce system size and printed circuit board complexity. The advantage of an MCM in the Pre-Processor system is that one-to-one connections between chips, e.g. wide digital buses, can be kept internal. Only signals like control, power supply and module input and output signals are used as package pins to interface to the outside board.

The PPrMCM technology can be classified by its substrate type. It is referred to as an MCM-L (laminated) technology. This technique was chosen to combine small feature sizes with low prices. The substrate is based on a multi-layer printed circuit board technology (PCB). It is an extension of chip-on-board technology (COB), where the bare dice are mounted directly on a substrate. The multi-layer structures are formed by etching patterns in copper foils laminated on an organic insulator core of Polyimid. Interconnections between layers are formed by 'blind' vias, which only extend from the surface part-way through the layers, or 'buried' vias, which connect only adjacent inner layers and do not extend to the surface in either direction. The smallest feasible layout structure in the design is referred to as feature size. The feature size of the MCM-L technology of the PPrMCM is 100 μm.

Related Documents

Due to the complexity of the MCM the following chip specifications and documents are of importance for the understanding of the electronics functionality.

- Chip Specifications: [ADC], [PPrAsic], [LVDS], [Phos4]
- Module Specifications: [PPM], [ROD]
- Thesis: [Ste00], [Pfe99/2]
- First Level Trigger TDR: [TDR98]

2 Pre-Processor System Overview

The Calorimeter Trigger gets analog input signals from the electro-magnetic and the hadronic calorimeters. These signals are summed separately in order to form trigger tower signals with a granularity of 0.1 x 0.1 in the η and ϕ directions. All in all the Calorimeter Trigger has about 7296 analog input signals, which are transmitted electrically via twisted-pair cables from the detector to the Level-1 Trigger electronics, located in the trigger cavern. The maximum cable length for trigger input signals is 60 m.

The Pre-Processor at the front-end of the ATLAS Level-1 Calorimeter Trigger links the ATLAS calorimeters with subsequent Calorimeter Trigger processors. It provides the digital data to identify objects of interest for the decision making on Level-1. The preprocessing includes digitization, identification of the corresponding bunch-crossing in time (BCID), calibration of the transverse energy, rate monitoring, readout of raw trigger data, and high-speed data transmission to the subsequent processors. The preprocessing of a large number of analog signals requires a compact system with fast hard-wired algorithms implemented in application-specific integrated circuits (ASICs) and Multi-Chip Modules (MCMs).

The basis of the Pre-Processor System is a compact 64-channel Pre-Processor Module (PPM). This modularity with a high degree of component integration is required to pre-process all trigger tower signals economically in eight electronics

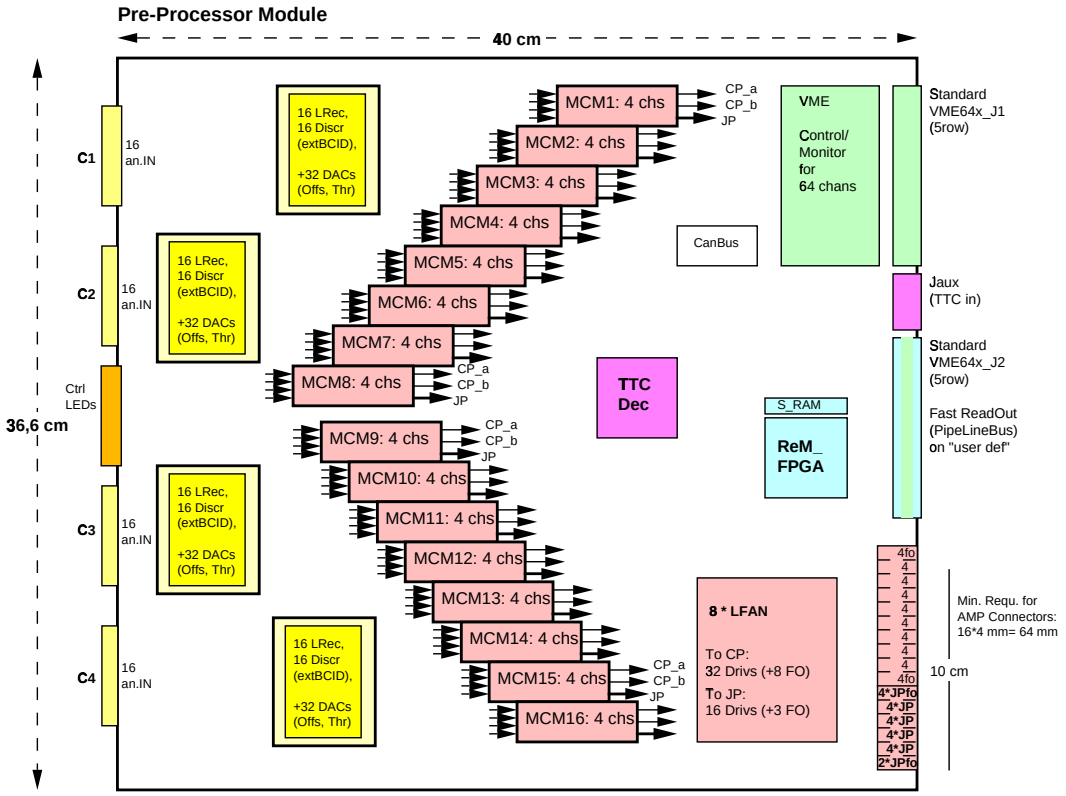


Figure 1: Pre-Processor Module block diagram

crates. Unused channels of the Pre-Processor should be grounded on the front-panel or maybe used to monitor noise effects throughout the up-stream trigger-tower electronics. Unused channels can be switched off by loading an appropriate look-up table content to the PPrAsic. A Receiver Station in front of the Pre-Processor converts the analog input signals to transverse energy within a ± 5 % band. The output results from the Pre-Processor System are sent via serial LVDS links to the down-stream processors, including duplication at ϕ-boundaries. All in all the Pre-Processor consists of 128 such modules. See [TDR98] for a detailed description of the tasks. The tasks on its input signals can be summarized as follows:

- **Preprocessing:** Provide the trigger processors downstream with digital data containing the transverse energy deposited, identified with the corresponding bunch-crossing. For the Cluster Processor (CP) the granularity is 0.1×0.1 for $|\eta| < 2.5$ and for the Jet/Energy-Sum Processor (JEP) the granularity is 0.2×0.2 for $|\eta| < 4.9$. In both cases the input data are separate for the electro-magnetic and the hadronic calorimeters.
- **Readout of event data:** Raw trigger data from the Pre-Processor are needed to be able to tell what has caused a trigger and to allow monitoring of the performance of the trigger system.

A 64-channel Pre-Processor Module has to carry 16 PPrMCMs. Input connectors for 64 differential analog signals will be located at the front panel. On the backplane side of a module the readout bus connectors (PipelineBus), the VMEbus connectors, and the connectors for the serial LVDS links will be located.

Figure 1 shows a block diagram of the Pre-Processor Module board space. The module will have 9 units (9U = 36,6 cm) and 40 cm in depth. The position of the PPrMCM on the Pre-Processor Module was optimized in terms of good heat exchange and a minimum of cross talk between the high-speed MCM output signals and the analog inputs. This figure makes it obvious that efficient signal routing and component placement will be of importance, and that the feasibility of

64 channels per module relies on the Pre-Processor MCM being compact in size. See [PPM] for a specification of the Pre-Processor Module.

3 Functional Description of the PPrMCM

The PPrMCM contains the preprocessing and the readout of the ATLAS Level-1 Calorimeter Trigger, for four trigger tower signals, in a single electronics module. The boundaries of the PPrMCM package were chosen at points of the processing chain where only few signals come in and out of the MCM package. The MCM has analog and digital signals as inputs and outputs, respectively, and it includes different semiconductor devices such as mixed-signal and pure digital chips. Some of them are commercially available and others are application specific. The MCM processes four trigger tower signals using a Pre-Processor ASIC developed at the ASIC laboratory of the University of Heidelberg [PPrAsic].

A schematic like block diagram of the PPrMCM is shown in Figure 2. It contains 9 dice: four ADCs [ADC], one four-channel Pre-Processor ASIC [PPrAsic], three LVDS serializers for the digital data transmission to the subsequent processors [LVDS], and a timer chip [Phos4], needed for the phase adjustment of the FADC strobes with respect to the analog input signals.

The tasks of the PPrMCM are:

- to digitize four analog trigger tower signals at 40 MHz with 10-bit resolution. Digitization at 12-bit is used to extend the effective number of bits. This means, the lowest two bits are not connected to the PPrAsic;
- to pre-process each trigger tower data in terms of energy calibration and bunch-crossing identification;
- to serialize pre-processed trigger tower data using high-speed Bus LVDS chip-sets.
- to provide dead-time free readout of four trigger towers.

In order to achieve these, the MCM consists of:

- four ADCs from Analog Devices (AD9042, [ADC]);
- one four-channel PPrAsic, providing readout and preprocessing;
- one timer chip [Phos4], needed for the phase adjustment of the FADC strobes with respect to the analog input signals;
- three Bus LVDS Serializer ([LVDS]) serializing 10-bit at 40 MHz (400 Mbps user data rate, 480 MBd including start- and stop bit).

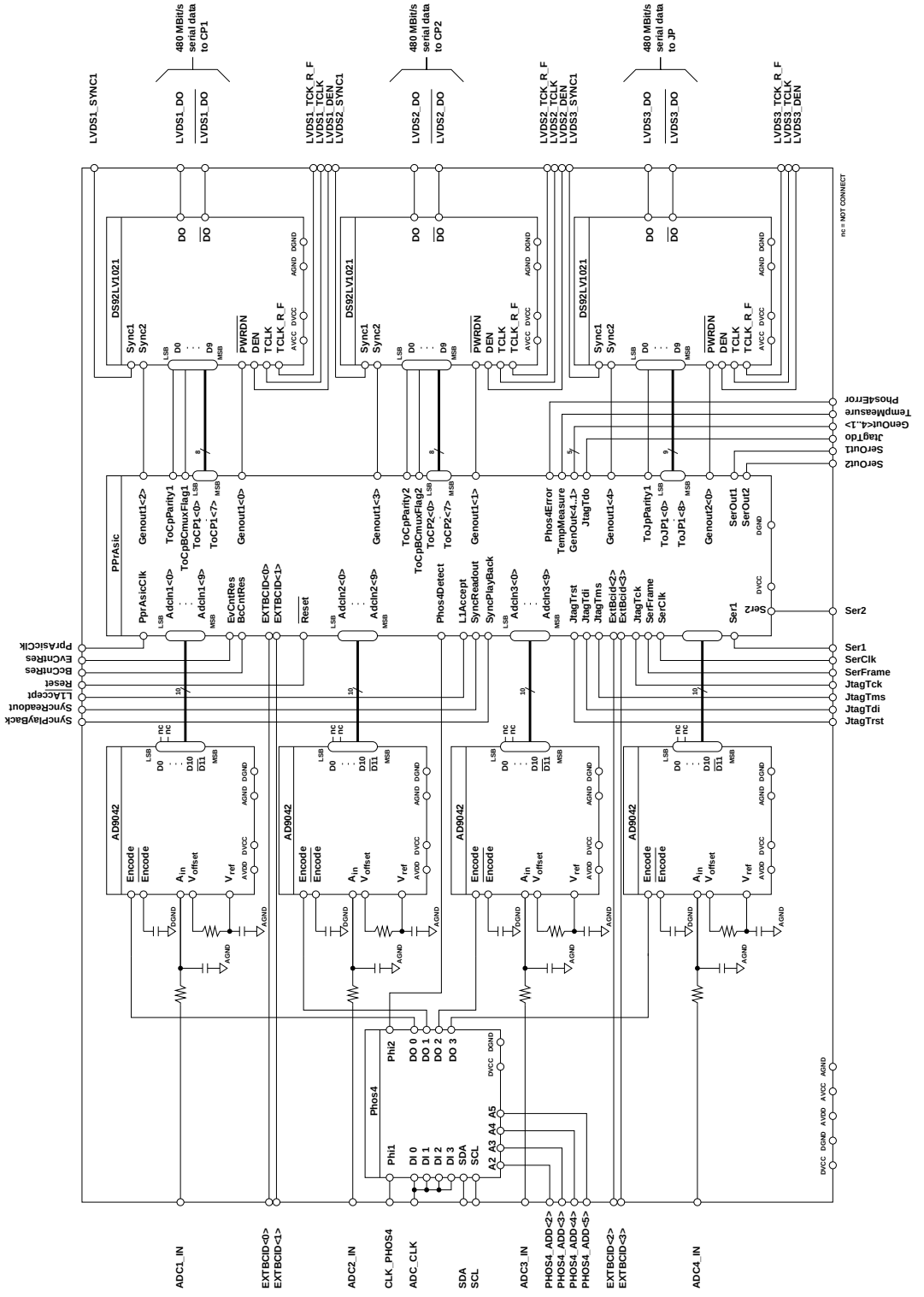


Figure 2: MCM functional block diagram

The block diagram shows the scope of the MCM, where wide parallel data buses are kept internal and only analog input, control, and the high-speed serial data signal come out of the MCM package. Each component has its own clock input, which will be buffered externally with the same clock phase. To ensure valid data at the following stage the rising or falling edge of the PPrAsic clock can be programmed. Programming is required because the ADC clock phase is adjustable channel-by-channel to the analog input pulse maximum. This is required to optimize BCID performance. The ADC clock phase is programmable in steps of 1 ns by the Phos4 Asic within 25 ns. The LVDS clock edge can be selected externally to meet the timing requirements at its input.

The real time signal processing flows from the left to the right. First, the FADC digitizes the analog trigger tower signals at 40 MHz to 12-bit precision (10-bits used) in a range of 1 V peak-to-peak around the internal generated 2.4 V reference voltage. Each FADC die generates its own reference voltage. The offset adjustment and scaling from the 2.5 V input signal range to this 1 V range is done by the analog input board shown in Figure 4. Next, the four 10-bit data buses are each digitally pre-processed inside the PPrAsic. The PPrAsic output is interfaced to three LVDS Serializer chips. Due to the use of bunch-crossing multiplexing (BC-mux) one LVDS chip can transmit the data from two ADCs. Due to coarser jet-elements the LVDS used for data transmission to the Jet/Energy Processor transmits the data from four channels.

Due to the complexity of the PPrAsic it has its own review. Ihe PPrAsic data path contains a look-up table (LUT) for data calibration and a Bunch-Crossing Identification unit (BCID) for unsaturated and saturated trigger tower signals. The unsaturated BCID unit consists of a finite impulse response filter (FIR filter) with configurable coefficients and a peak finder. The saturated BCID unit consists of a set of registers and comparators. The readout data path can record data from a pipeline memory up to a level-1 accept rate of 100 kHz for five time-slices including the BCID result.

3.1 MCM I/O Signals

The MCM I/O signals can be divided into three groups: analog input signals, digital output signals, control and readout signals. These signals will be described in the following.

Analog Input Signals

The analog twisted-pair trigger-tower signals are separate for the electro-magnetic and hadronic calorimeter. They are reordered by the Receiver Station in front of the Pre-Processor to the azimuth-oriented architecture of the trigger system. One can distinguish between PPMs exclusively assigned to em-signals and those assigned to had-signals. One PPM covers a trigger space of 0.4 x 1.6 in the η and ϕ direction. This corresponds to 4 x 16 signals each 0.1 x 0.1 in η and ϕ for the central region ($\eta < 2.5$). The signal mapping to PPMs in the forward direction above $\eta > 2.5$ is described in [PPM] where 'thinned out' cables are used to allow identical PPMs to be used. The differential signals are coming in via four Sub-D 37c connectors on the front panel. A footprint of the Sub-D 37c connector on the PPM board can be seen in Figure 3. The pair numbers are ordered along the front-panel from top to bottom. A group of four signals pairs cover a 0.2 x 0.2 area clockwise. In order to allow BC-multiplexing along ϕ inside the PPrAsic, a re-ordering of signal traces is required on the MCM. Up to the MCM, signal traces are straightforward connected through the analog input boards, used for signal conditioning and 'external BCID'. On the MCM, single-ended outputs of the analog input board are reordered in such a way that signal 1 and 4 are connected to the PPrAsic channels 1 and 2, and signal 2 and 3 are connected to PPrAsic channel 3 and 4.

The voltage range V_{tower} of the ADC corresponds to 0 to 250 GeV transverse energy deposited in the detector. The trigger-tower signal is bipolar shaped in case of the Liquid-Argon Calorimeter (LAr), with an undershoot of V_{under} (20 %). It is unipolar in case of the Tile Calorimeter. The voltage range V_{tower} is mapped to the digitization range V_{ADC} of the ADC. This is done by the analog input board in front of the MCM. This circuit is shown in Figure 4. The board has a low impedance output amplifier in order to eliminate gain variations introduced by variation of the ADC input resistance $R_{in,ADC}$. It is also used for baseline shift and to create an 'external BCID' signal connected to the PPrAsic. Intrinsic gain variations of the ADC will be compensated digitally by loading an appropriate look-up table content into the PPrAsic. Each input stage of the PPrMCM has a low-pass filter to reduce high frequency noise as close as possible to the ADC

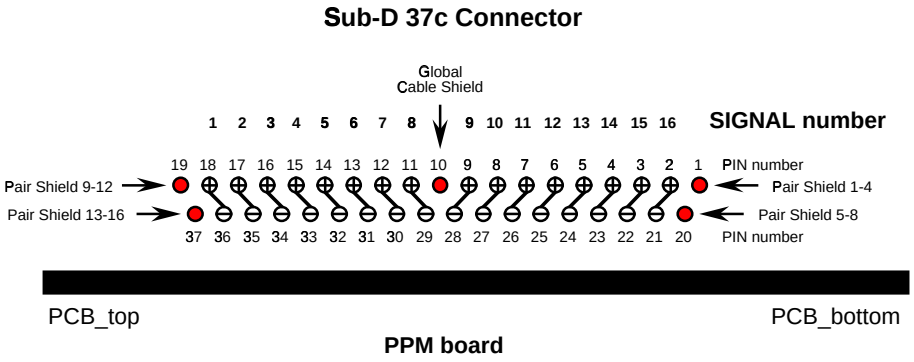


Figure 3: Pinning of the PPM front-panel connector from LAr calorimeters.

input. Default RC values are 5ns for manufacturing. If it turns out, during the final MCM test, that the input impedance variation of the ADC ($R_{in,ADC}$) is effecting the gain, an adaption of the resistor and capacitor values is required to match the gain criteria by keeping the RC value constant. This procedure will be part of the final MCM parameter test after encapsulation. These components are accessable for later re-soldering on an 'RC-balcony'. See Section 5.1 for a mechanical description. The analog return current of the input signals stage of the ADC will be kept separate of the digital by introducing an analog ground, connected to adjacent pins for shielding reasons.

Digital Output Signals

The PPrMCM delivers three BUS LVDS serial output streams at a serial data rate of 480 MBd (SDR). The user data rate, excluding a start and a stop bit, is 400 Mbps (UDR). Each serial output is generated from an DS92LV1021 Bus LVDS serializer from National Semiconductor. This device transforms a 10-bit wide parallel CMOS data bus from the PPrAsic into a single Bus LVDS serial data stream with an embedded 40 MHz clock. Two of the serial data streams contain the data to the Cluster Processor, which represent energy deposits on the 0.1 x 0.1 η and ϕ grid. The third stream contains energy deposits on the 0.2 x 0.2 grid, which are to be sent to the Jet/Energy Processor. The Cluster Processor data contains a 8-bit energy value, one BC-mux flag bit, and one odd parity bit. The Jet/Energy Processor data contains a 9-bit energy value and one odd parity bit.

The LVDS output traces are matched to 100 Ohm differential impedance. No pre-compensation circuit is required on the MCM, since the LVDS signals are refreshed on the PPM motherboard. A pre-compensation network is only used at the output stage of the motherboard LVDS buffer to drive the signal over a few meters of cable. This circuit does not influence the LVDS output section of the MCM.

Link tests at Birmingham, Heidelberg, and Mainz indicate low bit-error rates and acceptable link performance over 20 m long cables. The DS92LV1021 Bus LVDS Serializer is designed to work with the DS92LV1210 Deserializer, which requires a clock-jitter better than 150 ps. But, the TTCrx chip on the PPM may have a clock jitter of up to 250 ps, which makes it necessary to use the DS92LV1212A as an upgrade on the receiver end. This chip is an upgrade of the DS92LV1212 device which tolerates a minimum of 450 ps jitter the typical value is 730 ps. It maintains all of the features of the DS92LV1212 and is designed to be used with the DS92LV1021 Bus LVDS Serializer. Hence, a low jitter PLL at the PPM board level is not required to ensure a clock jitter better than 150 ps for the LVDS Serializer used on the MCM.

Control Signals and Readout Signals

The control and readout signals can be summarized as follows:

- I2C (Phos4)

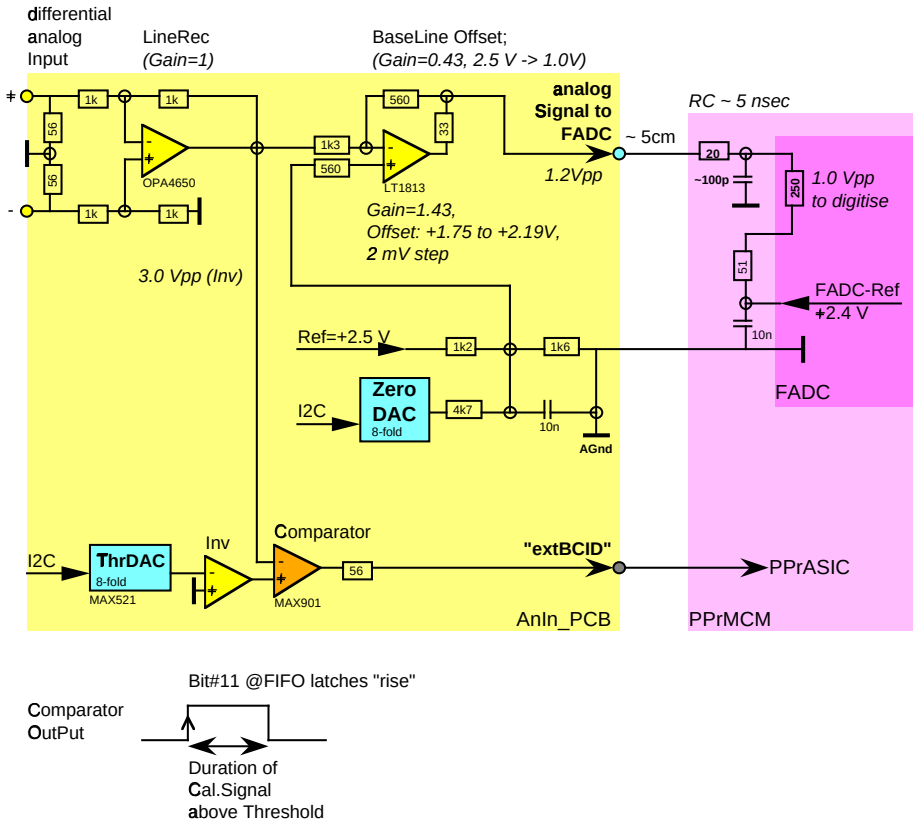


Figure 4: Block diagram of the analog input signal generation circuit

- JTAG (PPrAsic)
- Serial shift register (PPrAsic)

The I2C interface is used for Phos4 programming. The JTAG interface is used for in-circuit testing and boundary-scan of the PPrAsic. The JTAG interface provides boundary-scan I/O, to pre-load defined pad states and to scan the values received from the ADC. This is a very useful test feature for the MCM production test to identify connectivity problems inside. The serial shift register is the main readout path of the MCM. It is connected to a configurable device called RemFPGA located on the PPM. At the moment it is not intented to use the PPrAsic daisy-chain option, since routing board space on the PPM does not seem to be a problem. A temperature measurement diode on PPrAsic will be connected to an external resistor, which allows to monitor the MCM temperature via the PPM CAN-bus interface.

Readout operations of the PPrAsic are triggered by a Level-1 Accept signal, generated by the CTP and distributed by the TTC system. The TTC system distributes all timing information synchronously to all destinations. This includes the LHC clock, the bunch-crossing number (BCID-number), as well as the event-number (L1ID) and broadcast signals. Also reset signals for internal counters to maintain synchronization for the bunch-crossing number and Level-1 number is distributed via TTC. The MCM will use TTC broadcast signals to trigger the LVDS SYNC pattern, as well to trigger the PPrAsic reset and to start synchronous readout and playback. The following table is a summary of TTC signals connected to the PPrMCM. Please refer to the PPrAsic specification [PPrAsic] and to the ROD specification [ROD] for further details about the readout.

Table 1:

Symbol	Parameter	Default
Reset and Broadcast Signals from TDC		
EVCNTRES	PPrAsic event-number reset	
$\overline{\text{RESET}}$	PPrAsic reset signal	
BCCNTRES	PPrAsic bunch-crossing number reset	
L1ACCEPT	Level-1 accept signal	
SYNCPLAYBACK	start synchronous playback	
SYNCREADOUT	synchronize readout	
LVDS_SYNC	SYNC pattern for LVDS	

Internal Signals

The *Phos4Detect* signal on the MCM is connected from the Phos4 *Phi2* output to the PPrAsic *FreqIn* input. The frequency detection circuit in the PPrAsic is able to discriminate a frequency applied at the *FreqIn* input. This frequency detection is foreseen to be used for monitoring of the Phos4 phase detection output, which sends a signal with a frequency between 2 MHz and 6 MHz, when the Phos4 chip is operating correctly. The Phos4 chip loses all its programmed timing settings, if a momentary loss of its clock signal *Clk_Phos4* appears. In normal operation this should not be the case since the MCM *Clk_Phos4* pin is connected to a stable and free running quarz oscillator on the PPM motherboard.

The PPrAsic frequency detector checks, if the signal applied at *FreqIn* has a frequency higher than 0.3 MHz. If the frequency is lower or the signal has a constant value, the MCM *Phos4Error* output is set to 1. The frequency detection works reliably for frequencies up to 20 MHz. Higher frequencies may not be detected correctly, depending on how phase and frequency are related to the 40 MHz system clock of the PPrAsic. The *FreqLost* signal is also included in a read-back status word.

Power-up Sequence and Initialization

The Serializer has a synchronization mode that should be activated upon power-up of the MCM. The Deserializer will establish lock to this signal within 1024 cycles, and will flag lock status. Before data can be transmitted, the MCM must be initialized. Initialization refers to synchronization of the LVDS Serializer PLLs to the local 40 MHz clock. After MCM power-up and PPrAsic reset the MCM is in 'transparent mode'. This mode will bypass 10-bit data from the ADCs to the LVDS Serializers. The LVDS Deserializers, which are located in the Cluster Processor and Jet/Energy Processor, have to synchronize to the MCM outputs. The MCM Serializer outputs are held in tri-state, while the LVDS PLL locks to the 40 MHz clock (LVDS TCLK pin). The Serializer is then ready to send data or SYNC patterns depending on the levels of the SYNC1 and SYNC2 inputs. The SYNC pattern is composed of six 'ones' and six 'zeros' switching at the 40 MHz input clock rate. Please refer to the Serializer specification [LVDS]. The transmission of SYNC patterns to the Deserializer enables the Deserializer to lock to the Serializer. One or both of the Serializer SYNC inputs have to be asserted for at least 1024 clock cycles to initiate transmission of SYNC patterns. The MCM Serializer will continue to send SYNC patterns after the minimum of 1024 cycles if either of the SYNC inputs remains high.

If the Deserializer loses lock, its $\overline{\text{LOCK}}$ pin will go high. This must be monitored by the Processors to detect a loss of synchronization and the system must arrange to assert the Serializers SYNC1 and SYNC2 pin to re-synchronize the links. This takes at least 1024 clock cycles. The SYNC1 input pin is programmable via the serial interface of the PPrAsic and can be asserted by software, where the SYNC2 pin is an external MCM pin which will be set via a Trigger Timing and Control (TDC) broad-cast.

The edge of TCLK used to strobe in data is selectable via the TCLK_R/F pin. TCLK_R/F high selects the the rising edge for clocking data and low selects the falling edge. The MCM outputs (DO$\pm$) transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$=high and SYNC1 and SYNC2 are low. The DEN pin may be used to tri-state the outputs when driven low. The $\overline{\text{PWRDN}}$ signal shuts down the Serializer PLL and tri-states outputs putting the LVDS into a low power sleep

Table 2:

Symbol	Parameter	Default
Default Conditions		
GenOut1<4..0>	generic outputs of PPrAsic channel 1	0b'00011
GenOut2<4..0>	generic outputs of PPrAsic channel 2	0b'00011
GenOut1<2>	LVDS1 SYNC2 to CP	0b'0
GenOut1<3>	LVDS2 SYNC2 to CP	0b'0
GenOut1<4>	LVDS3 SYNC2 to JP	0b'0
GenOut1<0>	LVDS1 $\overline{\text{PWRDN}}$	0b'1
GenOut1<1>	LVDS2 $\overline{\text{PWRDN}}$	0b'1
GenOut2<0>	LVDS3 $\overline{\text{PWRDN}}$	0b'1
LVDS1_DEN	external MCM pin	0b'1
LVDS1_TCLK_R/F	external MCM pin	0b'1
LVDS2_DEN	external MCM pin	0b'1
LVDS2_TCLK_R/F	external MCM pin	0b'1
LVDS3_DEN	external MCM pin	0b'1
LVDS3_TCLK_R/F	external MCM pin	0b'1

mode. After a power-up of the MCM and a reset of the PPrAsic the defaults in Table 2 ensure that all LVDS Serializers are enabled to transmit valid data.

The three BUS LVDS serial output streams will be buffered on the PPM to be refreshed before transmission via twisted-pair cables on the PPM backplane connectors. Currently two options exist for that purpose. First an in-house developed ASIC called 'LFAN', which is an 8-fold differential LVDS buffer chip providing sufficient output current to drive LVDS signals across the cable connection between processor crates. Fan-out of LVDS signals to different processors at η boundaries is done by distributing the serial signal to two LFAN inputs. The second option is to use an XILINX Virtex FPGA with LVDS in- and output pins. Fan-out in this case is done by programming the device. All LVDS signals will be terminated with a 100 Ohm differential impedance at the input of the buffer chip.

4 Design Experience

The design of the PPrMCM will benefit from the design experience established by various demonstrator projects. First, a demonstrator Multi-Chip Module (PPrD-MCM) was successfully built and tested (see [Pfe99/2] for details). The demonstrator Multi-Chip Module had a size of 15.9 cm^2 and it consisted of 9 dies. The MCM was designed with the same feature size (100 μm) as the PPrMCM and it was fabricated in the same laminated MCM-L process offered by Würth Elektronik. A Flip-Chip mount technique was investigated and cooling was improved by cutout areas in the layer structure to deal with 12.25 W power dissipation. The PPrD-MCM was tested as part of a modular Pre-Processor test system, where transmission tests with 800 MBd and readout tests have been performed. Compared to this MCM the PPrMCM will be less demanding in terms of power, temperature, and link speed and hence it can achieve an improved reliability.

Further developments toward the final PPrMCM where investigated. This 'intermediate' step between the demonstrator and the final PPrMCM was set-up to test the interplay of new components and to evaluate layout properties. The die versions of ADC, LVDS and Phos4 were mounted on a CMC card called ECMC (see [Ste00] for details).

Link tests at Birmingham, Heidelberg, and Mainz indicate low bit-error rates and acceptable link performance over 20 m long cables. If there might be a problem using LVDS chip sets in the Trigger one could of cause have the G-link option as a fallback solution implemented on the MCM. This was proved to be feasible on the PPrD-MCM. The implication would be to re-design the PPrMCM layout and to use cutout areas to deal with an increased power dissipation for the G-links. But seriously folks, why should a device, lower in power, lower in speed and lower in temperature be less reliable than G-links?

5 Characteristics

This section describes PPrMCM characteristics like mechanical-, timing-, and electrical characteristics.

5.1 Mechanical Characteristics

The physical dimensions of the PPrMCM are shown in Figure 5. It will be 20 mm wide and 70 mm long with clamps on each end to arrest it and allow a quick replacement if required. On each end a 60 pin SMD connector from SAMTEC (BSH-030-01-F-D-A) [Sam] connects it to the PPM motherboard. The chips are encapsulated with a lid in between the two SMD connectors. The lid will be glued with electrically conducting epoxy to the layer compound. It will act as an EMI-shielding device and it will be filled with a silicone gel to remove atmosphere and to protect the dice from moisture. The four layer compound will be glued electrically isolated to a 800 μm thick copper substrate. The substrate itself is not grounded, because it does not act as a shielding device. The fourth layer 'ground plane' is exclusively used for this purpose, which allows a well defined thickness to ensure steady impedance for the design of 100 Ohm LVDS micro strip-lines. On the backside of the substrate an 8 mm heat-sink is glued to it. The total height $D_{z,MCM}$ of the MCM will be 15 mm. See Table 3 for MCM dimensions. Due to the height of the connector header on the motherboard there will be a clearance of 2 mm between the motherboard and the lid. This allows small SMD components to be placed between, close to the connector pins, e.g. bypass-capacitors for power supply lines.

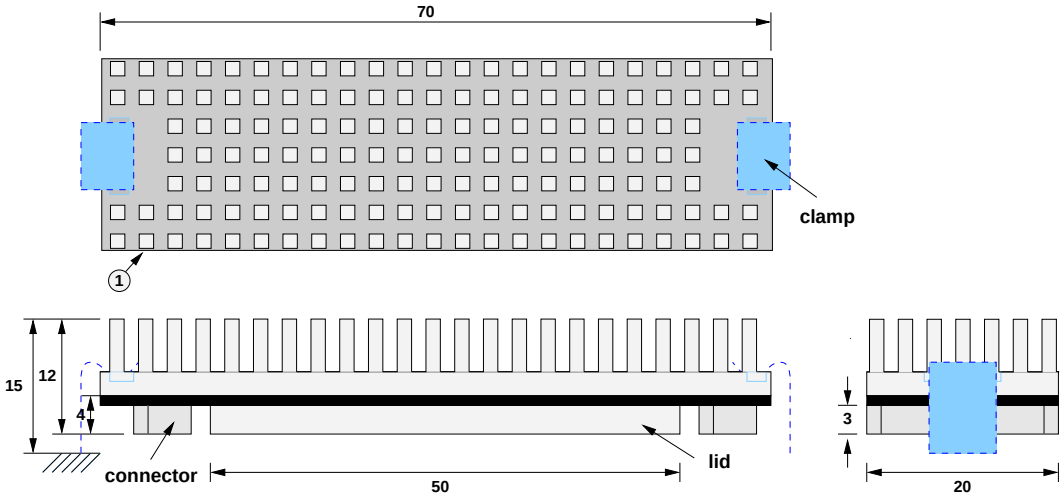


Figure 5: MCM physical dimensions

5.2 Timing Characteristics

The internal timing characteristic of the PPrMCM has to follow the requirements given by each chip specification. Figure 6 shows an internal PPrMCM timing diagram to illustrate set-up delay, output delay, and hold delay for each chip. Please refer to the individual chip specifications.

Due to the programmability of the ADC digitization strobe to the analog input signal, the ADC output data will be shifted accordingly. Hence, the PPrAsic must be programmed depending on the actual delay value used by the Phos4 chip to shift each ADC clock individually. The PPrAsic clock edge used to latch the ADC input data can be programmed channel-by-channel as well as the data bit from the external BCID. This synchronization is required to clock valid data into the LVDS Serializers. The LVDS Serializer clock will be selected to latch the PPrAsic data with the falling edge. This may be changed after detailed timing measurements at the PPrAsic have proven its hold delay $t_{hd,PPrAsic}$ (5 ns) and output delay $t_{od,PPrAsic}$ (7 ns). See also Table 3 for the switching characteristics.

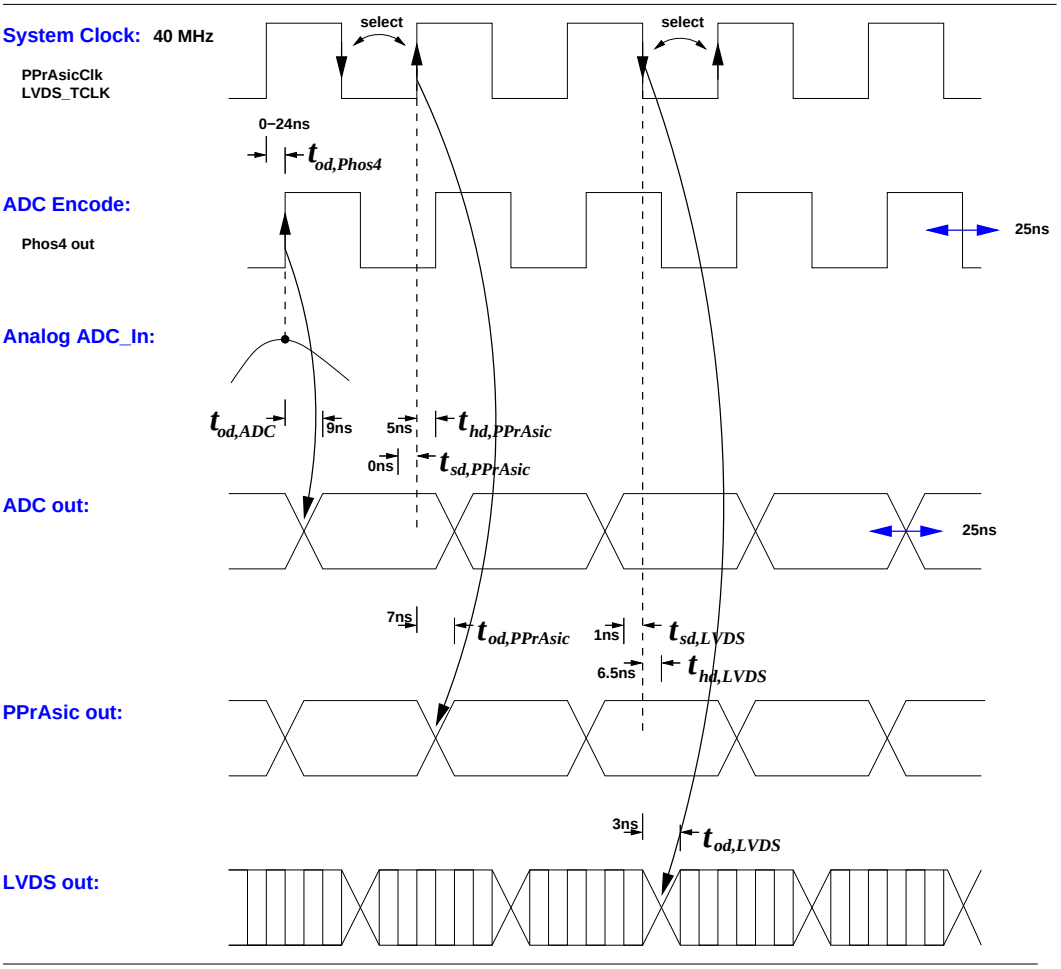


Figure 6: MCM timing diagrams

5.3 Electrical Characteristics

The PPrMCM requires 3.3 V and 5 V supply voltages. Only the ADCs require 5 V. The ADC output stage will have a 3.3 V supply to match the output logic levels to be CMOS compatible. The PPrAsic and the LVDS Serializers have CMOS compatible I/O logic levels except of the high-speed serial data outputs of the LVDS chips. Please refer to Section 4, where tests of the ADC and LVDS chips have been made. One of the major outcomes of these tests are, that no current limiting resistors are required on the MCM due to the reduced capacitive load of short chip connections.

6 Production Technique

The design process of the laminated multi-layer structure is based on an industrially-available production technique for high-density printed circuit boards. The process, which is offered by Würth Elektronik [Wue] is called TwinFlex. It is characterized by its use of plasma etched micro-vias, where plasma is used for ‘dry’ etching of the organic insulating Polyimide. Radicals and ions from a plasma react chemically with organic molecules accessible through open areas in a layer mask. Reaction products are removed instantaneously during the etching process, because of the reduced pressure and density of the plasma phase. Plasma etching enables precise via contacts between layers with a diameter of 100 μm.

Table 3:

Symbol	Parameter	Conditions	Typ	Units
Electrical Characteristics				
DVCC	digital power supply		3.3	V
DGND	digital ground		0	V
AVDD	analog power supply		5	V
AVCC	analog power supply		3.3	V
AGND	analog ground		0	V
P_{ADC}	power dissipation	DC	595	mW
$P_{PPrAsic}$	power dissipation	(to be defined)	1200	mW
P_{Phos4}	power dissipation	@40 MHz	200	mW
P_{LVDS}	power dissipation	@40 MHz	106	mW
P_{MCM}	power dissipation	(to be defined)	4100	mW
$R_{in,ADC}$	input impedance		250 ± 50	Ohm
$R_{in,MCM}$	input impedance		$300 \pm 1\%$	Ohm
R_{out}	output impedance	differential (DO- to DO+)	100	Ohm
R_{square}	trace resistance per square	$\rho = 1.724 \times 10^{-6} \Omega m$	0.069	Ohm
Analog Input				
V_{ADC}	analog input voltage range ADC		0-1	V
V_{tower}	trigger-tower voltage range		0-2.5	V
V_{under}	bipolar LAr under-shoot		20	%
V_{sat}	analog trigger-tower saturation voltage		3.0	V
DNL_{MCM}	differential non-linearity 10-bits	10.15 MHz sine, @40 MHz	± 0.2	LSB
INL_{MCM}	integral non-linearity 10-bits	10.15 MHz sine, @40 MHz	± 2	LSB
$ENOB_{MCM}$	effective number of bits	1.8 MHz sine, @40 MHz	8.9	ENOBs
$ENOB_{MCM}$	effective number of bits	9.9 MHz sine, @40 MHz	7.8	ENOBs
Serial LVDS Output				
V_{OH}	high level output voltage	I_{OH}=-9mA	2.93	V
V_{OL}	low level output voltage	I_{OL}=-9mA	2.0 - 5.0	V
SDR	serial data rate	@40 MHz	480	MBd
UDR	user data rate	@40 MHz	400	Mbps
Switching Characteristics				
$t_{od,Phos4}$	output delay Phos4	programmable delay	0-24	ns
$t_{od,ADC}$	output delay AD9042	+2 ticks	9	ns
$t_{od,PPrAsic}$	output delay PPrAsic	(+10 CP, +11 JP) ticks	7	ns
$t_{od,LVDS}$	output delay DS92LV1021	+2 ticks	3	ns
$t_{od,MCM}$	MCM output delay 3+10(11)+1	(+14 CP, +15 JP) ticks	3	ns
$t_{sd,LVDS}$	set-up delay DS92LV1021		1	ns
$t_{hd,LVDS}$	hold delay DS92LV1021		6.5	ns
$t_{sd,PPrAsic}$	set-up delay PPrAsic		0	ns
$t_{hd,PPrAsic}$	hold delay PPrAsic		5	ns
Mechanical Characteristics				
$D_{xy,MCM}$	MCM substrate dimension	heat-sink	70 x 20	mm^2
$D_{xy,PCB}$	MCM substrate dimension	incl. connector head	70 x 22	mm^2
$D_{z,MCM}$	total MCM height	inc. heat-sink	15	mm
N_{bond}	number of wire bonds	incl. test bonds	416	
N_{pin}	number of connector pins		120	
N_{die}	number of dice		9	
N_{layer}	number of routing layers	inc. ground plane	4	
Thermal Characteristics				
T_{MCM}	max. MCM temperature	forced convection 2m/s	55	°C
$MTBF_{MCM}$	Mean Time Between Failures	α_{die} = 1 ppm	111.111	h
R_{MCM}	reliability		92.4	%
$R_{jc,MCM}$	junction-to-case resistance		7.3	°/W

The number of vias, which may be etched at once is not limited and does not effect the complexity of a design and its price.

6.1 Layer Structure

The body of the PPrMCM is a combination of three flexible Polyimid foils laminated onto a rigid copper substrate to form four routing layers. Here a description of the layer cross-section is given in the way they are manufactured: an inner-foil of 50 μm thickness, also referred to as *core* foil, carries 18 μm copper plates on either side. Plasma etching is used for 'buried' via connections to adjacent layers and routing structures are formed in copper using conventional etching techniques. The core foil is surrounded by outer foils of 25 μm Polyimid, which are copper plated only on one side. Figure 7 shows a side view of each flexible foil prior to laminating. The actual contact through the core foil is accomplished with electroplated copper and after that, the routing structure are formed. The electroplating process increases the track thickness from 18 μm to 25 μm. The surface metallurgy of layer 1 will be gold plated with 100 nm to allow wire-bonding universally with 25 μm Al wires.

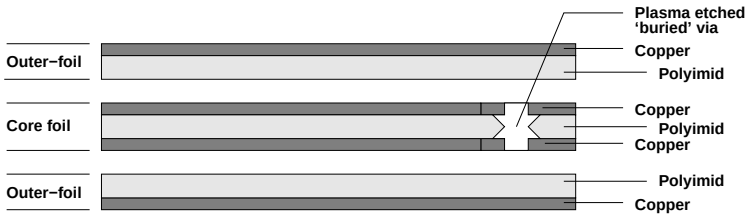


Figure 7: MCM layer definition

The application of adhesive accomplishes laminating. Then insulating Polyimid is removed by plasma etching above a 'target' pad to form a surface 'blind' micro-via contact for the 'outer' foils. After electroplating of copper, routing structures for the top and bottom layer are etched to form final connections. Figure 8 shows the final laminated and flexible part of the MCM after etching of outer routing structures.

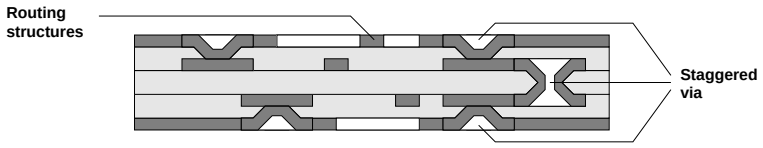


Figure 8: Cross-section with staggered via connection through all layers.

As shown in Figure 8, a combination of three vias is needed to accomplish a contact from the top to the bottom layer. A 'blind' surface micro-via connects layer 1 to layer 2, a 'buried' via connects layer 2 to layer 3, and finally a surface micro-via connects layer 3 to its destination on layer 4. Drilled vias are avoided, because they would need a more rigid and therefore thicker core foil, which would unnecessarily increase the total thermal resistance of the design.

The flexible multi-layer is finally glued onto an electrical isolated copper substrate (layer 4 acts as ground plane). Dice are connected to bond pads on the top layer of the cross-section using a standard ultrasonic wire-bond technique. Components such as capacitors and resistors are connected to the multi-layer structure using surface-mount technology. Advanced Flip-Chip mounting was investigated but is omitted for the final PPrMCM to reduce production complexity. Staggered vias are grouped as close as possible to form thermal vias, which improve heat conduction to the substrate underneath the ADCs. Due to the large number of semiconductor devices and MCMs at the Pre-Processor board level, a high-density SMD connector is used to permit a quick replacement of a broken MCM. If built-in tests have identified a broken MCM, it can be replaced without any soldering. The MCM is encapsulated with a lid and filled with a silicon gel as an elastic encapsulation material to absorb stress and to hermetically protect all components from atmosphere.

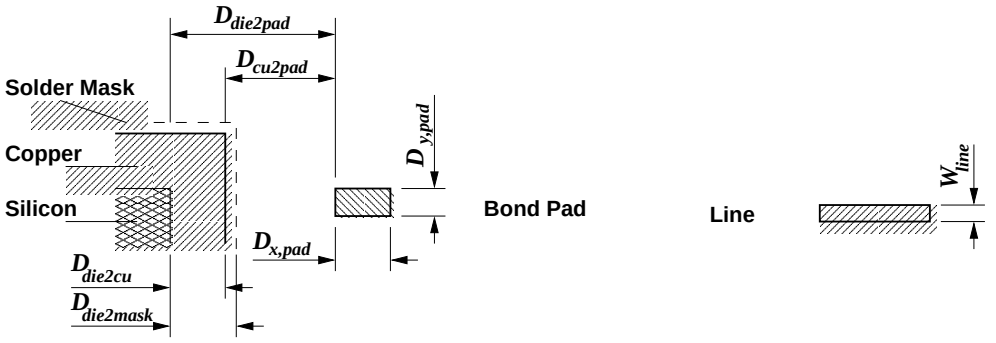


Figure 9: MCM design rules

6.2 Feature Size and Design Constraints

The TwinFlex MCM-L technology is offered by its manufacturer with no relation to any specific physical layout tool. The company does not support a software product with libraries containing information on materials, cross-section, or design constraints. The designer is free to choose a suitable layout tool, and he has to ensure that all process parameters and constraints given by the manufacturer are set up properly. The layout tool is then able to check the layout against given constraints automatically, which is referred to as Design Rule Check (DRC).

For the PPrMCM the physical layout tool APD (Advanced Package Designer, [Apd97]) was used. It is a layout system for creating and optimizing micro-electronic packages, such as MCMs or Single-Chip Modules (SCM). APD is part of the integrated software, which the Cadence company [Cad] sells for accomplishing the major physical layout tasks. APD can also be used together with other Cadence products, namely: Concept [Con96] for schematic capture, Thermax [The97] for thermal analysis, SigNoise [Sig97] for signal noise analysis, and EMC [Emc97] for checking of electro-magnetic interference rules. Following this product division, one can define constraints in each of these products, e.g. for the geometrical layout, for the maximum allowed module and component temperature, for the electrical signal integrity, and the electro-magnetic interference.

Table 4 describes the applied layout constraints as they were arranged in conjunction with Würth Elektronik for the PPrMCM. The layout constraints are illustrated in Figure 9. A characteristic number of 100 μm was chosen as the minimum allowed feature size. No line or shape of the layout is allowed to be smaller than this number. The etching technique can produce smaller routing structures of 80 μm, but 100 μm was used to lower the MCM price and to stay within a more conservative range for which the TwinFlex process has shown best results. The minimum feature size applies to the line space and width of copper tracks as well as to the solder-mask space and width. For the distance of lines and shapes to cutout regions and for the milling tool radius, a size of 500 μm was defined.

Via constraints are defined by a hole diameter, to form the contact to an adjacent layer, and the diameter of a surrounding contact and target pad. Table 4 lists their values for ‘buried’ micro-vias, and ‘blind’ micro-vias. These via types can be combined to form a staggered contact through all four signal layers. Apart from the definition of alternating materials, their thickness is important for both thermal and electrical characteristics. See Table 4 for the thickness of each cross-section layer.

7 Schematic

The PPrMCM schematic was created in Concept as front-end tool for the physical design entry. Concept is part of the Cadence design work frame. It can be used in combination with the simulation tool Analog Workbench (AWB) that Cadence provides for accomplishing mixed-signal simulations. All schematic pages are included in this document. The TOP page (Figure 10) was used as a top-level symbol in a mixed-signal simulation as described in Section 8.1. Page one

Table 4:

Symbol	Parameter	Conditions	Typ	Units
Geometrical Layout Characteristics				
W_{line}	line width	min feature size	100	μm
$D_{xy,pad}$	bond pad dimension	single width	300 x 150	μm^2
$D_{die2pad}$	distance silicon die edge to bond pad edge		750	μm
D_{cu2pad}	copper to bond pad edge		550	μm
D_{die2cu}	silicon die edge to copper overlap		200	μm
$D_{die2mask}$	silicon die edge to solder-mask cut-out		200	μm
$D_{cu2mill}$	copper to mcm boundary space (milling tool space)		500	μm
Via Characteristics				
	‘buried’ micro-via hole diameter		100	μm
	‘buried’ micro-via pad diameter		300	μm
	‘blind’ micro-via hole diameter		100	μm
	‘blind’ micro-via pad diameter		350	μm
Layer Characteristics				
	Surface metallurgy (Au)	thickness	100	nm
	Surface metallurgy (Ni)	thickness	5	μm
	Copper tracks	thickness	25	μm
	Outer Polyimid insulator	thickness	25	μm
	Epoxy glue between layers	thickness	10	nm
	Core Polyimid insulator	thickness	50	μm
	Epoxy glue to substrate	thickness	50	μm
	Copper substrate	thickness	800	μm
	Aluminium heatsink	thickness	8000	μm

(Figure 11) is the ADC part of the MCM, Page two (Figure 12) the PPrAsic and Phos4 schematic, page three (Figure 13) is the LVDS Serializer schematic and finally page four (Figure 14) shows the connector pin to signal allocation.

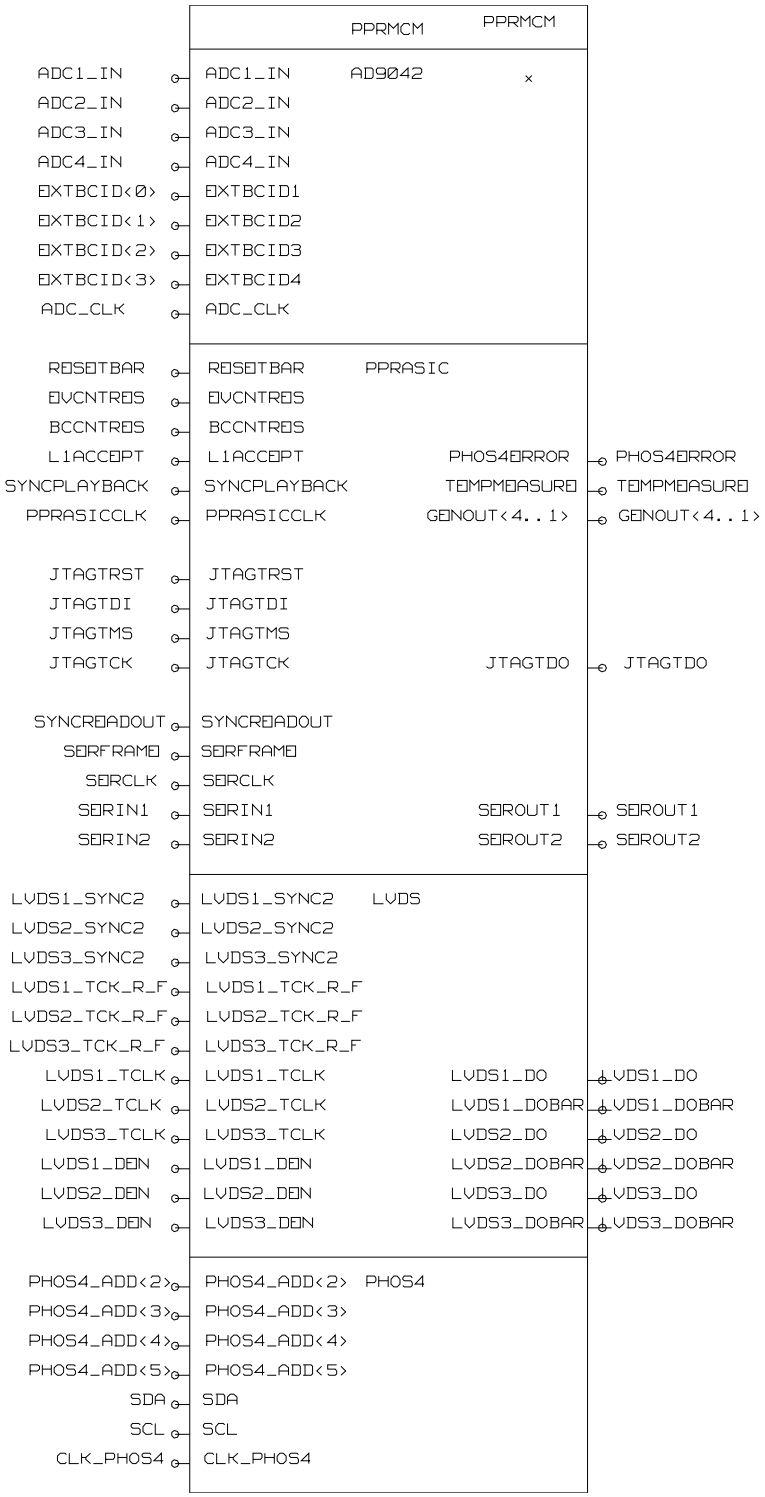


Figure 10: MCM schematic TOP

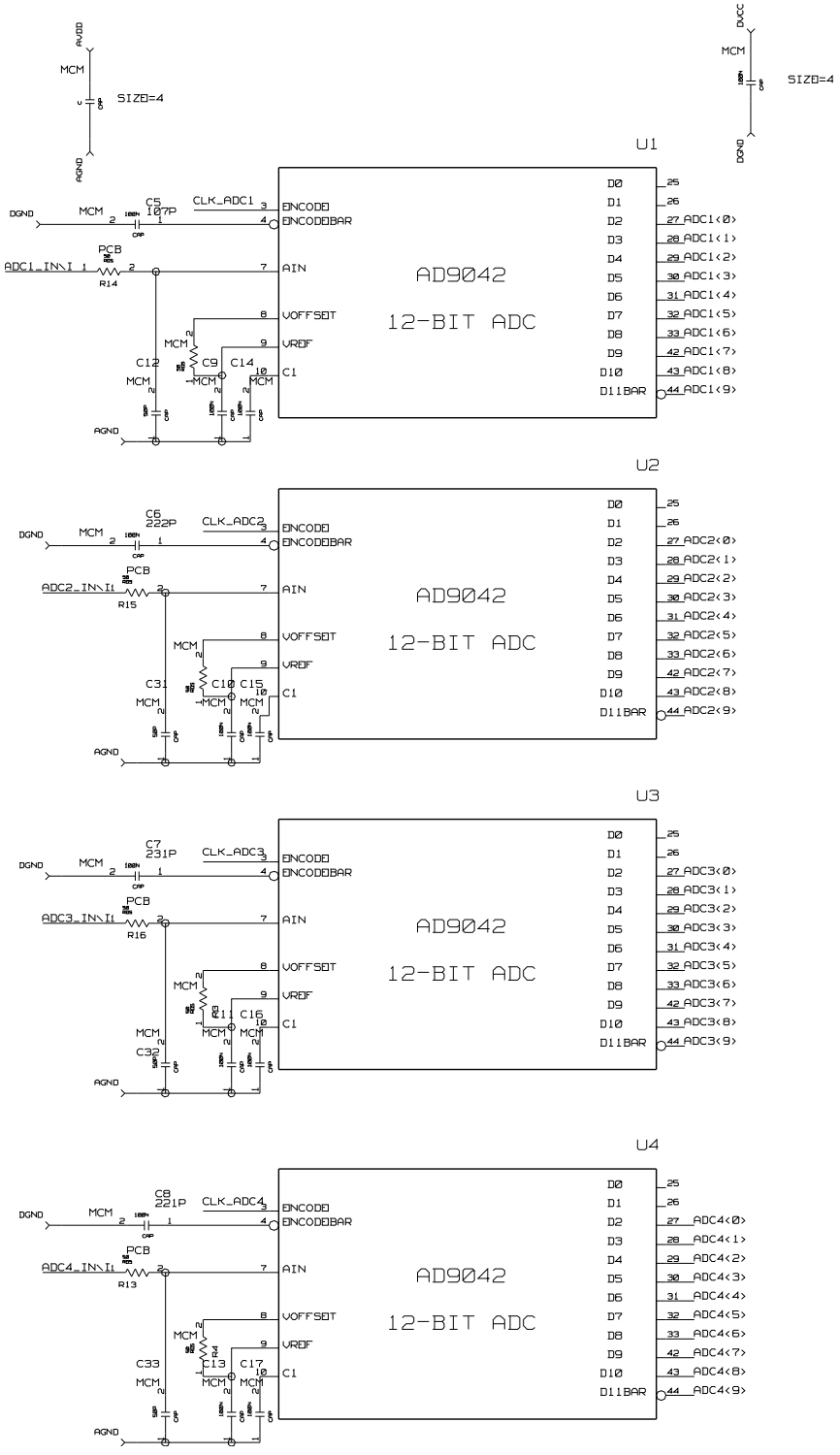


Figure 11: MCM schematic page 1

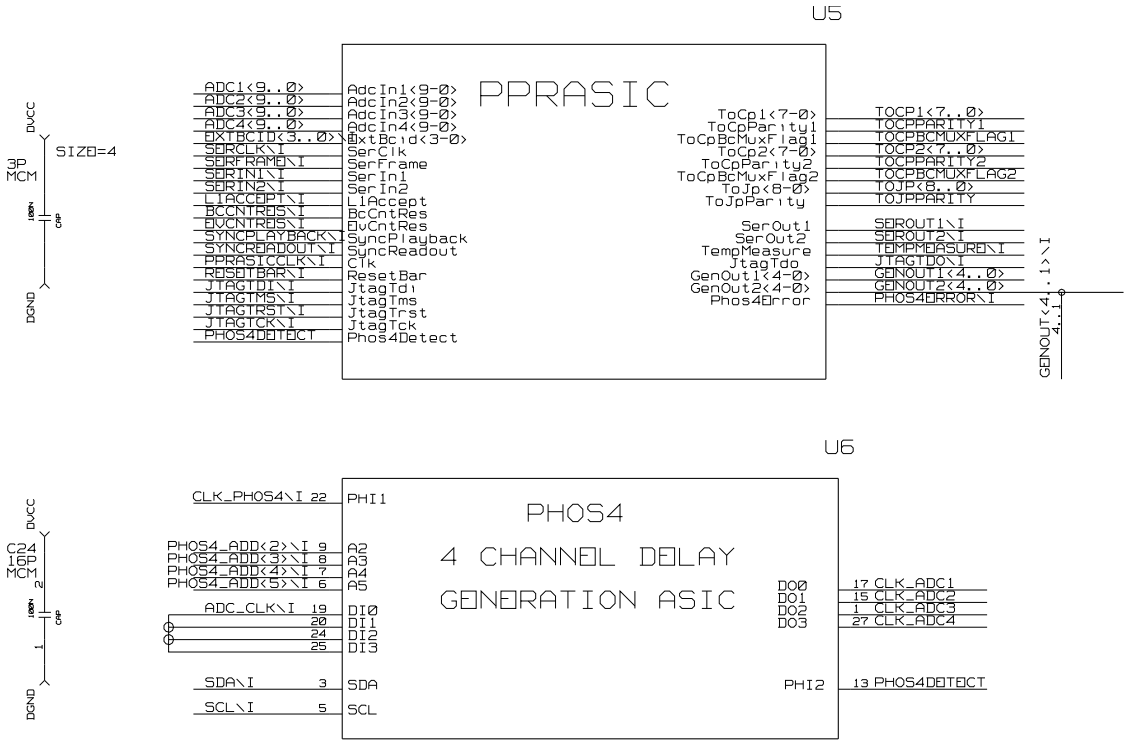


Figure 12: MCM schematic page 2

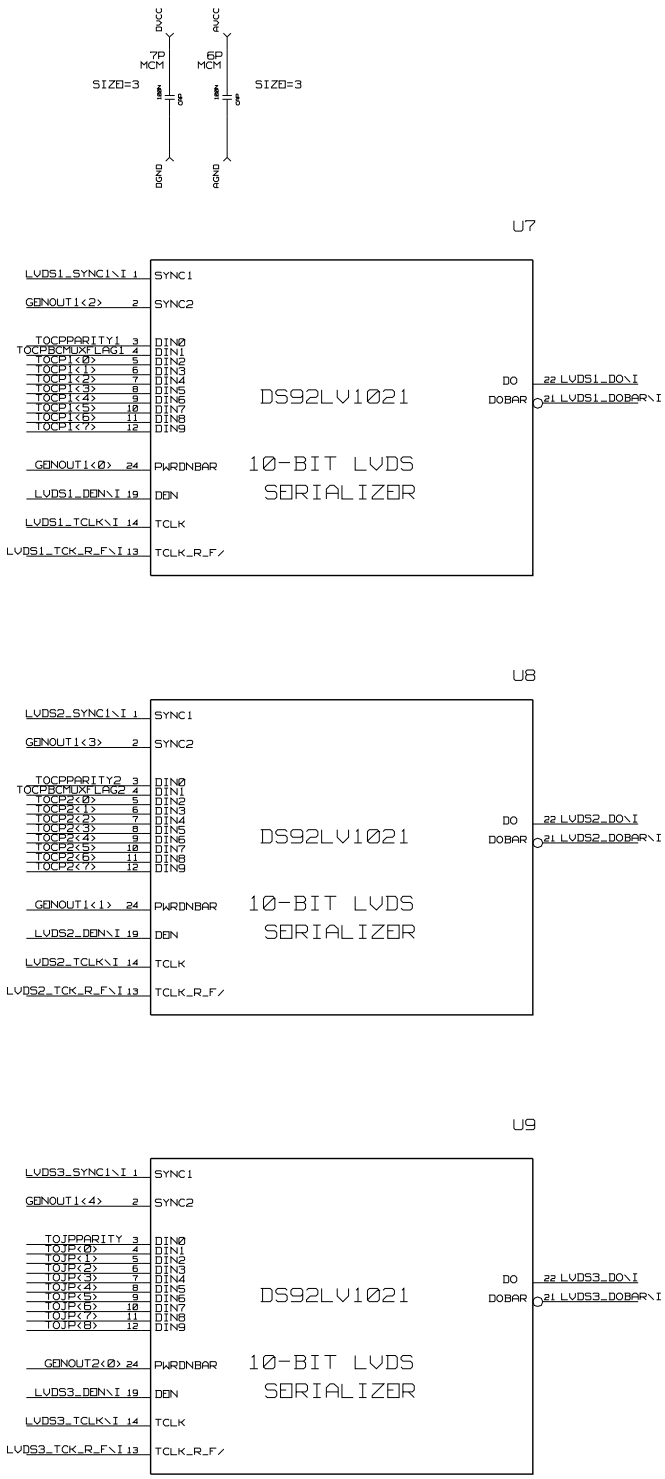


Figure 13: MCM schematic page 3

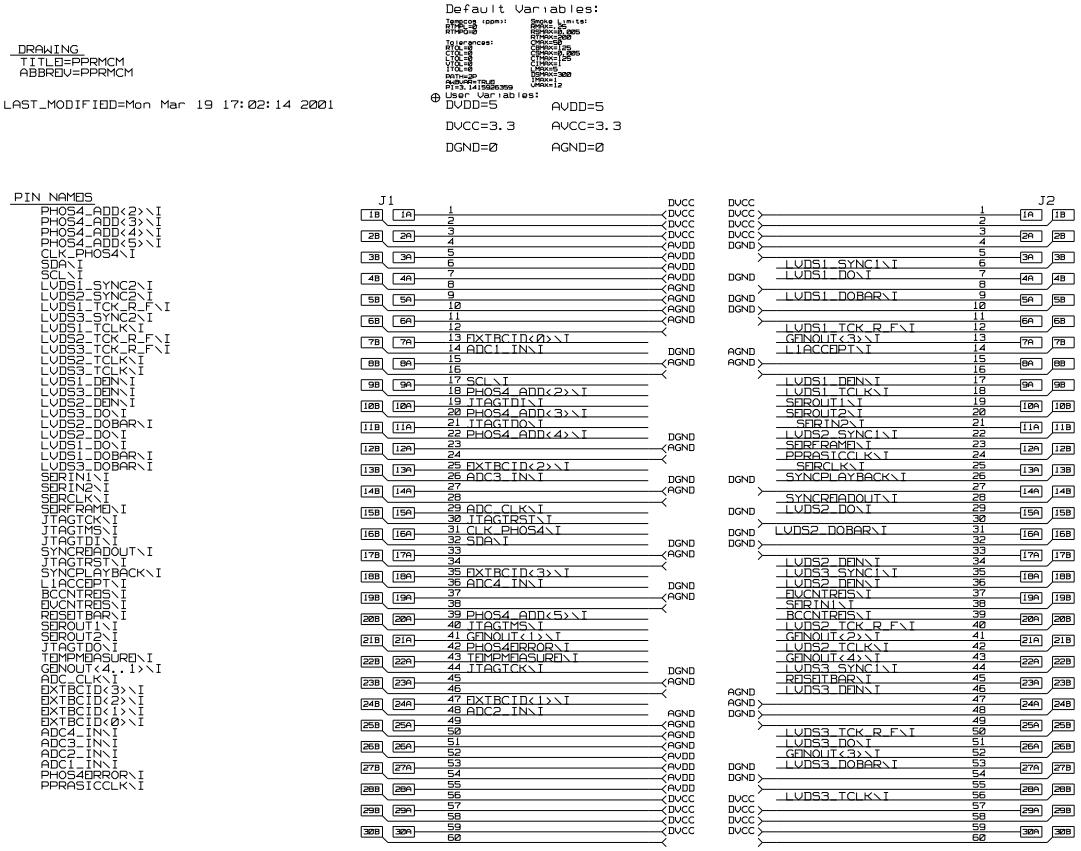


Figure 14: MCM schematic page 4

8 Simulations

Electrical and thermal simulations were of use during the design of the MCM. A circuit simulation was set-up and used to check for connectivity errors during the design. This simulation will also be used for the final MCM production test to generate digital and analog ‘test vectors’ as well as ‘expected vectors’ (see Section 12). The thermal simulation was of use for the temperature budget of the PPM.

8.1 Circuit Simulations

Figure 15 shows the scope of the mixed-signal simulation. Analog calorimeter input data to the Simulation were generated by a Pspice simulation of the LAr trigger tower electronic. Other analog stimulus data can be generated within the AWB simulation; like clock pulses, noise-, or time-jitter effects. This simulation was used to check set-up and hold times, ADC clock phase-adjustment using the Phos4. It can also be used to simulate the effect of e.g. variations of the ADC input resistance. ‘Basic’ simulation models for the ADC, Phos4, and LVDS were written in VerilogA. For the Pre-Processor Asic the actual Verilog code was used. This simulation is of importance to generate expected result vectors to be used in an automated production test required for such a complex mixed-signal device.

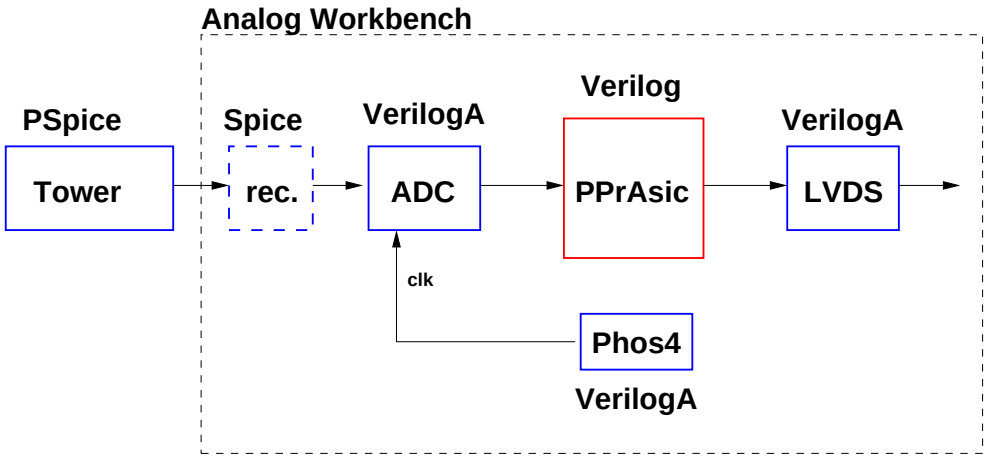


Figure 15: Mixed-signal simulation and test vector generation

8.2 Thermal Simulations

For analyzing the thermal characteristics of the demonstrator PPrMCM, the analysis tool Thermax [The97] was used. It is part of the Cadence product distribution [Cad] and it is integrated in the APD (Advanced Packaging Designer,[Apd97]). After a Thermax simulation is complete, one can view two- and three-dimensional maps that can be overlaid on the APD design.

For each die, material, size, and thermal resistance from the junction to the die attachment were defined and provided in a component library for simulation. Because of equal treatment of each component, the simulation cannot take special cooling approaches such as thermal vias of the cross-section into account. Hence, the simulation results for the MCM must be seen as a worst case system simulation to estimate maximum ratings, and to observe the thermal behaviour dependent on variation of boundary conditions. From thermal spread-sheet calculations the individual die cooling is improved by about 87 % by using thermal vias [Pfe99/2]. But, because of the loss of all routing area underneath a chip, such a cooling mechanism was only applied to the ADCs.

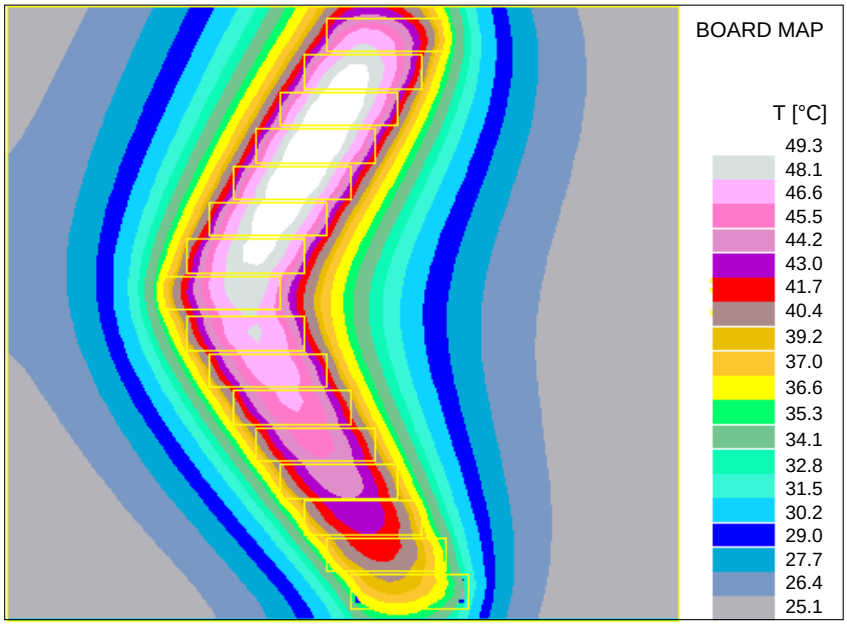


Figure 16: Temperature simulation for chevron-like MCM placment

Figure 16 shows the heated area of the Pre-Processor motherboard equiped with 16 PPrMCMs. The PCB is heated up from the initial temperature of 25 °C to the maximum of 49.3 °C. A fan is blowing vertically from the bottom to the top and the temperature map is overlaid on the PPM layout to identify the MCM positions. The temperature simulation has shown good results for a 'chevron-like' MCM placement. In addition, this placement separates analog signals from digital signals.

9 Layout

Figure 17 shows an overview picture of all MCM routing layers. One can see the copper shapes for the die attachment, SMD pads, bonding pads, and the top ground shielding. The chip location is, from left to the right: Phos4, ADCs, PPrAsic, and LVDS. Each connector has 60 pins. The left one carries only analog, power, and slow control signals whereas the right one carries digital, clock, and high-speed serial output signals. As a guide line, the following points have been considered during the layout:

- **Analog and digital parts:** Analog chips were separated from digital chips, and power and ground signals were kept separate. This applies also to the signal routing.
- **Component placement:** Optimum distance to other components, to achieve uniform heat distribution were considered. Extra space needed for component mounting technologies, e.g. wire-bonding and soldering were foreseen.
- **Signal routing:** Because of the high signal density, no auto routing tool was used. The layout is fully hand crafted, with two signal layers surrounded by the bottom ground plane and a top layer, consisting of shielding shapes, bonding pads, and SMD pads. One signal layer was mainly used for routing in x-direction and the other one for routing in y-direction.

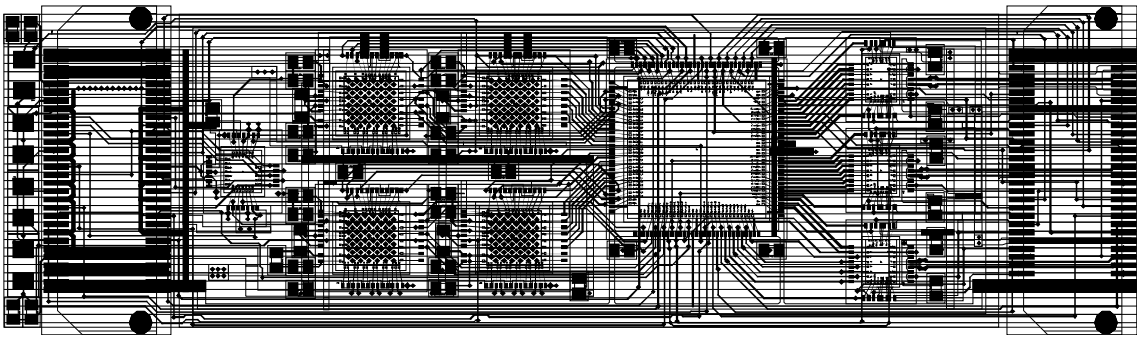


Figure 17: All MCM layers

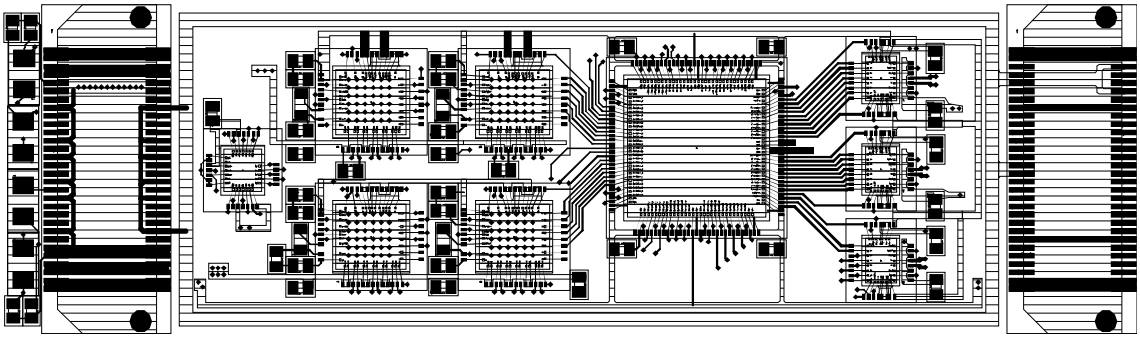


Figure 18: MCM layer 1

- **Track width:** Wider power tracks were used to limit the voltage drop on power rails. For a MCM copper routing layer a resistivity of $1.724{\cdot}10^{-6}\,\Omega\mathrm{m}$ and a thickness of 25 μm was taken to calculate the resistance per square R_{square} which is 0.069 $\Omega/square$. The resistance of any track with constant width w is equal to the number of rectangular squares with size $w \times w$ multiplied by R_{square}. For example, a typical power track is 350 μm wide, 1 cm long, and a current of 133 mA has a track resistance of 1.97 Ω and a voltage drop of 0.26 V.

- **Chip power supply:** Separate power tracks for each chip type were used. Those tracks were separately connected to the external power pins of the MCM package. The power pins will be connected together by external power connections. See Appendix B for the names of the decoupled power net names of each die.

- **Chip power blocking:** The power supply lines are blocked for each die using a bypass capacitor of 100 nF separate for the analog and digital supply lines. One for the Phos4, two for each ADC, four for the PPrAsic, two for each LVDS. See the MCM schematic in Section 7 showing the capacitors and their size property attached to indicate their multiplicity. You may also find their location on the layout view in Figure 18.

- **Clock distribution:** The clock distribution was done for each chip individually using short tracks. This ensures a uniform propagation delay for all clock signals.

- **Via placement:** A via can carry the same current as a copper track of 100 μm width. Hence, in wider power rails the number of vias was increased.

- **Via count:** The number of vias for the high-speed serial LVDS signals was reduced. A via, which connects adjacent layers of different impedance, can cause reflections affecting high-speed signals.

- **Bond-pad size:** The MCM has used a bond-pad size of 150 μm $\times$ 300 μm. This size is large enough for wire-bonding, even if one needs to probe at bonding pads during the MCM test or to place a second bonding wire.

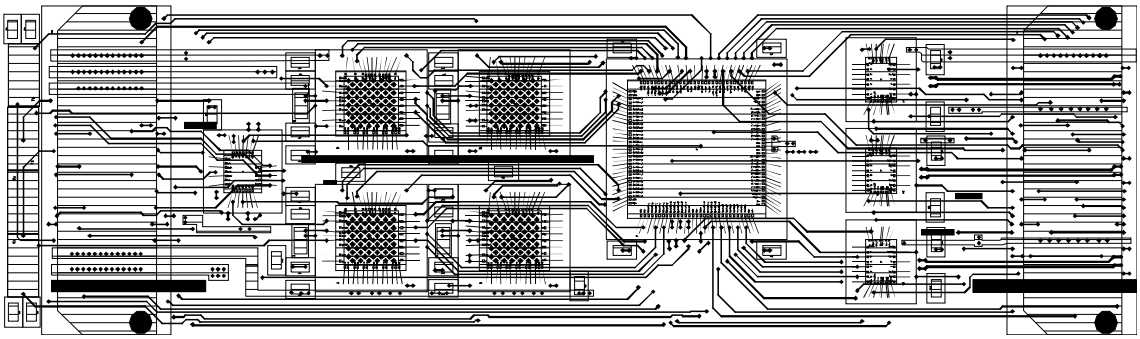


Figure 19: MCM layer 2

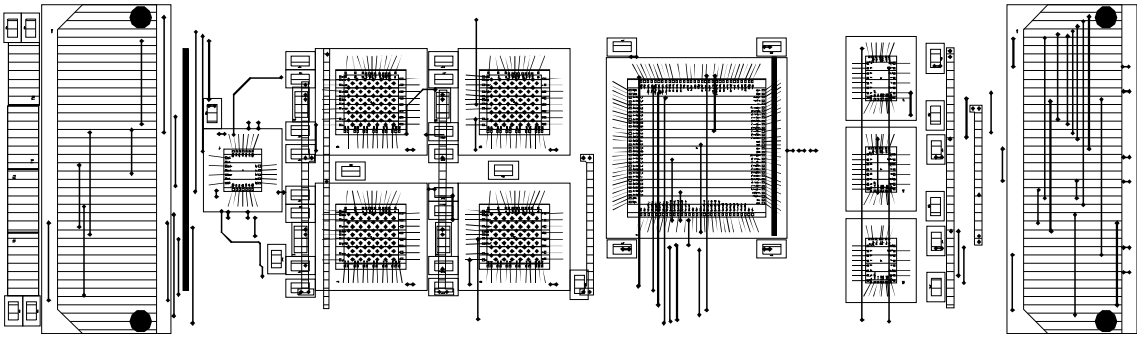


Figure 20: MCM layer 3

- **Test pads:** Test pads are placed on the top layer. During the MCM pre-test at Heidelberg, needle probes can then spy on signals which are otherwise buried in the layer cross-section. This is important during the MCM test, where each chip needs to be tested. See Section 12.
- **Thermal vias:** A thermal via is a kind of staggered via, which connects through the cross-section to provide good thermal conduction. Attention must be paid to chip mounting on thermal vias, because the silver glue needs to fill up all micro-via holes to remove air between chip and copper shape. When the MCM is heated up with air underneath, the attachment will pop up, which is often referred to as 'popcorn' effect. This will be avoided.
- **EMI shielding:** Layer four of the layer compound (Figure 17) is used as ground plane and electro-magnetic shielding layer. On the top layer, a cross-hatched ground shape surrounding bonding and SMD pads is used to improve the shielding further. This reduces the electro-magnetic influence of signals to each other and it stabilizes the ground potential. A cross-hatched shape is needed because drying moisture coming out of the cross-section can destroy the MCM.
- **Chip attachment:** Copper shapes beneath each die are required to connect the die substrate with its voltage potential.
- **Solder-mask:** A solder-mask is used to prevent short circuits during soldering of SMD components, and to protect bonding pads from the die attachment glue.

Individual routing layers are shown in Figure 18 for layer 1, in Figure 19 for layer 2, in Figure 20 for layer 3, and the common DGND ground plane on layer 4 is shown in Figure 21. On each plot the footprints of dice, SMD capacitors and SMD connectors are included.

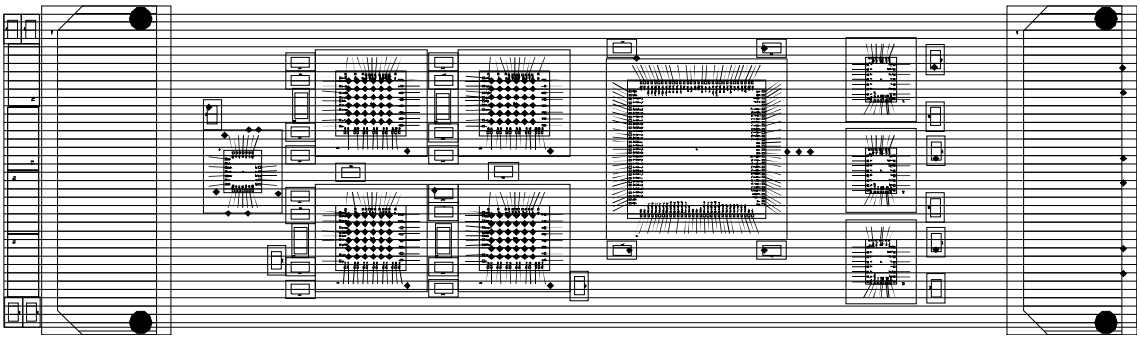


Figure 21: MCM layer 4

Table 5:

Parts	**Production #** (inc. yield)	**Running #**	**Spares** (plugged on)	**Spares** (preserved)	**Testing**	**Yield**	**Defect**
Yield and spare policy							
PPMs	143	128	0	13 (10 %)	2	100 %	0
PPrMCMs	2870	2048	240	572 (25 %)	10	75 %	957
MCM substrates	3866	3827				99 %	39
PPrASIC	6378	3827				60 %	2551
AD9042	17009	1530				90 %	1701
Phos4	4037	3827				95 %	210
LVDS	12757	1148				90 %	1276
Socket	7732	7654				99 %	78
Header	4623	4576				99 %	47
Lid	3866	3827				99 %	39
HASEC	3827						

10 Yield and Spare Policy

The Pre-Processor is of importance for the running of the ATLAS experiment, because all the Level-1 Calorimeter Trigger input data have to go through it. In case that the Pre-Processor needs to be repaired, a quick exchange of broken modules is required. Therefore, it is not desirable to have different types of modules implying a large set of different spare modules. Hence, all the Pre-Processor Modules and Multi-Chip Modules will be identical, having the same functionality.

System failures are often caused by a combination of temperature and vibration. Therefore, low temperature operation was one of the major objectives when designing the PPrMCM to improve the system reliability. The PPrMCM consisting of 9 dice, each having an assumed failure rate α of 1.0 part per million hours. The Mean Time Between Failures ($\mathrm{MTBF_{MCM}}$) is 111.111 hours. The probability of zero failures over one year is 92.4 % (see Equation 1). This makes it obvious that connectors for the Pre-Processor MCM are essential, because an exchange of a Pre-Processor Module as a whole in case of an MCM failure is of course not affordable in terms of spares and costs.

The PPrMCM reliability R is defined as:

$$R := e^{-\frac{t}{\mathrm{MTBF_{MCM}}}}, \quad \text{with} \quad \mathrm{MTBF_{MCM}} = \frac{1}{\sum_i \alpha_i(T)}. \tag{1}$$

11 Manufacturing

The development and design of the PPrMCM was done by the University of Heidelberg, whereas the final production of 2780 MCMs needs to be done in conjunction with external companies. The four layer MCM substrate including the 800 μm copper carrier will be done by Würth Elektronik [Wue]. The assembly of dice, SMD components, wire bonding, and encapsulation will be done by Hasec [Has]. Alternative manufacturers have been looked at, but the mentioned above satisfies our needs for cooperation, quality and prices. The lid and heat-sink including clips at each end will be provided by us.

The production starts with a pre-production of 64 MCMs to fully equip 4 PPMs. These PPMs will be part of the ATLAS Level-1 Calorimeter Trigger slice test and to act as a data source. Using the ATLAS terminology these modules will be named module-0 devices. Before this production can actually be started the MCM have to have a pre-test where errors in the design can be identified. As part of this pre-test a movable MCM test set-up will be developed, which is required to test the MCM at the manufacture site. The small volume pre-test will include 10 MCM. These modules will be build at the ASIC laboratory of the University of Heidelberg. This assembly procedure was already applied to the demonstrator MCM including ultrasonic wire bonding, chip attachment, and soldering. Encapsulation at this point will not be required.

The production sequence is linked with tests at various points, because it is not affordable in terms of yield and prices to just identify known good MCMs and to sort out defect devices after a whole batch was manufactured. The following list provides the sequence in which the PPrMCM will be manufactured and tested.

1 Production: Substrate layer compound

2 Test: Electrical test

3 Test: Bond test

4 Assembly: Silk-screen printing of solder paste

5 Assembly: Placement of SMD components

6 Assembly: SMD reflow soldering

7 Assembly: Chip attachment

8 Assembly: Ultrasonic wire-bonding

9 Test: Electrical connection test

10 Test: MCM test and repair procedure

11 Assembly: Encapsulation, lid and silicon gel

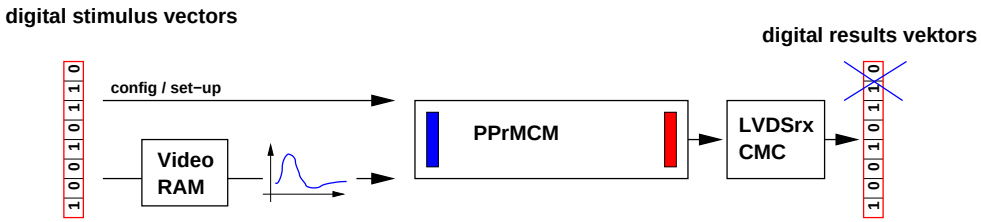
12 Test: Performance test (not part of the production)

Point 1 and 2 will take place at Würth Elektronik [Wue]. Point 3 to 11 will be done at Hasec [Has]. The final performance test and changes to the input RC-filter on the MCM will be done at Heidelberg. See Section 3.1 for the use of the ‘RC-balcony’. The first electrical test at Würth checks for manufacturing errors of the MCM substrate against the ‘netlist’ provided. This test will reject broken via connections and short-cuts. The second test located at Hasec can be seen as a quality inspection of the delivered substrates to ensure bondability on its surface metallurgy. After assembly of all components an electrical connection test checks for wire bond connections by measuring the input resistance of the chip I/O stages. Bad wire-bond connections can be double bonded because of an extra space that is foreseen on the MCM bond pad layout. Point 10 in the production sequence is probably the most important test, because the yield of the commercial ADC and LVDS dice will not be 100 %. We expect to have failures on chips and hence we need to replace them on the MCM. This test needs to be sufficient complex to find the error and to identify the defect chip. See the following Section

12 for a description of the planed test set-up. For the repair procedure two options exist. The first prefered option is to remove the dice by heating the copper shape on which they are glued to. This works fine for chip footprints without thermal vias. It is less suitable for the ADC chips where thermal vias provide a good thermal contact to the copper carrier. Essential heating the ADC means heating the MCM and this is not desirable. In this case, option two has been looked at, which just mounts a second die on top of a broken one. This is quite a common and easy way to exchange dice but maybe not very ‘esthetic’.

12 Testing

This section describes a test set-up which will be used as part of a repair procedure at Hasec and it will also be used for a final performance test at Heidelberg. A fast and automated test to say ‘yes’ or ‘no’ is required to identify chip and MCM failures. Hence, a mixed-signal simulation of the full MCM including the chip logic is required to generate expected results one can check for. Such a simulation was described in Section 8.1. Analog stimulus signals will be generate by an arbitrary function generator or by a more suitable video RAM, modified for that purpose. This device will than be programmed by digital data which was used during simulation. The ‘real’ output of the MCM can then be checked against what was simulated. The comparison can be executed in software (HDMC) or in programmable hardware. Because of its analog nature, the MCM test will have boundary criteria within the result should stay. For example, a parameter rejection can be done by ignoring the LSB end of a data word, see Figure 22.



1) assembly:	all MCMs at Hasec
2) functional test:	apply analog & digital stimulus for functional test e.g. power, bonding; using Jtag and "transparent" PPrAsic mode (10bit) −> first test of ADCs at 40 MHz & LVDS at 480 Mbit/s
3) repair:	exchange defect components at Hasec
4) encapsulation:	final encapsulation at Hasec
5) "full" test:	performance measurements, parameter rejections

Figure 22: MCM test sequence

The test hardware will be built from a modular VME based test system used to build a small-scale version of the Pre-Processor based on the existing prototype components. The basis of the modular Pre-Processor test system is a general-purpose motherboard on which several daughter-cards provide the special functionality. The test set-up may consist of two such motherboards where CMC cards can be plugged into card slots. One CMC card carries the PPrMCM and a second CMC card carries an LVDS receiver. See Figure 23. The test will be set-up and analyzed by the Hardware Diagnostic Monitor and Control software (HDMC) [Sch99].

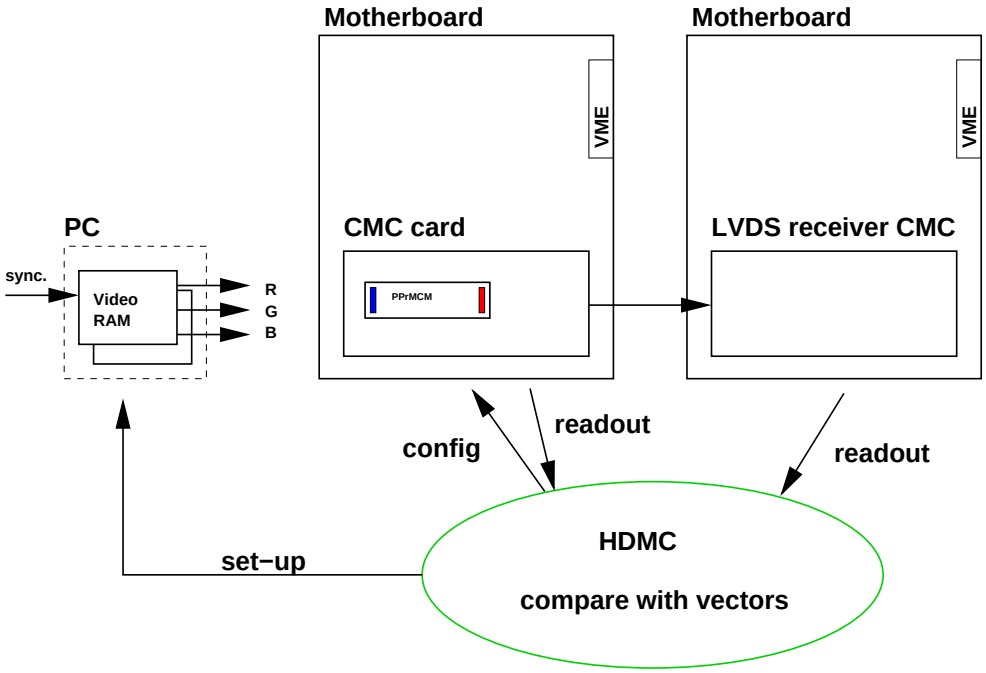


Figure 23: MCM test set-up at MCM assembler

A Chip Footprints

This appendix provides the chip footprints as used for the MCM layout. These footprints will also serve as bondig diagrams for the MCM assembly.

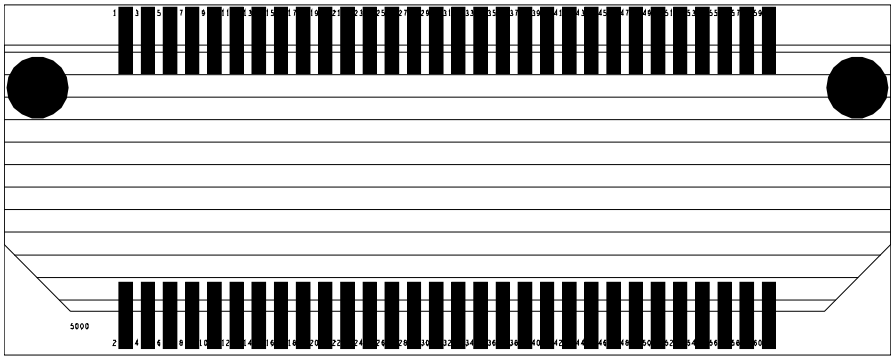


Figure 24: BTH030 footprint

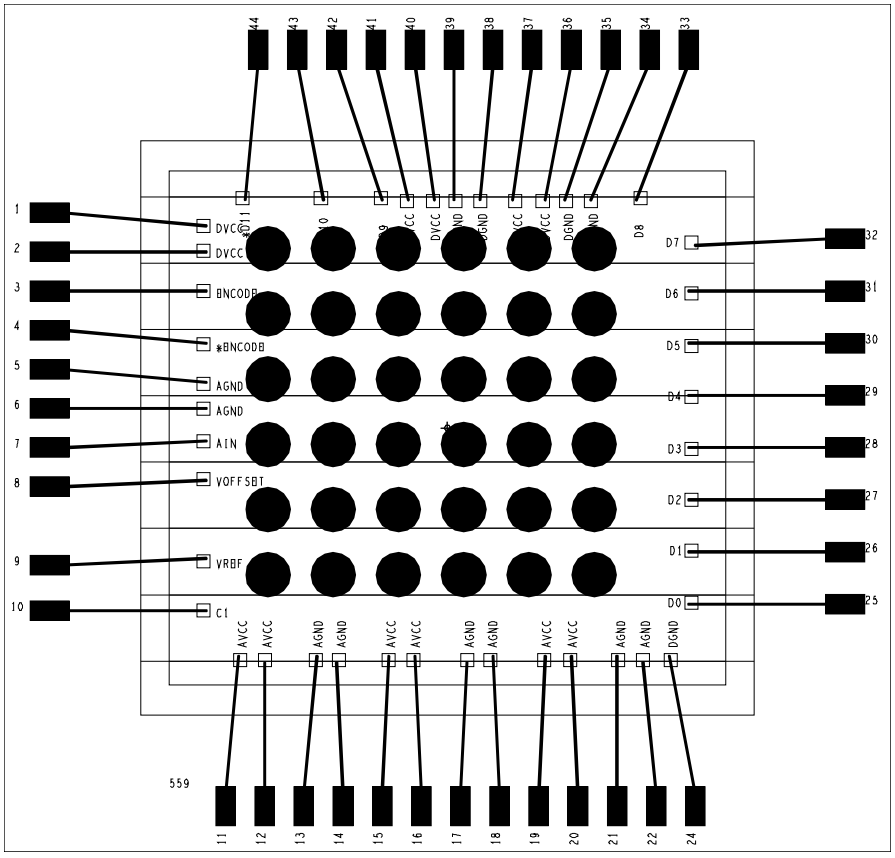


Figure 25: AD9042 footprint

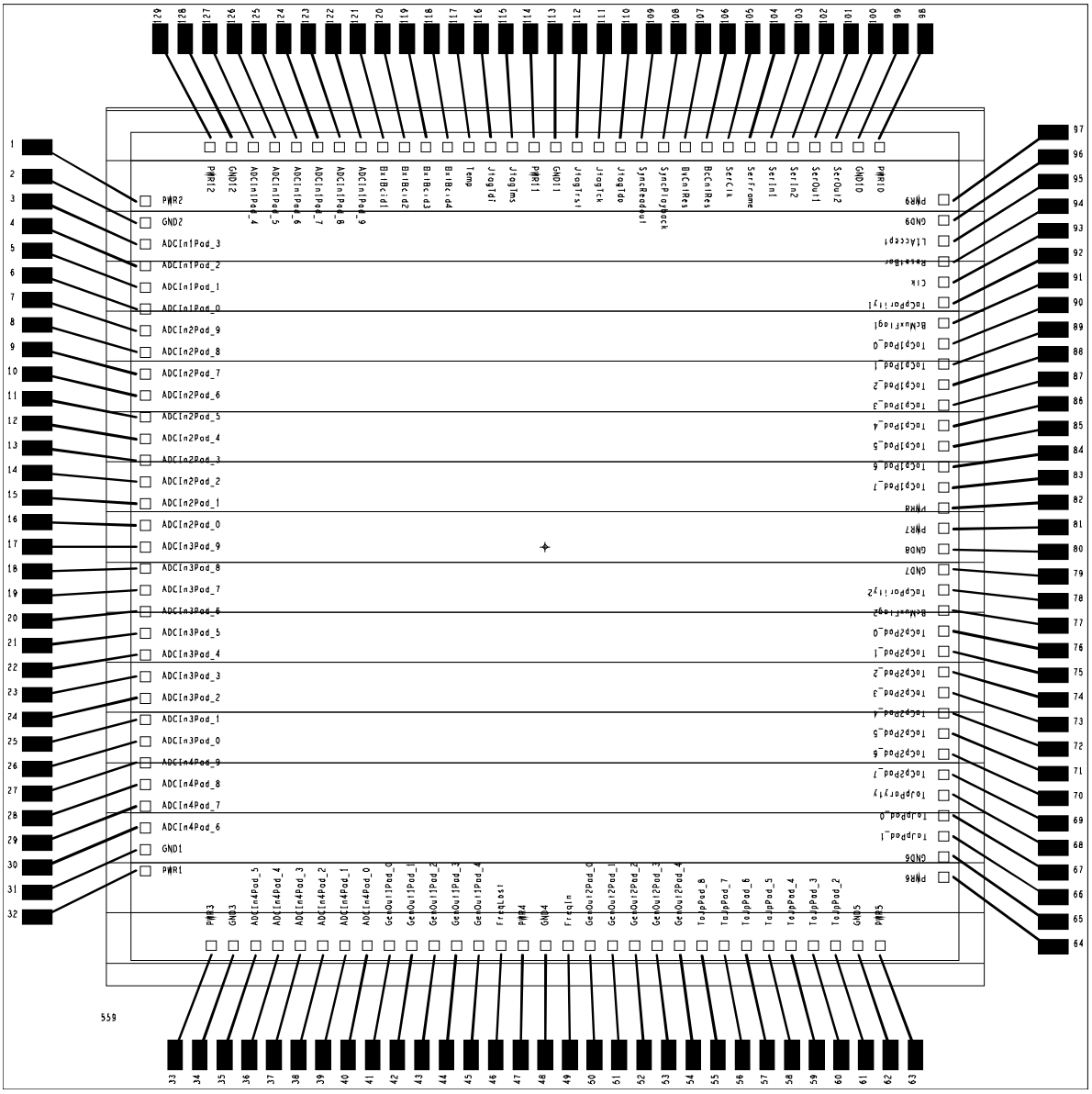


Figure 26: PPrAsic footprint

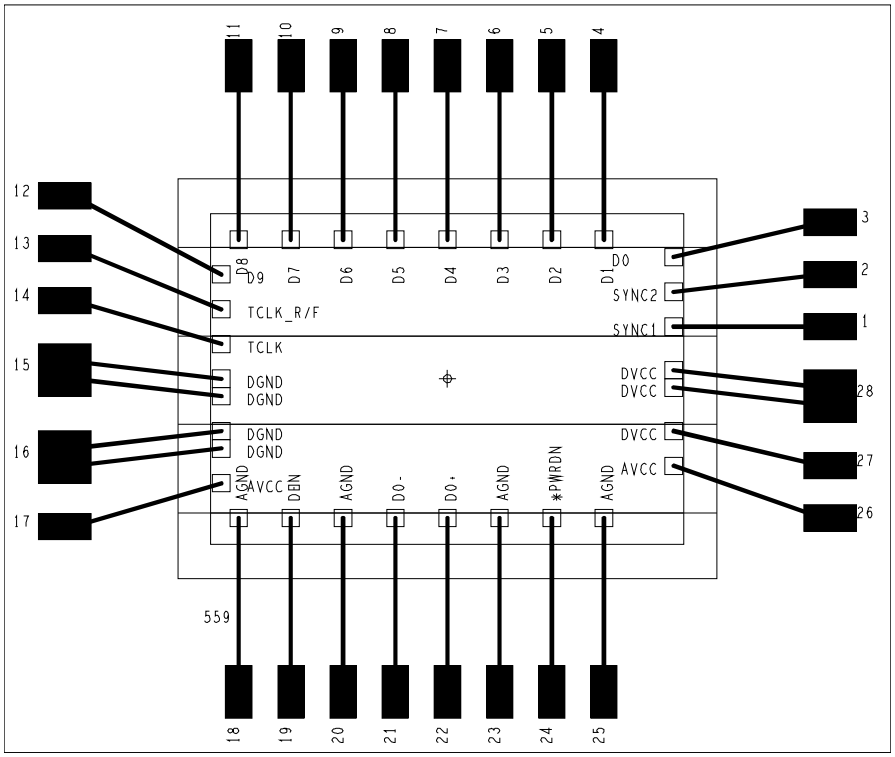


Figure 27: DS92LV1021 footprint

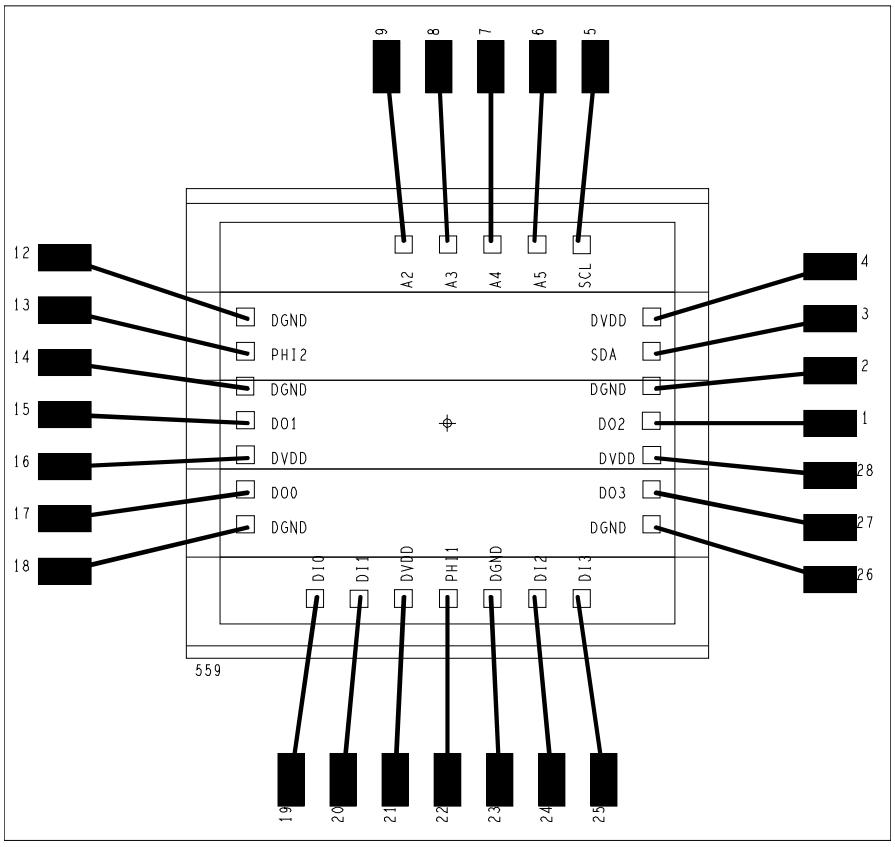


Figure 28: Phos4 footprint

B MCM Pin and Net Name Listings

This appendix provides pin and netname listings for each die in the MCM layout and the pin and netnames assigned to the SMD connectors.

Pin Number	Pin Name	APD Net Name
1	1A	DVCC
2	1B	DVCC
3	2A	DVCC
4	2B	DVCC
5	3A	AVDD
6	3B	AVDD
7	4A	AVDD
8	4B	AVDD
9	5A	AGND
10	5B	AGND
11	6A	AGND
12	6B	AGND
13	7A	EXTBCID<0>
14	7B	ADC1_IN
15	8A	DGND
16	8B	AGND
17	9A	SCL
18	9B	PHOS4_ADD<2>
19	10A	JTAGTDI
20	10B	PHOS4_ADD<3>
21	11A	JTAGTDO
22	11B	PHOS4_ADD<4>
23	12A	DGND
24	12B	AGND
25	13A	EXTBCID<2>
26	13B	ADC3_IN
27	14A	DGND
28	14B	AGND
29	15A	ADC_CLK
30	15B	JTAGTRST
31	16A	CLK_PHOS4
32	16B	SDA
33	17A	DGND
34	17B	AGND
35	18A	EXTBCID<3>
36	18B	ADC4_IN
37	19A	DGND
38	19B	AGND
39	20A	PHOS4_ADD<5>
40	20B	JTAGTMS

Table 6: Pin assignment of part J1 (BTH03001FDA)

Pin Number	Pin Name	APD Net Name
41	21A	GENOUT<1>
42	21B	PHOS4ERROR
43	22A	TEMPMEASURE
44	22B	JTAGTCK
45	23A	DGND
46	23B	AGND
47	24A	EXTBCID<1>
48	24B	ADC2_IN
49	25A	AGND
50	25B	AGND
51	26A	AGND
52	26B	AGND
53	27A	AVDD
54	27B	AVDD
55	28A	AVDD
56	28B	AVDD
57	29A	DVCC
58	29B	DVCC
59	30A	DVCC
60	30B	DVCC

Table 7: Pin assignment of part J1 (BTH03001FDA)

Pin Number	Pin Name	APD Net Name
1	1A	DVCC
2	1B	DVCC
3	2A	DVCC
4	2B	DVCC
5	3A	DGND
6	3B	LVDS1_SYNC1
7	4A	LVDS1_DO
8	4B	DGND
9	5A	LVDS1_DOBAR
10	5B	DGND
11	6A	DGND
12	6B	LVDS1_TCK_R_F
13	7A	GENOUT<3>
14	7B	L1ACCEPT
15	8A	AGND
16	8B	AGND
17	9A	LVDS1_DEN
18	9B	LVDS1_TCLK
19	10A	SEROUT1
20	10B	SEROUT2
21	11A	SERIN2
22	11B	LVDS2_SYNC1
23	12A	SERFRAME
24	12B	PPRASICCLK
25	13A	SERCLK
26	13B	SYNCPLAYBACK
27	14A	DGND
28	14B	SYNCREADOUT
29	15A	LVDS2_DO
30	15B	DGND
31	16A	LVDS2_DOBAR
32	16B	DGND
33	17A	DGND
34	17B	LVDS2_DEN
35	18A	LVDS3_SYNC1
36	18B	LVDS2_DEN
37	19A	EVCNTRES
38	19B	SERIN1
39	20A	BCCNTRES
40	20B	LVDS2_TCK_R_F

Table 8: Pin assignment of part J2 (BTH03001FDA)

Pin Number	Pin Name	APD Net Name
41	21A	GENOUT<2>
42	21B	LVDS2_TCLK
43	22A	GENOUT<4>
44	22B	LVDS3_SYNC1
45	23A	RESETBAR
46	23B	LVDS3_DEN
47	24A	AGND
48	24B	AGND
49	25A	DGND
50	25B	LVDS3_TCK_R_F
51	26A	LVDS3_DO
52	26B	GENOUT<3>
53	27A	LVDS3_DOBAR
54	27B	DGND
55	28A	DGND
56	28B	LVDS3_TCLK
57	29A	DVCC
58	29B	DVCC
59	30A	DVCC
60	30B	DVCC

Table 9: Pin assignment of part J2 (BTH03001FDA)

Pin Number	Pin Name	APD Net Name
3	ENCODE	CLK_ADC1
4	ENCODEBAR	Dummy Net
7	AIN	Dummy Net
8	VOFFSET	Dummy Net
9	VREF	Dummy Net
10	C1	Dummy Net
25	D0	NC
26	D1	NC
27	D2	ADC1<0>
28	D3	ADC1<1>
29	D4	ADC1<2>
30	D5	ADC1<3>
31	D6	ADC1<4>
32	D7	ADC1<5>
33	D8	ADC1<6>
42	D9	ADC1<7>
43	D10	ADC1<8>
44	D11BAR	ADC1<9>
11,12,15,16,19,20		AVDD
1,2,36,37,40,41		DVCC
5,6,13,14,17,18,21,22		AGND
24,34,35,38,39		DGND

Table 10: Pin assignment of part U1 (AD9042)

Pin Number	Pin Name	APD Net Name
3	ENCODE	CLK_ADC2
4	ENCODEBAR	Dummy Net
7	AIN	Dummy Net
8	VOFFSET	Dummy Net
9	VREF	Dummy Net
10	C1	Dummy Net
25	D0	NC
26	D1	NC
27	D2	ADC2<0>
28	D3	ADC2<1>
29	D4	ADC2<2>
30	D5	ADC2<3>
31	D6	ADC2<4>
32	D7	ADC2<5>
33	D8	ADC2<6>
42	D9	ADC2<7>
43	D10	ADC2<8>
44	D11BAR	ADC2<9>
11,12,15,16,19,20		AVDD
1,2,36,37,40,41		DVCC
5,6,13,14,17,18,21,22		AGND
24,34,35,38,39		DGND

Table 11: Pin assignment of part U2 (AD9042)

Pin Number	Pin Name	APD Net Name
3	ENCODE	CLK_ADC3
4	ENCODEBAR	Dummy Net
7	AIN	Dummy Net
8	VOFFSET	Dummy Net
9	VREF	Dummy Net
10	C1	Dummy Net
25	D0	NC
26	D1	NC
27	D2	ADC3<0>
28	D3	ADC3<1>
29	D4	ADC3<2>
30	D5	ADC3<3>
31	D6	ADC3<4>
32	D7	ADC3<5>
33	D8	ADC3<6>
42	D9	ADC3<7>
43	D10	ADC3<8>
44	D11BAR	ADC3<9>
11,12,15,16,19,20		AVDD
1,2,36,37,40,41		DVCC
5,6,13,14,17,18,21,22		AGND
24,34,35,38,39		DGND

Table 12: Pin assignment of part U3 (AD9042)

Pin Number	Pin Name	APD Net Name
3	ENCODE	CLK_ADC4
4	ENCODEBAR	Dummy Net
7	AIN	Dummy Net
8	VOFFSET	Dummy Net
9	VREF	Dummy Net
10	C1	Dummy Net
25	D0	NC
26	D1	NC
27	D2	ADC4<0>
28	D3	ADC4<1>
29	D4	ADC4<2>
30	D5	ADC4<3>
31	D6	ADC4<4>
32	D7	ADC4<5>
33	D8	ADC4<6>
42	D9	ADC4<7>
43	D10	ADC4<8>
44	D11BAR	ADC4<9>
11,12,15,16,19,20		AVDD
1,2,36,37,40,41		DVCC
5,6,13,14,17,18,21,22		AGND
24,34,35,38,39		DGND

Table 13: Pin assignment of part U4 (AD9042)

Pin Number	Pin Name	APD Net Name
3	ADCIN1<3>	ADC1<3>
4	ADCIN1<2>	ADC1<2>
5	ADCIN1<1>	ADC1<1>
6	ADCIN1<0>	ADC1<0>
7	ADCIN2<9>	ADC2<9>
8	ADCIN2<8>	ADC2<8>
9	ADCIN2<7>	ADC2<7>
10	ADCIN2<6>	ADC2<6>
11	ADCIN2<5>	ADC2<5>
12	ADCIN2<4>	ADC2<4>
13	ADCIN2<3>	ADC2<3>
14	ADCIN2<2>	ADC2<2>
15	ADCIN2<1>	ADC2<1>
16	ADCIN2<0>	ADC2<0>
17	ADCIN3<9>	ADC3<9>
18	ADCIN3<8>	ADC3<8>
19	ADCIN3<7>	ADC3<7>
20	ADCIN3<6>	ADC3<6>
21	ADCIN3<5>	ADC3<5>
22	ADCIN3<4>	ADC3<4>
23	ADCIN3<3>	ADC3<3>
24	ADCIN3<2>	ADC3<2>
25	ADCIN3<1>	ADC3<1>
26	ADCIN3<0>	ADC3<0>
27	ADCIN4<9>	ADC4<9>
28	ADCIN4<8>	ADC4<8>
29	ADCIN4<7>	ADC4<7>
30	ADCIN4<6>	ADC4<6>
35	ADCIN4<5>	ADC4<5>
36	ADCIN4<4>	ADC4<4>
37	ADCIN4<3>	ADC4<3>
38	ADCIN4<2>	ADC4<2>
39	ADCIN4<1>	ADC4<1>
40	ADCIN4<0>	ADC4<0>
41	GENOUT1<0>	GENOUT1<0>
42	GENOUT1<1>	GENOUT1<1>
43	GENOUT1<2>	GENOUT1<2>
44	GENOUT1<3>	GENOUT1<3>
45	GENOUT1<4>	GENOUT1<4>
46	PHOS4ERROR	PHOS4ERROR
1,32,33,47,63,64,81,82,97,98,114,129		DVCC
2,31,34,48,62,65,79,80,96,99,113,128		DGND

Table 14: Pin assignment of part U5 (PPRASIC)

Pin Number	Pin Name	APD Net Name
49	PHOS4DETECT	PHOS4DETECT
50	GENOUT2<0>	GENOUT2<0>
51	GENOUT2<1>	GENOUT<1>
52	GENOUT2<2>	GENOUT<2>
53	GENOUT2<3>	GENOUT<3>
54	GENOUT2<4>	GENOUT<4>
55	TOJP<8>	TOJP<8>
56	TOJP<7>	TOJP<7>
57	TOJP<6>	TOJP<6>
58	TOJP<5>	TOJP<5>
59	TOJP<4>	TOJP<4>
60	TOJP<3>	TOJP<3>
61	TOJP<2>	TOJP<2>
66	TOJP<1>	TOJP<1>
67	TOJP<0>	TOJP<0>
68	TOJPPARITY	TOJPPARITY
69	TOCP2<7>	TOCP2<7>
70	TOCP2<6>	TOCP2<6>
71	TOCP2<5>	TOCP2<5>
72	TOCP2<4>	TOCP2<4>
73	TOCP2<3>	TOCP2<3>
74	TOCP2<2>	TOCP2<2>
75	TOCP2<1>	TOCP2<1>
76	TOCP2<0>	TOCP2<0>
77	TOCPBCMUXFLAG2	TOCPBCMUXFLAG2
78	TOCPPARITY2	TOCPPARITY2
83	TOCP1<7>	TOCP1<7>
84	TOCP1<6>	TOCP1<6>
85	TOCP1<5>	TOCP1<5>
86	TOCP1<4>	TOCP1<4>
87	TOCP1<3>	TOCP1<3>
88	TOCP1<2>	TOCP1<2>
89	TOCP1<1>	TOCP1<1>
90	TOCP1<0>	TOCP1<0>
91	TOCPBCMUXFLAG1	TOCPBCMUXFLAG1
92	TOCPPARITY1	TOCPPARITY1
93	CLK	PPRASICCLK
94	RESETBAR	RESETBAR
95	L1ACCEPT	L1ACCEPT
100	SEROUT2	SEROUT2
1,32,33,47,63,64,81,82,97,98,114,129		DVCC
2,31,34,48,62,65,79,80,96,99,113,128		DGND

Table 15: Pin assignment of part U5 (PPRASIC)

Pin Number	Pin Name	APD Net Name
101	SEROUT1	SEROUT1
102	SERIN2	SERIN2
103	SERIN1	SERIN1
104	SERFRAME	SERFRAME
105	SERCLK	SERCLK
106	BCCNTRES	BCCNTRES
107	EVCNTRES	EVCNTRES
108	SYNCPLAYBACK	SYNCPLAYBACK
109	SYNCREADOUT	SYNCREADOUT
110	JTAGTDO	JTAGTDO
111	JTAGTCK	JTAGTCK
112	JTAGTRST	JTAGTRST
115	JTAGTMS	JTAGTMS
116	JTAGTDI	JTAGTDI
117	TEMPMEASURE	TEMPMEASURE
118	EXTBCID<3>	EXTBCID<3>
119	EXTBCID<2>	EXTBCID<2>
120	EXTBCID<1>	EXTBCID<1>
121	EXTBCID<0>	EXTBCID<0>
122	ADCIN1<9>	ADC1<9>
123	ADCIN1<8>	ADC1<8>
124	ADCIN1<7>	ADC1<7>
125	ADCIN1<6>	ADC1<6>
126	ADCIN1<5>	ADC1<5>
127	ADCIN1<4>	ADC1<4>
1,32,33,47,63,64,81,82,97,98,114,129		DVCC
2,31,34,48,62,65,79,80,96,99,113,128		DGND

Table 16: Pin assignment of part U5 (PPRASIC)

Pin Number	Pin Name	APD Net Name
1	DO2	CLK_ADC3
3	SDA	SDA
5	SCL	SCL
6	A5	PHOS4_ADD<5>
7	A4	PHOS4_ADD<4>
8	A3	PHOS4_ADD<3>
9	A2	PHOS4_ADD<2>
13	PHI2	PHOS4DETECT
15	DO1	CLK_ADC2
17	DO0	CLK_ADC1
19	DI0	ADC_CLK
20	DI1	ADC_CLK
22	PHI1	CLK_PHOS4
24	DI2	ADC_CLK
25	DI3	ADC_CLK
27	DO3	CLK_ADC4
4,16,21,28		DVCC
2,12,14,18,23,26		DGND

Table 17: Pin assignment of part U6 (PHOS4)

Pin Number	Pin Name	APD Net Name
1	SYNC1	LVDS1_SYNC1
2	SYNC2	GENOUT1<2>
3	DIN0	TOCPPARITY1
4	DIN1	TOCPBCMUXFLAG1
5	DIN2	TOCP1<0>
6	DIN3	TOCP1<1>
7	DIN4	TOCP1<2>
8	DIN5	TOCP1<3>
9	DIN6	TOCP1<4>
10	DIN7	TOCP1<5>
11	DIN8	TOCP1<6>
12	DIN9	TOCP1<7>
13	TCLK_R_F	LVDS1_TCK_R_F
14	TCLK	LVDS1_TCLK
19	DEN	LVDS1_DEN
21	DOBAR	LVDS1_DOBAR
22	DO	LVDS1_DO
24	PWRDNBAR	GENOUT1<0>
18,20,23,25		AGND
15,16		DGND
17,26		AVCC
27,28		DVCC

Table 18: Pin assignment of part U7 (DS92LV1021)

Pin Number	Pin Name	APD Net Name
1	SYNC1	LVDS2_SYNC1
2	SYNC2	GENOUT1<3>
3	DIN0	TOCPPARITY2
4	DIN1	TOCPBCMUXFLAG2
5	DIN2	TOCP2<0>
6	DIN3	TOCP2<1>
7	DIN4	TOCP2<2>
8	DIN5	TOCP2<3>
9	DIN6	TOCP2<4>
10	DIN7	TOCP2<5>
11	DIN8	TOCP2<6>
12	DIN9	TOCP2<7>
13	TCLK_R_F	LVDS2_TCK_R_F
14	TCLK	LVDS2_TCLK
19	DEN	LVDS2_DEN
21	DOBAR	LVDS2_DOBAR
22	DO	LVDS2_DO
24	PWRDNBAR	GENOUT1<1>
18,20,23,25		AGND
15,16		DGND
17,26		AVCC
27,28		DVCC

Table 19: Pin assignment of part U8 (DS92LV1021)

Pin Number	Pin Name	APD Net Name
1	SYNC1	LVDS3_SYNC1
2	SYNC2	GENOUT1<4>
3	DIN0	TOJPPARITY
4	DIN1	TOJP<0>
5	DIN2	TOJP<1>
6	DIN3	TOJP<2>
7	DIN4	TOJP<3>
8	DIN5	TOJP<4>
9	DIN6	TOJP<5>
10	DIN7	TOJP<6>
11	DIN8	TOJP<7>
12	DIN9	TOJP<8>
13	TCLK_R_F	LVDS3_TCK_R_F
14	TCLK	LVDS3_TCLK
19	DEN	LVDS3_DEN
21	DOBAR	LVDS3_DOBAR
22	DO	LVDS3_DO
24	PWRDNBAR	GENOUT2<0>
18,20,23,25		AGND
15,16		DGND
17,26		AVCC
27,28		DVCC

Table 20: Pin assignment of part U9 (DS92LV1021)

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