Final Design Review - Check List

- What is the maximum operating frequency — **50 MHz** [1]
- What is the minimum operating frequency — **single step**
- Master reset even if POR cell used — **yes**/no
- Checked for bus contentions on power on — **N/A**
- Does the circuit conforms to the vendors Design Guide lines — **yes**/no
- Are there any 'non-standard' operating conditions — **yes**/no[2]
  - internal clocking, gated clocks
- Have any compiled megacells used (DPRAMs, RAMs, Multipliers, etc) — **yes**/no
- BIST included for compiled megacells — yes/**no**[3]
  - if no how to test memories, multipliers (fault coverage)
- Are there any long shift register or counters — **yes**/no[4]
- Use of any custom cells — **yes**/no[5]
  - If yes then authorised by the vendor — **yes**/no
- Has the circuit been compiled and simulated — **yes**/no[1]
- Has it been functionally simulated to the maximum operating frequency — **yes**/no[1]
- Simulated to show specification is met — **yes**/no[1]
- Any changes to specification signed off — **yes**/no[6]
- DRC and LVS checks done on top level layout — yes/**no**
- Is the maximum junction temperature compatible with the de-rating — **yes**/no
- Simulations done for checking race conditions (skew check) — **yes**/no
- 1000 ns interval simulations used for static tests — **N/A**
- Timing analysis done — **yes**/no
- Worst case simulations done (min max for set-up and hold time violation) — **yes**/no
- Fan-out error messages cleared — **None**
- Warnings have been cleared with the vendor — **None**
- Internal scan paths used — **yes**/no
- DRC checks done after scan path insertion — **yes**/no
- Number of scan paths used compatible with the tester — **N/A**
- Does the simulations use stimuli from the input pins — **yes**/no
- Fault coverage of test vectors sufficient for known good dies for MCM — **yes**/no[7]
- Asynchronous inputs — **yes**/no
  - Metastable proofing for asynchronous inputs — **yes**/no
- Clock trees balanced — **yes**/no
- Output drivers compatible to external interfaces (Voh, Vol, Iol, Ioh) — **yes**/no
- Sufficient power and ground pins (for Core and for I/O) — **yes**/no[8]
- Pad size and pitch compatible with standard wire-bond — **yes**/no
- Power dissipation compatible with the package — **yes**/no[9]

Notes:

1. Not post-layout. Carry-out post layout before submission to manufacture
2. Gated clocks used - need to check with simulations for glitches. Will be checked by internal review.
3. BIST not used, will be tested via the serial interface
4. There are long counters, scan registers will be used here for testing
5. Only custom cell is the temperature sensor
6. All changes to the original specification to be documented
7. Aim to reach 98%-99% fault coverage
8. Manufactures guide lines observed
9. Compatible with the MCM