Handling JEM Slice data and RoIs on the ROD

This document describes the requirements for handling slice readout and RoI readout for the JEM processor on the prototype ROD modules

Reference:
[1] Prototype ROD Specification Version 1.1a

[2] Jet/Energy Processor module specification, Version Draft 0.8d, 13th November 2001

1. Handling JEM Slice data on the ROD

1.1 JEM Slice data as seen by the ROD

The slice data readout will be very similar to the slice data readout of the CPMs with single or multiple slice readout and zero suppression capability. The FPGA firmware needs to be developed to handle data and event formats as described below.

There are 13 sources of DAQ data from each JEM, hence the G-Link will be used in16 bit mode (M20SEL pin of the G-Link chip held low)

1. Incoming LVDS link data (9 bits) plus the error detect (SE) and link ready (LR) per Input FPGA, contributing to a one bit wide serial data stream to the G-Link (X 11 Input FPGAs)
2. 24 bit of Jet count information plus one odd parity bit (P)
3. 24 bit of energy sum information plus odd parity bit (P)

Data as seen by the ROD via the G-link is shown in figure 1 below. The data (89 bits/G-link data line) is merged on to the G-Link as follows:

1. G-Link data D[0:10] will carry input data from the 11 Input FPGAs.
2. D11 will carry the Jet count, thresholds 0 to 7 (three bits/threshold) plus the three eight bit energy sums.
3. D12 will carry the 12 bit BC number and a three bit crate number (4-7)
4. D[13:15] are unused and will be set to zeros.
5. There are 88 data bits and an odd parity bit (GP) on each of the G-link data lines.

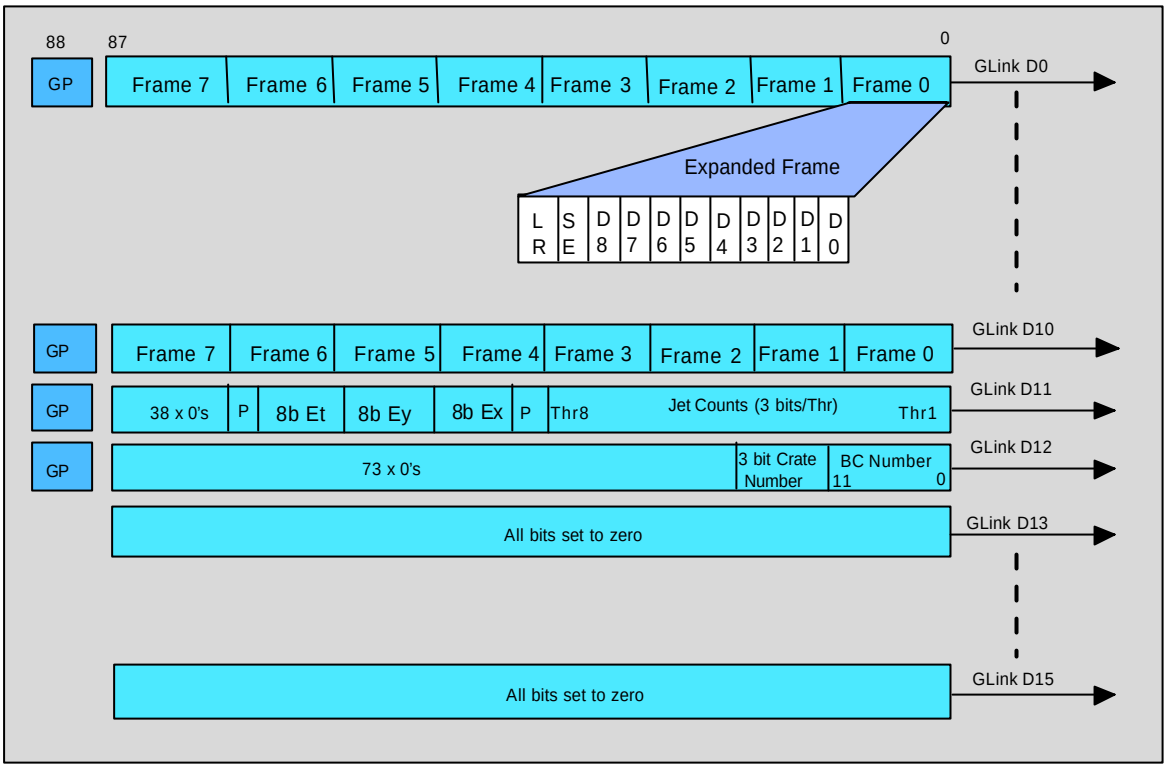

Figure 1: Slice Data as seen by the ROD.

1.2. Slice Data Event Format

The format of the JEM slice data sent to DAQ will be very similar to the CPM slice data event format with a header, data words, status words and a trailer (see 3.14 of [1])

The data word format will be as shown in figure 2. The frames are written on to the S-Link packets as they arrive from the G-Link in pair of frames starting from FPGA 1 to 11 to reduce latency and ease of design.

Note:

1. Bits 31:30 is used as a word ID to identify the type of data or sub status.

2. A3:A0 is used to identify the source of data (G-link data D0 to D12).

3. F1:F0 is used to identify the frames

4. A3:A0 in conjunction with Bit 26 will distinguish between jet count (set to 0) and energies (set to 1)

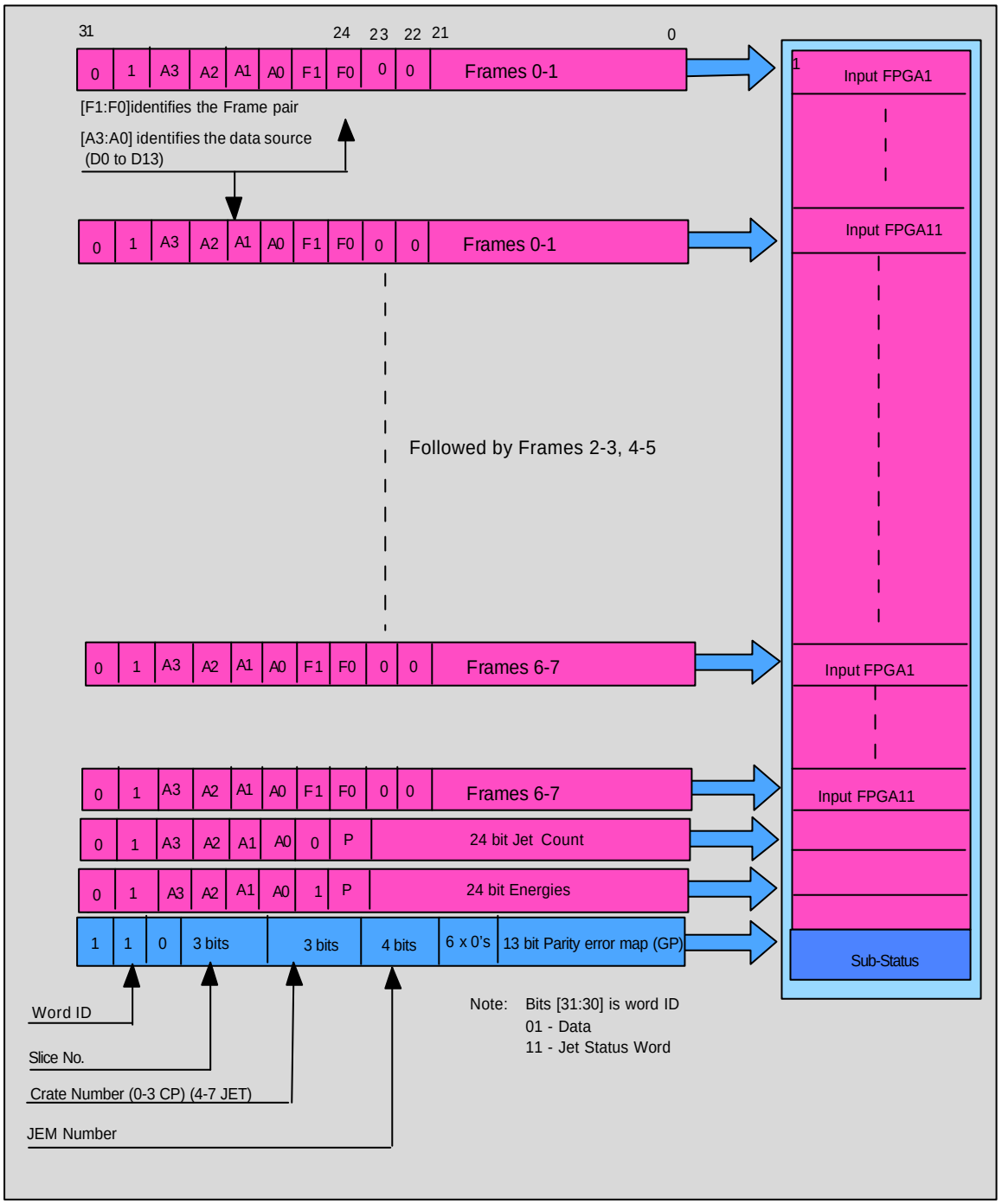

Figure 2: S-Link Data packet sent to DAQ

1.3 Status words

The status words will be as described in sections 3.10.1 and 3.10.2 of the Prototype ROD Specification Version 1.1a

2. Handling RoIs on the ROD

2.1 RoI data as seen by the ROD

The JEM RoIs as seen by the ROD is shown in figure 3 below. Four (0-3) RoI frames are sent on bit zero of the G-Link and Four (4-7) RoI frames are sent on bit one of the G-Link. Individual RoI frames will have and odd parity bit associated with it. Bit two of the G-Link will carry the BC number and the crate number. All unused G-link data lines will be set to zero.

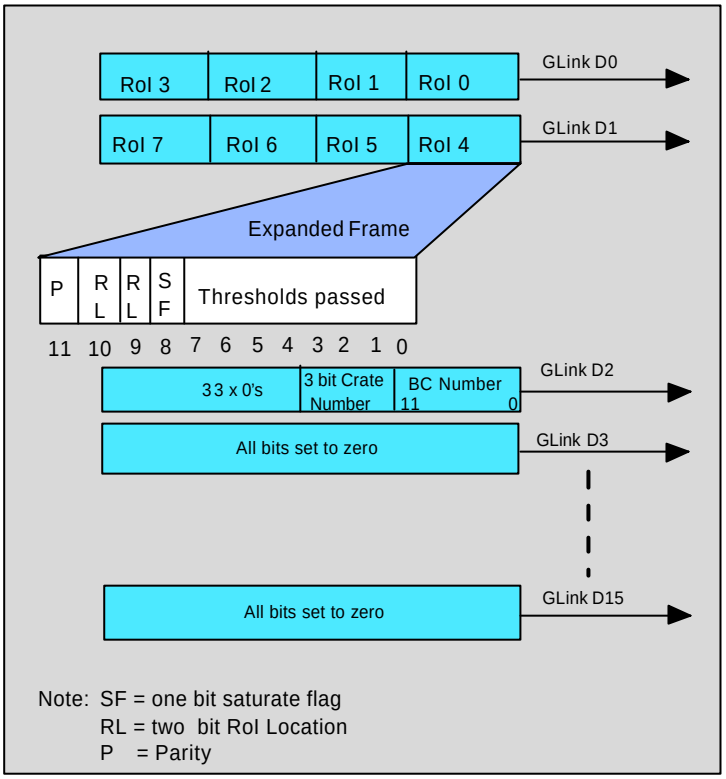

Figure 3. RoI data as seen by the ROD

2.2 RoI Event Format

The format of the RoIs sent to level 2 will be very similar to the slice event format with header, data words, status and a trailer. The data word format will as shown in figure 4 below

1. Bits 0 to 10 will carry a RoI frame as indicated in the diagram, RoI 0 followed by 4, 1, 5, etc as it arrives from the two data pins on the G-Link.
2. Bit 11 if set to one will indicate a parity error (error on JEM ->ROD link)
3. Bits 12 to 19 are unused and will be set to zero
4. Bits 20 to 22 (F0:F2) will identify the RoI frame
5. Bits 23 to 26 will identify the JEM
6. Bits 27 to 29 will be used to identify the crate number

7. Bits 30 and 31 are word ID, set to zero.

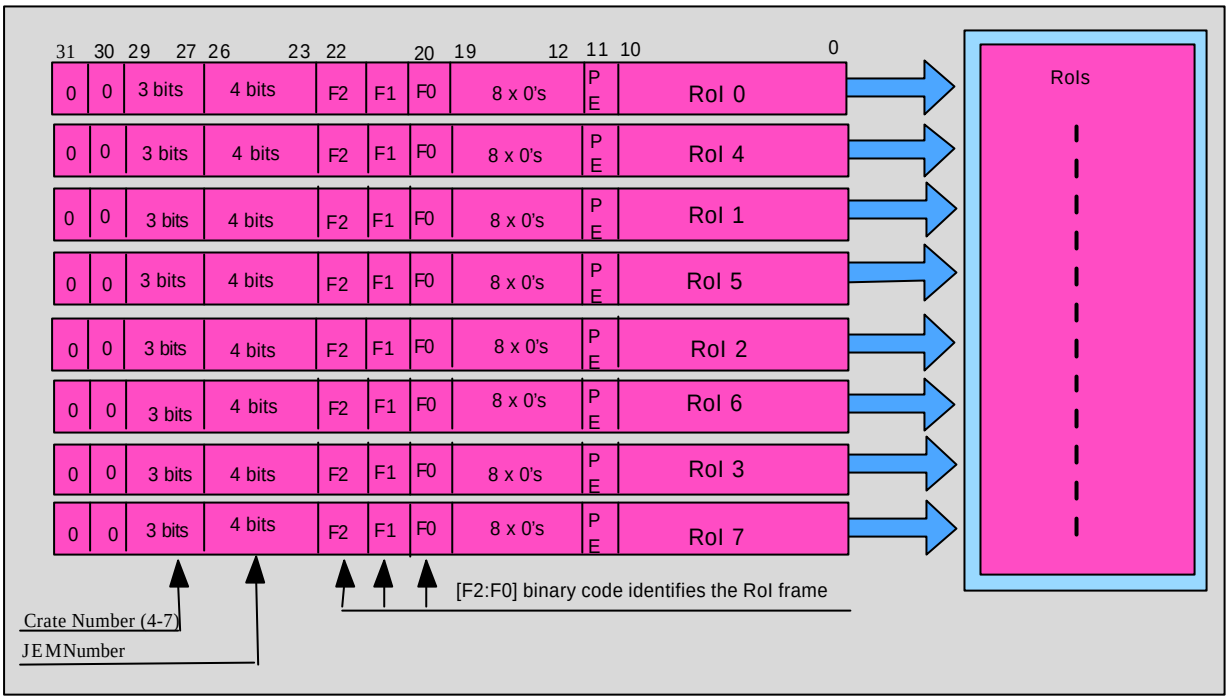

Figure 4. RoI Event Format

2.3 Status word

The status words will be as described in sections 3.10.1 and 3.10.2 of the Prototype ROD Specification Version 1.1a