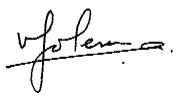
Project Specification

Project Name: ATLAS Calorimeter First Level Trigger- Prototype Read-out Driver

Version: 1.1a

October 2000

Approval	Name	Signature	Date
Project Manager	**V. Perera**		**11/10/00**

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Changes to version 1.1:

1. Memory map updated (Spy buffer)
2. More bits added to the Mother control register

1. Scope

To prototype the read-out driver module (ROD) and to demonstrate the data transfer from multiple data sources (cluster processor modules) to a data sink (read-out buffers) via the ROD module.

2. Related projects and documents

2.1 ATLAS TDR at http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html
2.2 S-link documentation at http://www.cern.ch/hsi/s-link/
2.3 Low Cost Gigabit Rate Transmit/receive Chip set from Hewlett Packard
2.4 TTC documents at http://www.cern.ch/TTC/intro.html
2.5 Data Source and Sink (DSS) Module- Requirement and Specification Document, Version 2C, July 1999
2.6 Serialiser FPGA Specification, http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html
2.7 CPM Specification, http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html
2.8 TTC Decoder Card, http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html

3. Technical Aspects

The ROD module will be a 6U VME motherboard with two plug-in Common Mezzanine Card (CMC) standard interfaces, to interface with the S-Link source module, and with the DSS module, which will emulate data from CPMs

3.1 Requirements and Specifications

A read-out driver (ROD) module in the final Cluster Processor (CP) and the Jet & energy processor (JEP) system has to collect data from the cluster processor modules (CPM), Jet Energy processor modules (JEMs) and hit counting modules (HCM), and send the formatted data on to the DAQ and to Level -2 (RoIs). The ROD requirements are listed below:

- Collect data from several trigger processing modules
- Data processing (zero suppression)
- Error detection on received data
- Format event data
- Interface to the readout link (S-link)
- Monitoring (spy on the data sent on the S-Link)
- Receive TTC
- Interface to CTP (ROD Busy)
- Operate at level-1 event rate

In the first stage the ROD prototype module will demonstrate the data transfer from the serialising FPGAs, since this has the highest data volume. The prototype will have four channels (e.g. one channel = data from one CPM), whereas the final ROD will have 16 channels.
A data source/sink (DSS) module will emulate the data transfer from the CPM and the data transfer to the read-out buffer (ROB) from the ROD module (see figure 1)

The ROD module will be used in the CP system and the in the JEP system for DAQ data as well as RoI data, hence the ROD should be adaptable to both systems by loading the appropriate firmware to handle different requirements.

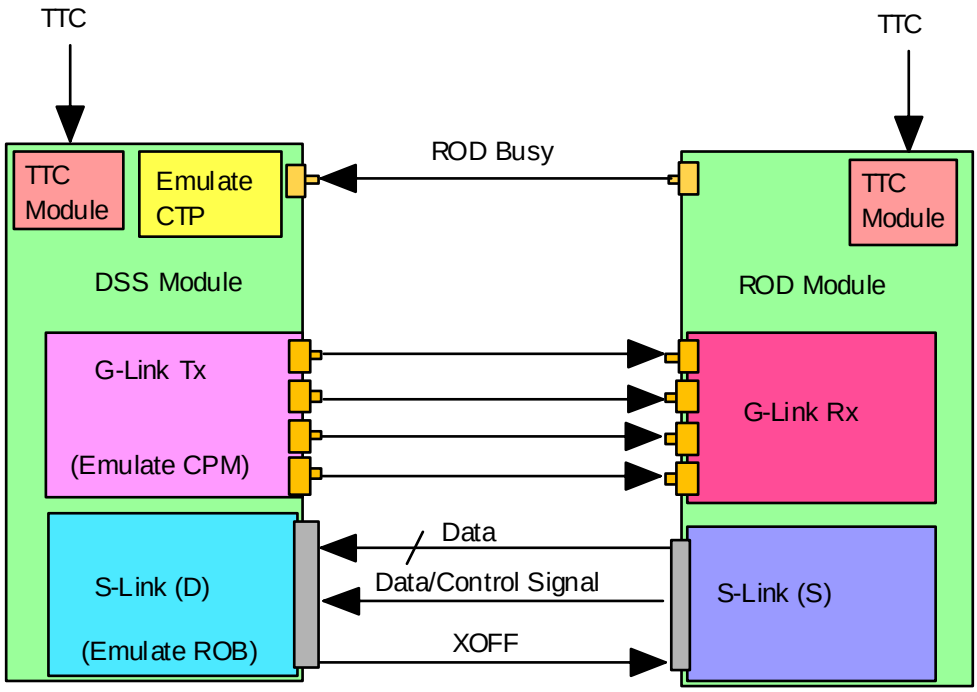

Figure 1. Prototype ROD Set-up

3.2 Functionality

The prototype ROD will provide the following functionality:
(a) Receive data at 800 Mbit/s using the G-Link Rx daughter cards.
(b) Compare the transmitted bunch numbers with the on-board TTCrx generated numbers. If the two do not match set an error flag in the readout data.
(c) Perform parity check on the incoming data.
(d) Perform zero suppression (ZS) on the trigger tower (TT) data from each channel.
(e) Option of bypassing ZS logic and not performing ZS
(f) Write formatted (see below for data format) data on to the FIFO buffers
(g) Select data to be transferred to the ROB on 'trigger type' received from the TTC.
(h) Transfer the data from these buffers to the ROB and the RoI builder using S-Link.
(i) Terminate RoI data transfer if the number of RoIs are greater than a pre-determined number
(g) Flag data words received with parity and link errors
(h) Provide an event buffer to spy on the S-link data
(i) Provide access to the spy event buffer via the VME to a single board computer (SBC)
(j) Carryout processing on the spy event buffer data using an FPGA or PCI DSP mezzanine card.
(k) Provide a PCI interface to access the spy event buffer

Figure 2 shows the block diagram of the prototype ROD module.

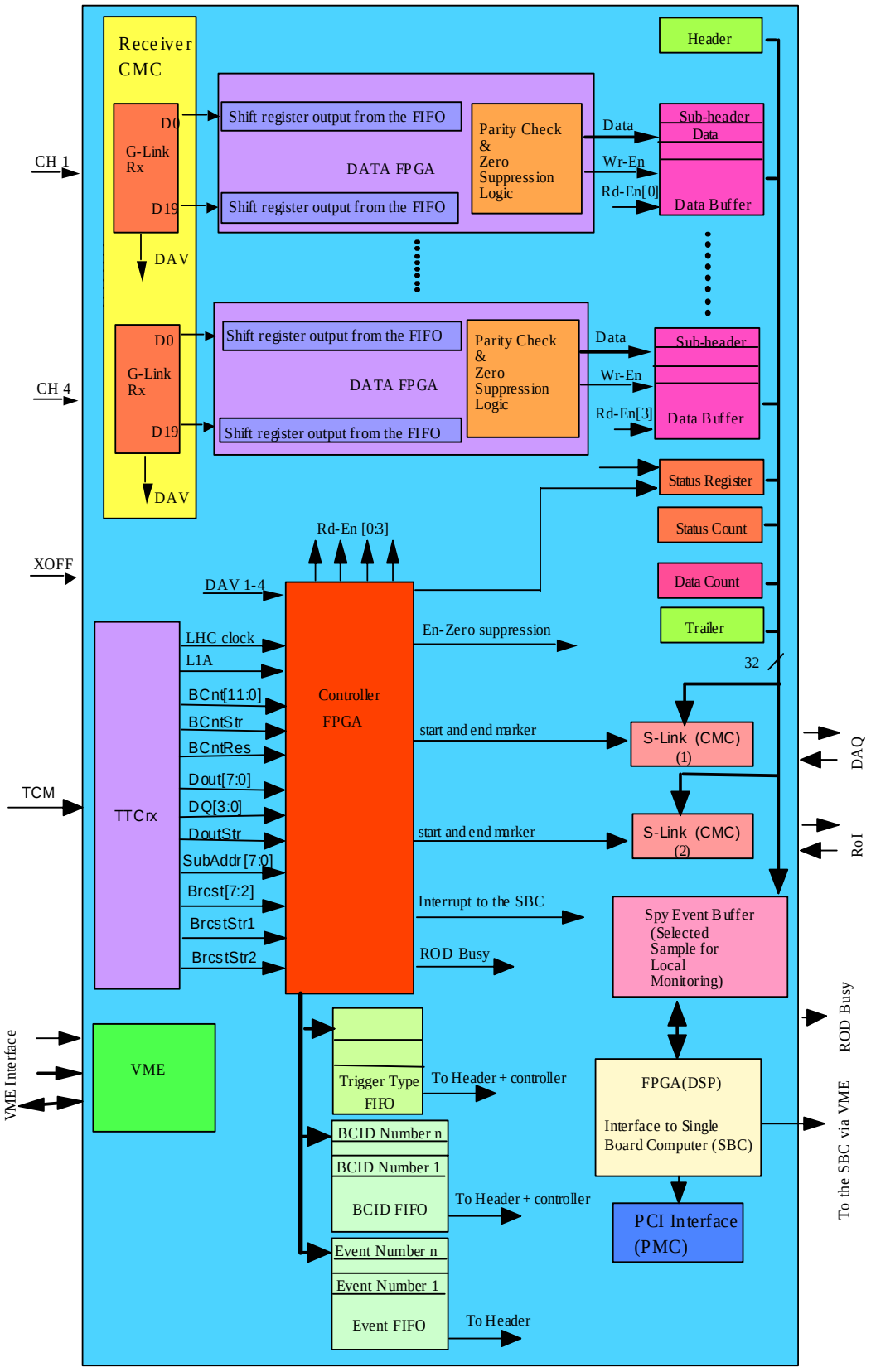

Figure 2. ROD Block Diagram

Note: The block diagram shows functionality not implementation

3.3 Read-Out Process

3.3.1 Sources of read-out data

There are three sources of read-out data (figure 3) from the CPMs; the 160 Mbit/s serialiser FPGAs, cluster hit count FPGAs and the cluster processor ASICs (or FPGAs). The serialiser data and the hits will be sent on one G-link, the data (RoIs) from the cluster processor ASICs will use a second G-Link. Since the largest data volume is on the serialiser FPGAs, the read-out process described below will be for this type of data.

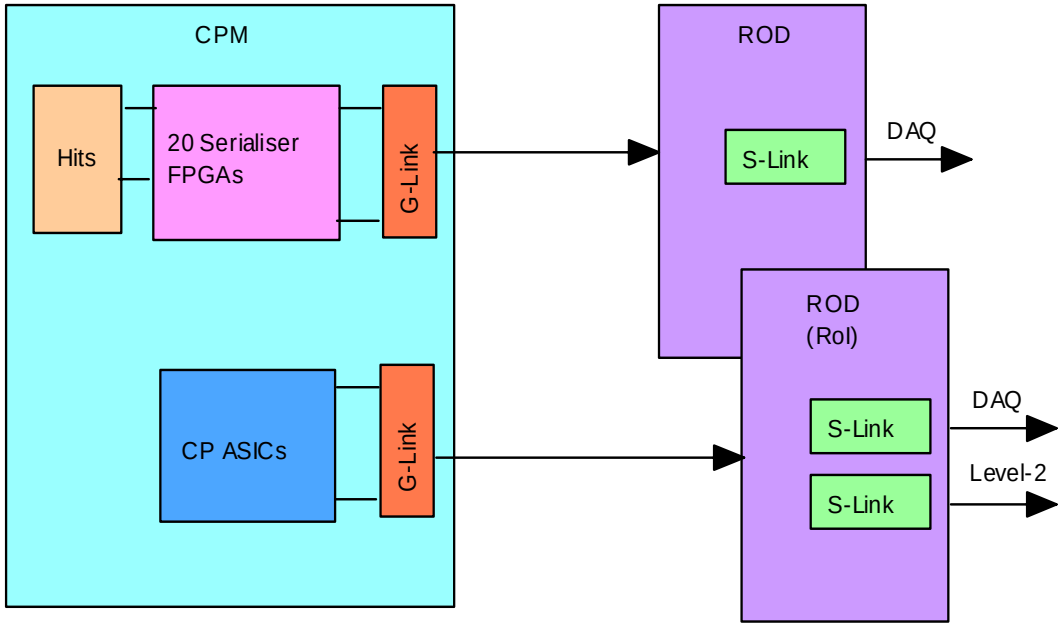

Figure 3. Data Source for the RODs

3.3.2 Serialiser Data

The serial data format of the serialiser FPGA, and as seen by the prototype ROD module is shown in figure 4. The bit field is arranged as shown for processing convenience.

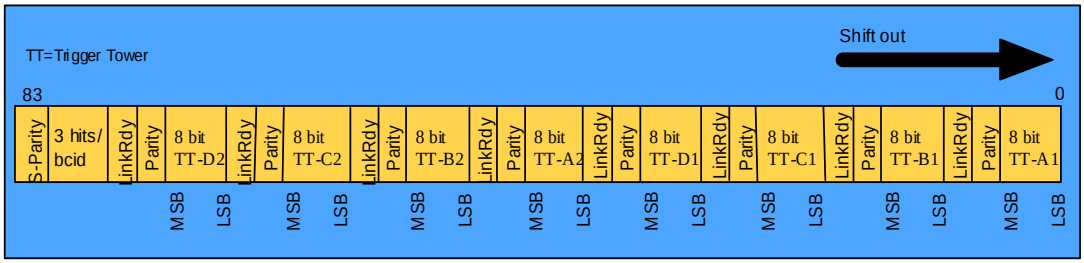

Figure 4. Serial Data Format as seen by the ROD

The ROD (see figure 2) will receive the data using a G-Link receiver mezzanine board and buffer the data until all the data is transferred out of these data buffers to the ROB. The entire process will be controlled by the controller logic on the ROD. The control logic will monitor the DAV signals of the G-links and initiate the data receive process. It will also check the contents of the slice register to determine how many slices of data are expected, and also depending on the trigger type information received from the TTCrx, it will transfer the appropriate data to the DAQ. There will be a time delay between the L1A and when the trigger type information is received on the ROD. The minimum time is 1.05 μs and the maximum unknown. Therefore if the trigger type does not arrive within a pre-defined time (programmable register) this data will be sent with the trigger type information set to zero, and it will be indicated in the status register (3.10).

The Data FPGAs as shown in figure 2, will perform zero suppression and parity checking and write data on to the data buffers. These data buffers will be readout sequentially one at a time, and will be transferred to the 'ROB' (DSS module for testing). A selection of these data will be copied on to the spy event buffer. A FPGA (DSP FPGA) will be provided for analysing this data, or to transfer the data via VME interface to a single board computer and/or to transfer the data to a DSP co-processor via a PCI interface for analysis and local monitoring. In some cases, depending on the trigger type information (e.g. test run) the data will not be transferred out on the S-link, but it is required that this data is written on to the spy event buffer.

On receipt of the level-1 accept signal, the control logic on the ROD will place the event number (ROD_L1ID) and the BCID number (ROD_BCID) generated by the TTCrx into the event and the BCID buffers. When it receives the DAV signal, the controller will take the event number and the BCID number from these buffers and place them on the header buffer FIFO and then initiate the ZS logic. The control logic will also check the received BCID number against the TTCrx generated number on the ROD. If there is a miss-match and providing there were no parity errors, then the controller will generate a signal to indicate to the TTC system to reset the BCID counters in the system via a status register (see 3.10). This condition should not occur if the system is in-step and operating correctly.

The five bit serialiser FPGA ID (20 FPGAs), the module ID (4 bits) and the crate ID (2 bits) will be implemented on the RODs. The FPGA ID is implicit from the connection to the data bit of the G-Link. The module ID will be the link number since each G-link will be uniquely assigned to a CPM, and the crate ID will be the ROD number since each ROD will uniquely handle data from one crate only. This information will be used in the header and sub-status of the S-Link formatted data frame as shown in figure 5.

Each data processing FPGA within the ROD will take control signals from the controller logic, and perform the ZS and then write the formatted data on to the data buffers including the crate ID and the module ID as shown in figure 5. During the testing phase, when the VME has to access these buffers, to prevent VME reading the

buffers when they are empty, the write counters should be read first to ascertain the data block length to be read out.

When the ZS has been completed and the data has been formatted, the controller will transfer the data from the four data buffers in an S-Link packet as follows:

S-Link Header
Data for slice 1 from data buffer 1
Sub-Status
Data for slice 2 from data buffer 1
Sub-Status
Data for slice 3 from data buffer 1
Sub-Status
Data for slice 4 from data buffer 1
Sub-Status
Data for slice 5 from data buffer 1
Sub-Status

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Data for slice 1 from data buffer 4
Sub-Status
Data for slice 2 from data buffer 4
Sub-Status
Data for slice 3 from data buffer 4
Sub-Status
Data for slice 4 from data buffer 4
Sub-Status
Data for slice 5 from data buffer 4
Sub-Status
S-Link Trailer

For a single slice event the S-Link packet will be as follows:
S-Link Header
Data for slice 1 from data buffer 1
Sub-Status
Data for slice 1 from data buffer 2
Sub-Status
Data for slice 1 from data buffer 3
Sub-Status
Data for slice 1 from data buffer 4
Sub-Status
Data for slice 1 from data buffer 5
Sub-Status
S-Link Trailer.

The controller will also monitor the Xoff signal from the ROBs to stop any data transfers in case the ROBs get full. Since the Xoff signal prevents the data transfer

out of the ROD module, the incoming data may fill the ROD buffers. In this situation, before the ROD buffers get full (almost full), the ROD must indicate to the CTP via the BUSY module to stop sending data (CTP will suppress the L1A signal).
Note: even if BUSY acts instantaneously, there could be several events in the CPMs, which need to be read out. Hence there must be enough space on the RODs.

3.3.3 Data Formats for Slice Readout

The data format within the event fragment will be as shown in figure 5 below.
The two most significant bits will be used to differentiate between:

1. Serialiser Data (01)

   Each data line within the 'data field' could be zero-suppressed to compress the amount of data to be transferred on to the DAQ.
2. Hit Data (10)
3. Sub-Status (11)
   1. Indicates any parity errors on the 20 serial lines from the serialiser FPGAs
   2. Crate number
   3. CPM number
   4. Slice Number

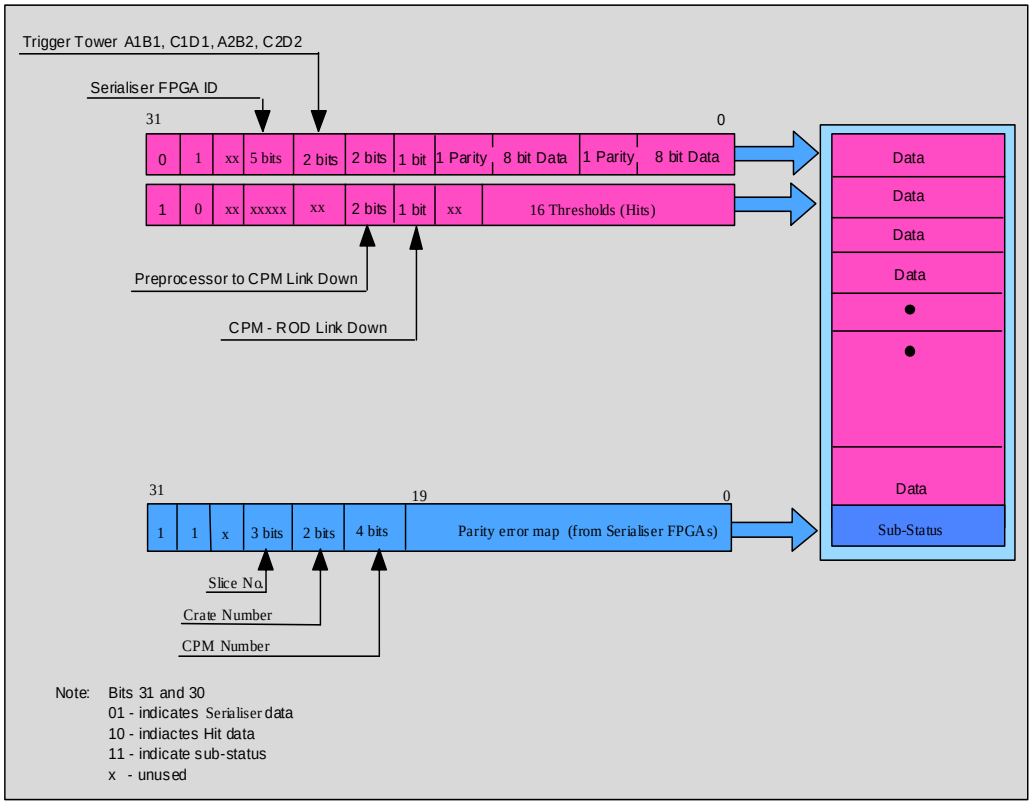

Figure 5. Data Format for Slice Readout.

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3.3.4 RoI Data

The principle of data transfer for the RoIs will be the same except for the bit field definitions and the requirement for terminating the RoI transmission to level-2. If there were more RoIs received from the CPMs than a pre determined RoI number held in a programmable register on the ROD, the ROD will terminate the RoI transmission to Level-2 and will indicate this via the status register (section 3.10).
The Data FPGAs must be capable of sorting the RoIs and transmitting the highest priority RoIs (e/γ) before transmitting the τ/h.

3.3.5 Data transfer Rates to ROD

Operating the shift register on the serialiser FPGA and the G-link in 20 bit mode at 40 MHz (960 Mbaud) you can transfer four time slices of data under 10 μseconds (100 KHz trigger rate). Transferring five time slices will meet the 75 KHz trigger rate, however if required the G-link and the shift register can be operated at a higher frequency (50 MHz for example) to meet the 100 KHz trigger rate requirement without any need for data compression on the serialiser FPGA.

3.3.6 TTCrx Interface

As mentioned above, the ROC will obtain information from the TTCrx chip.
The information arrives via broadcast through data and sub-addressing. Also the L1A and the bunch counter reset can be delayed to take into account the latencies associated within the system. Full details can be obtained from 2.4

The following sections (3.4 to 3.20) describe the functional blocks as shown in figure 2. Some of these blocks are implemented as daughter cards and some are implemented on the motherboard using FPGAs, FIFOs, and dual- port RAMs, etc

3.4 Receiver G-Link CMC

The ROD will receive data using a G-Link receiver CMC based on the HDMP-1024 chips from HP. These CMCs will be the same ones as described in the DSS specification. Other types of link technologies for the ROD can also be evaluated.

3.5 Header

The header will contain the following information and will be transferred out first.

Content	**Type**
Begin of Fragment (B0F00000 Hex)	Control
Start of Header Marker (EEEEEEEE Hex)	Data
Header Size (0008 Hex - number of words in the header excluding control word)	Data
Format Version Number (presently 1)	Data
Source_ID (serial number of the ROD)	Data
ROD_L1ID (24 bit event)	Data
ROD_BCID (12 bit BCID)	Data
Level 1 Trigger Type	Data
Detector Specific Event Type (00000000)	Data

3.6 BCID Number Buffer

This will be 256 deep x 16 bits wide FIFO buffer to queue the BCID number (12 bits) generated by the TTCrx chip on a level-1 accept signal. When the ROD receives a DAV signal, the first number in the queue is transferred to the header, ready to be transferred out on the S-Link.

3.7 Event Number Buffer

This will be 256 deep x 24 bits wide FIFO buffer to queue the event number (L1-ID) generated by the TTCrx chip on a level-1 accept signal. When the ROD receives a DAV signal, the first number in the queue is transferred to the header, ready to be transferred out on the S-Link

3.8 Trigger Type Buffer

This will be 256 deep x 8 bits wide FIFO buffer to queue the level-1 trigger type generated by the TTCrx chip on a level-1 accept signal. When the ROD receives a DAV signal, the first number in the queue is transferred to the header, ready to be transferred out on the S-Link

3.9 FIFO Data Buffers

The four data buffers will be 128K deep x 32 bits wide and will hold processed data in the format shown in figure 6 above ready to be transferred out on the S-Link.

3.10 Status Registers

There will be two status words to indicate to level-2 the status of the transmitted data. In non-corrupted events the status registers should be zero.

3.10.1 Status Word 1

This will be a single 32-bit word to indicate fatal error conditions such as buffer overflow and timeouts. Following are the bit definitions if the bit is set.

Bit 0 - indicates that one or more of the ROD buffers overflowed. This should not occur if the ROD busy mechanism to CTP is operating correctly.

Bit 1 - indicates a BCID mismatch between the ROD and a CPM.

Bit 2 - indicates a timeout has occurred due to non-arrival of data from CPMs (no DAV)

Bit 3 - Link error between Pre-processor and CPMs

Bit 4 - Link error between CPMs and RODs

Bit 5 - 31 – set to zero

3.10.2 Status Word 2

This will be a 32-bit word to interpret the contents of the data block

Bit 0 - indicates to level-2 that there were more than <n> RoIs and the transmission was terminated after the <n> RoIs were sent.

Bit 1- indicates a timeout condition if the trigger type does not arrive within a pre-determined time. However the data will be sent on after the timeout period with this flag set

3.11 Status Count

This 32-bit register is used to indicate the status summary using bits [31:16]. This field is not defined yet, therefore should be set to hex 0000. The bit field [15:0] is used to indicate the number of status words in the event fragment, which will be two in this design (see 3.10 above)

3.12 Data Count

This is a 32 bit counter indicates the number of data words in the event fragment**.**

3.13 Trailer

The trailer will include:
1. Number of status elements
2. Number of data elements
3. Status block position (one indicating that the data block precedes the status block)
4. End of fragment control word (E0F00000 Hex)

3.14 S-Link Interface

S-Link standard connector with the appropriate signals will be provided on the module to plug-in a commercially available S-Link source module. The event fragment with the format shown below will be transferred out on the S-Link.
The event fragment will be marked with a 'begin fragment' and an 'end fragment' using the control/data (UCTRL) line to indicate the data transmitted is a control word. Event throughput of 10 μs on the S-Link (operating at 100 Mbytes/s) must be maintained for a single slice event as well as for multi-slice events.

Content	**Type**
Begin of Fragment (B0F00000 Hex)	Control
Start of Header Marker (EEEEEEEE Hex)	Data
Header Size (0008 Hex - number of words in the header excluding control word)	Data
Format Version Number	Data
Source_ID - four byte field: [71][Crate ID][Module type][Module ID]	Data
ROD_L1ID (24 bit event)	Data
ROD_BCID (12 bit BCID)	Data
Leve1 Trigger Type	Data
Detector Specific Event Type (00000000)	Data
Data Words (from Data Buffers)	Data
Status Word-1	Data
Status Word-2	Data
Status Summary [31:16]/ Number of Status elements [15:0]	Data
Number of data elements	Data
Status block position	Data
End of Fragment (E0F00000 Hex)	Control

Two S-Link interfaces are provided on this module. When this module is used to send slice data to the DAQ then one S-Link (DAQ) interface is used. When this module is used to collect RoIs for level -2, a second S-Link (RoI) is used as well as the S-Link (DAQ) is used to send a copy of the RoIs to the DAQ.

3.15 Spy Event buffer

A 32 K space is reserved for capturing (spy) and processing the data sent out on the S-Link. Four 4K FIFOs will be used for capturing the spy data. The 4K buffers will hold a sample of data from a single event (data corresponding to a BCID number from all data buffers). The 'Event Buffer Manager' will allocate a free spy FIFO to capture the data and will transfer the data from these spy FIFOs to the 16 K RAM (DSP RAM) for processing. The same 16 K RAM will be used to store the processed data.
The data can be transferred out of the DSP RAM on to a single board computer (SBC) via the VME bus for monitoring and analysis, or the contents of this buffer can be accessed via a PCI interface to process the data using a DSP co-processor.

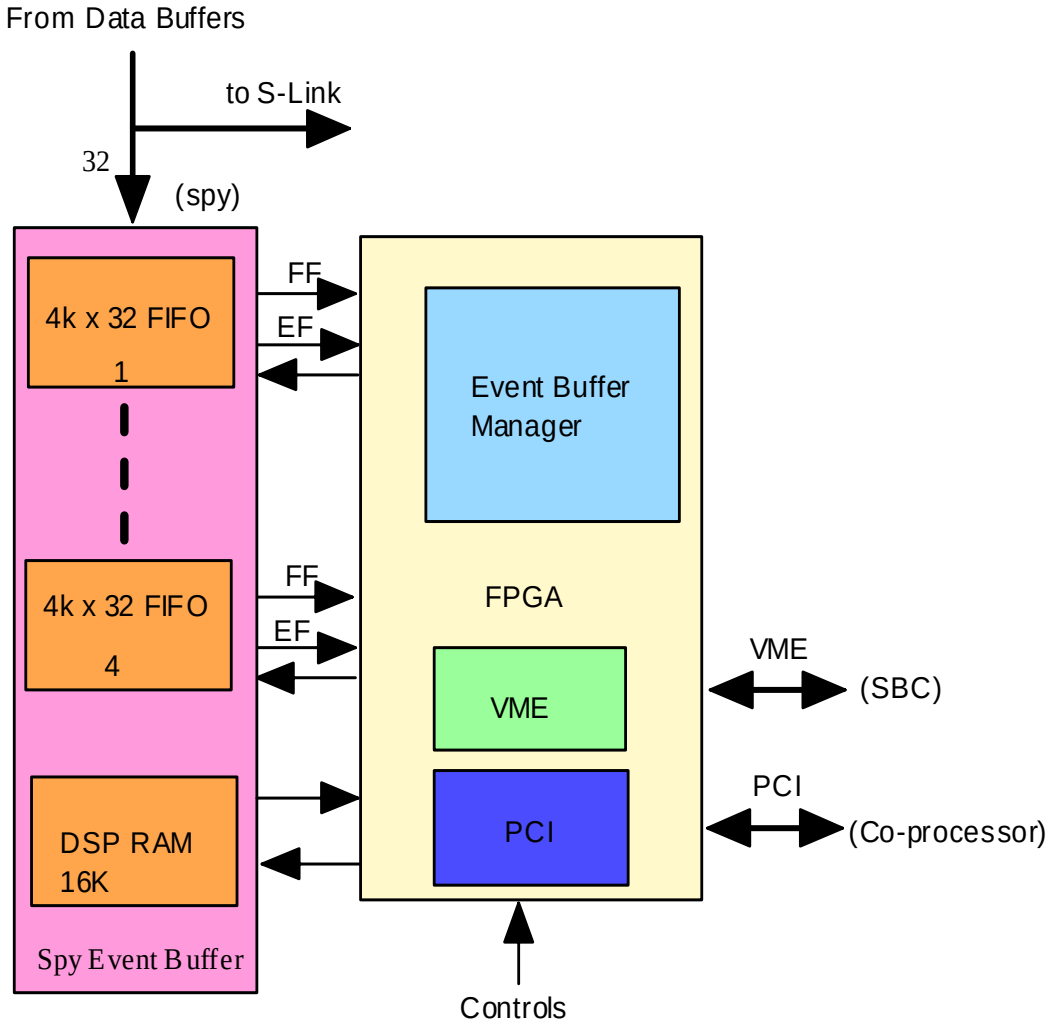


Figure 6. Spy Event Buffer Manger

3.16 FPGAs

3.16.1 Data FPGAs

All data processing logic described in section 3.3.2 will be implemented on these FPGAs. The block diagram indicates four FPGAs, however it may be implemented on fewer FPGAs taking into account new devices available at the time of the design.

3.16.2 FPGA (DSP)

An FPGA will be provided for accessing and managing the spy event buffer and to process the data using DSP functions. This FPGA will provide the necessary interface between the spy event buffer and a Single Board Computer, as well as, if required to provide an interface between the spy event buffer and a DSP Co-processor via a 32 bit PCI interface.

3.16.3 Controller FPGA

This implements all the control and buffer management and 'house keeping' functions.

3.16.4 Configuring the FPGAs

The FPGAs can be configured in the following ways to give maximum flexibility for the module users.

1. EEPROMs will be socketed so that they can be programmed with the configuration data using a standalone device programmer.
2. ISP port will be provided to down load configuration data from a PC for example.
3. VME port via a register will be provided, for downloading the FPGAs as well as the EEPROMs. The user must provide the software drivers.

3.17 Single Board Computer Interface

A Single board computer in the ROD crate can access the spy event buffers on the RODs via the VME.

3.18 PCI

The 32 bit, 33 MHz PCI interface will allow a commercial PMC Co-processor module to be used with the ROD module. This will be in place of the S-Link (RoI) module, to evaluate the requirements for DSP applications. The PCI interface will be implemented on the FPGA (DSP) using PCI core from the FPGA vendor.

3.19 VME Interface

All VME related logic such as; address decoding, memory addressing, and any other controls and status registers required will be implemented on a programmable logic device. The VME interface will be standard D32, A24/32 with interrupt capability.
Note: Final version of the ROD should probably be VME64 to comply with the ATLAS standard for RODs.

3.20 TTCrx Daughter Board

This module will interface with the TTC system and provide all the clocks and control signals for the ROD Module. The TTC Decoder card [2.9] test module will be used.

3.21 Motherboard

The motherboard will be a standard 6U VME module implementing all the functionality described above. It will be a triple width module to host the various CMC cards. If the rear PMC card and the S-Link (RoI) cards are not required then it will be implemented as a double width module.

3.21.1 Signal handling on the motherboard

The track impedance between the CMC connectors and the devices on the motherboard will be 75 Ω. All transmission lines should have series terminations for a 75 Ω track impedance.

3.21.2 Front Panel Input and Outputs

3.21.2.1 Front Panel Inputs

Description	Connector
TTCin	Via TTCrx module
Data-In [4..1]	Via G-Link Rx daughter card

3.21.1.2 Front Panel Outputs

Description	Logic	Connector
ROD Busy	LVDS	LEMO 00

3.21.3 Front Panel Monitoring (LEDs)

The LEDs will be located at the top of the front panel.

Description	Signal name	Colour
+5 Volts		Green
+3.3 Volts		Green
-5 Volts		Green
System clock is active	SYSCLK	Green
FPGAs Loaded	PromDone	Green
VME access in progress	Board_Sel	Yellow
Level-1 accept	L1ACCEPT	Green

* Fast signals will be stretched so that they will light the LEDs for long enough to be seen.

3.21.4 Rear Panel Input and Outputs

1) VME J1 Connector
2) VME J2 Connector

3.21.5 Test and Set-up Points

1. There will be logic analyser probe points on various data paths to aid in debugging the module.
2. JTAG boundary scan port
3. In-System-Programming (ISP) port for downloading FPGA code

3.21.6 Ground Points

Ground points will be provided for scope probe grounding in exposed areas of the motherboard.

3.21.7 Power Requirements

Voltage rail	Maximum. Current
+5V & +3.3V	9A
-5V	1A
+3.3V	7A

3.21.8 CMC Connectors

The connectors (Socket) used on the motherboard will be Molex 52763-0649 (10 mm stand-off)

3.21.8 Component Height Restrictions on the Motherboard

The component height restrictions and exclusion zones are shown in figure 7. The sane rules apply for the underside of the motherboard where CMC cards are positioned.

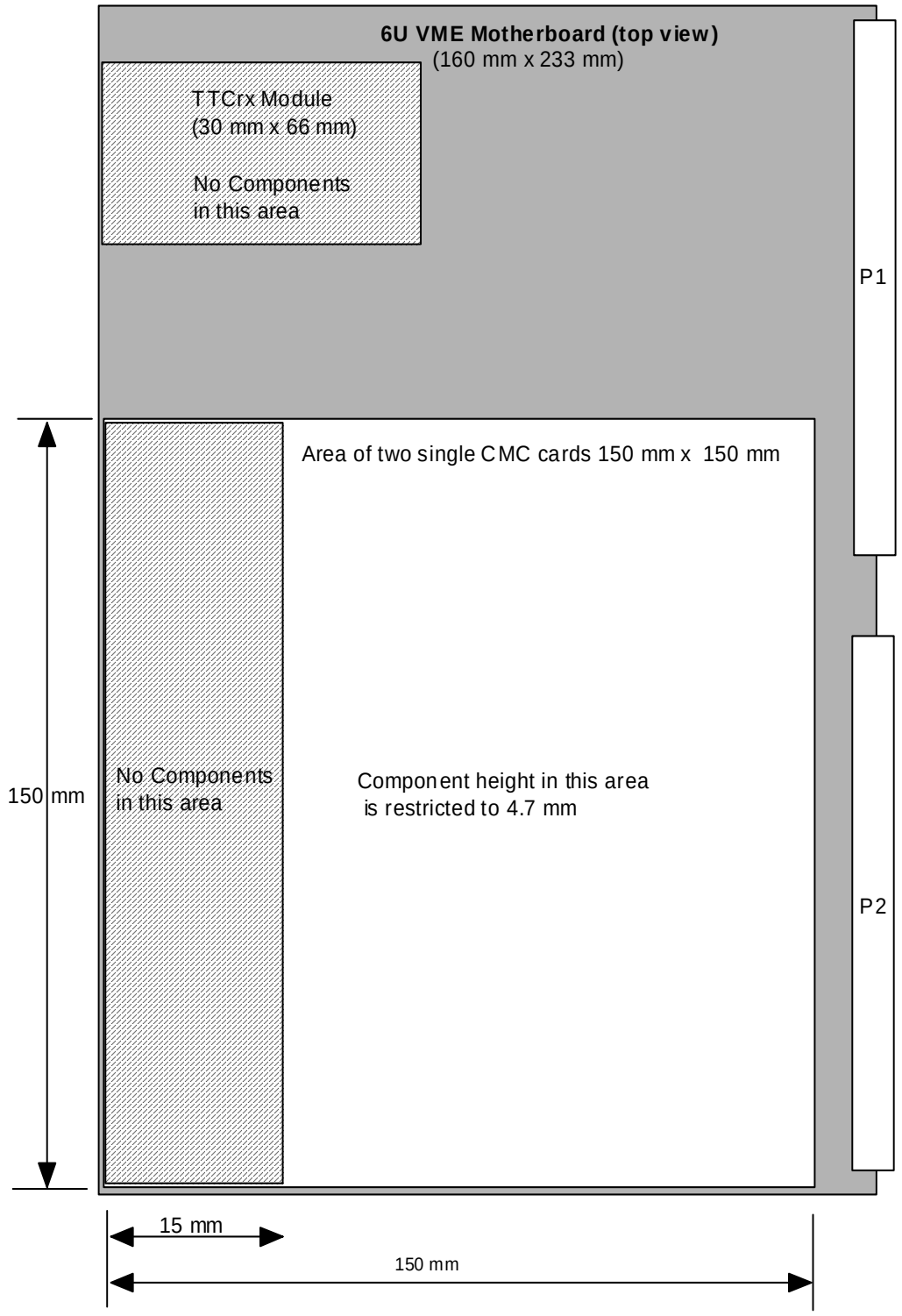


Figure 7. Motherboard Component Placement Restrictions (not to scale)

3.22 Programming Model

3.22.1 Guidelines

These are to aid the software control of the module.

1. All registers can be read by the computer, hence there are no 'write only' registers.

   1.1 All Status Registers shall be Read-Only registers.
   1.2 All Control Registers shall be Read/Write registers.

2. If the computer tries to read or write a value, which the module itself is able to modify at the same time, the data integrity cannot be guaranteed. The only exception been the Control Register and the Status Register. Therefore it is recommended that before any software tries to read or write to any registers the status of the module should ascertained by reading the Status Register.

3. When the address space occupied by the module is accessed, it will always respond with a handshake to avoid a bus error.

4. The power-up condition of all registers will be all zeros, unless otherwise stated.

3.22.2 Notation

The names of the registers and bit fields within them are written in *italic*. The names of the signal lines are *underlined italic*. Bit fields are labelled Input to Card and Output from Card rather than Write and Read to make it clear whether it is the card or the computer which is doing the writing.

In this document, a byte is always an 8-bit field, a word is always 16 bits and a long-word is always 32 bits.

Setting a bit field means writing a 1 to it, clearing it means writing a 0.

3.22.3 Memory Map

The ROD module is addressed using an A24 address bus. It uses the 20 least significant bits of the A24 address bus, hence the address space of the ROD module is 20-bits. This corresponds to 1024 kilobytes per module. The 4 most significant bits of the address can be pre-set by switches to allow the 1024 kilobyte memory space required to sit at any convenient 1024 kilobyte boundary within the 16 megabyte A24 address space.
The map shown below may change during the design phase to accommodate any design requirements not foreseen at the time of writing this document. For similar reasons the byte addresses are not allocated at this stage.

Address (hex)	Register type	Register Name	Size in bytes	Description
00000	RO	*MotherID*	4	Type, serial number & revision
00004	RW	*MotherCR*	4	Control Register
00008	RO	*MotherSR*	4	Status Register
0000C	RO	*G-Link DaughterID*	4	Serial number
00010	RW	*G-Link DaughterCR*	4	Control Register
00014	RO	*G-Link DaughterSR*	4	Status Register
00084	RO	*PMC DaughterID*	4	Serial number if applicable
00088	RW	*PMC DaughterCR*	4	Control Register
0008C	RO	*PMC DaughterSR*	4	Status Register
00064	RO	*Write-Counter1*	4	Wr counter data buffer 1
00068	RO	*Write-Counter2*	4	Wr counter data buffer 2
00074	RO	*Write-Counter3*	4	Wr counter data buffer 3
00078	RO	*Write-Counter4*	4	Wr counter data buffer 4
00018	RW	*Pulse Register*	4	Generates pulses
00080	RO	*S-Link_Revision*	4	S-Link FPGA Revision
00040	RO	*Controller_Revision*	4	Control FPGA Revision
00060	RO	*Data-1_Revision*	4	Data FPGA-1 Revision
00070	RO	*Data-2_Revision*	4	Data FPGA-2 Revision
0001C	RO	*VME-Revision*	4	VME Revision
00020	RW	*Program_Reg*	4	VME 'ISP' programming
00024	RW	*Crate-ModuleID*	4	Crate and Module ID
00028	RW	*Slice_Reg*	4	Number of slices to ROD
0002C	RW	*RoI_overflow*	4	Maximum number of RoIs
00030	RW	*Interrupt_register*	4	Interrupt control register
00044	RW	*BCID_Buffer*	1K (256 x 16)	BCID Buffer (bits [12:15] unused)
00048	RW	*Event_Number*	1K (256 x 32)	Event number Buffer (bits [24:31] unused)
0004C	RW	*Trigger_type*	1K (256 X 8)	Trigger type
20000	RW	*Data_Buffer_1*	512K (128Kx 32)	Data Buffer 1[1]
40000	RW	*Data_Buffer_2*	512K (128Kx 32)	Data Buffer 2[1]
60000	RW	*Data_Buffer_3*	512K (128Kx 32)	Data Buffer 3[1]
80000	RW	*Data_Buffer_4*	512K (128Kx 32)	Data Buffer 4[1]
A0000	RW	*Spy_Buffer_1*	16K (4 K x 32)	Spy Event Buffer 1
A4000	RW	*Spy_Buffer_2*	16K (4 K x 32)	Spy Event Buffer 2
A8000	RW	*Spy_Buffer_3*	16K (4 K x 32)	Spy Event Buffer 3

AC000	RW	*Spy_Buffer_4*	16K (4 K x 32)	Spy Event Buffer 4
B0000	RW	*DSP_Ram*	64K (16 K x 32)	DSP RAM
				Unused

Note 1. These buffers are FIFO buffers and not random access.

RO means that the computer can only read the value of this register, writing has no effect either to the value or the state of the module.

RW means that the computer can affect the state of the module by writing to this register.

All memory on the card is directly mapped into VME address space so as to be conveniently accessible by the computer.

The module responds to the following VME Address Modifier codes.

AM code	
39	Standard (A24) non-privileged data access
3D	Standard (A24) supervisory data access

3.22.4 MotherID Register

The ROD module identification register is used to uniquely identify the module.

Register Bits	Assignment	Description
0-15	RAL Number (2413)	Same for each module type, number recorded in RAL register
16-23	Module Serial number	an unique number assigned to each module
24-27	Issue	Issue number
28 -31		Unused

3.22.5 Mother Control Register

All bit fields are inputs to card. Power-up condition will initially set all control register bits to 0 unless otherwise stated.

Bit	Descriptive Name	Signal name
0 -7	*Zero suppression threshold*	*SuppressionTH[7:0]*
8	*Software-Xoff*	*X_OFF*
9-10	*Clock-Source*	*CLKSEL*

3.22.5.1 Zero Suppression Threshold

Bit 0 -7

Suppression TH[7:0] = 0	Suppression disabled
1< Suppression TH[7:0] < 255	Data below the threshold is suppressed

Bit 8

Software XOFF	Setting this bit HI will disable the read out circuitry, preventing the FIFOs from emptying.

Bit 9-10

This will set the board clock source.

[10:9]	Selected clock
00	Crystal Oscillator on Board [1]
01	TTC Clock40Des1
10	TTC Clock40Des2
11	TTC Clock40

Note 1

The default condition will be the 00. To prevent problems, selection of a TTC source will be prohibited if the TTC is not present, or not READY. In this situation the selection will revert to the default when the register is written to.

3.22.6 Mother Status Register

This is a read-only register.

Bit	Descriptive Name	Signal name	
0 (LSB)	*Data Buffer 1 Full*	*DB1FF*	
1	*Data Buffer 2 Full*	*DB2FF*	
2	*Data Buffer 3 Full*	*DB3FF*	
3	*Data Buffer 4 Full*	*DB4FF*	
4	*Data Buffer 1 Empty*	*DB1EF*	
5	*Data Buffer 2 Empty*	*DB2EF*	
6	*Data Buffer 3 Empty*	*DB3EF*	
7	*Data Buffer 4 Empty*	*DB4EF*	
8	*Control FPGA Loaded*	*PromCDone*	
9	*Data FPGA 1 Loaded*	*Prom1Done*	
10	*Data FPGA 2 Loaded*	*Prom2Done*	
11	*S-Link/PCI FPGA*	*Prom3Done*	
11	*TTC Ready*	*TTCReady*	
12-15			Always 0 on read

3.22.6.1Data Buffer Full

Bit 0 - 3

0	Data buffer not full
1	Data buffer full

3.22.6.2

Bit (4-7)

0	Data buffer not empty
1	Data buffer empty

3.22.6.3

Bit 8

0	Control FPGA not loaded
1	Control FPGA successfully loaded

3.22.6.4

Bit 9

0	FPGA 1 not loaded
1	FPGA 1 successfully loaded

3.22.6.5

Bit 10

0	FPGA 2 not loaded
1	FPGA 2 successfully loaded

3.22*.6.6*

Bit 11

0	SLINK/PCI FPGA is not ready
1	SLINK/PCI FPGA is ready

3.22*.6.7*

Bit 12

0	TTCrx is not ready
1	TTCrx is ready

3.22.7 Daughter ID Register

Bits 0-15 is reserved for the G-Link Rx daughter card.

Register Bits	Assignment	Description
0-4	Serial number	an unique number assigned to each module
5-31	zero	Set to zero

3.22.8 G-Link Daughter Control Register

*3.22.8.*1 DIV0

Bits 0

0 set 0 on DIV0 of G-links
1 set 1 on DIV0 of G-links

3.22.9 G-Link Daughter Status register

3.22.9.1

Bits 0 -3

0 Links not locked
1 Links locked

3.22.10 PMC Daughter ID Register

Reserved for the DSP Co-processor

3.22.11 PMC Daughter Control Register

Reserved for the DSP Co-processor

3.22.12 PMC Daughter Status register

Reserved for the DSP Co-processor

3.22.13 Write Counters 1-4

When the VME has to access the data buffers, to prevent VME reading the buffers when they are empty, the write counters should be read first to ascertain the data block length to be read out.

3.22.14 Pulse Register

Bit	Descriptive Name	Signal name	
0 (LSB)	*Motherboard Reset*	*MBReset*	Pulse (200ns)
1	*TTC Reset*	*TTCReset*	Pulse (200ns)
2	*G-Link Reset*	*Glink_Reset*	Pulse (200ns)
3	*FIFO Reset*	*FIFO-Reset*	Pulse (200ns)
4	*FIFO Retransmit*	*Retransmit*	Pulse (200ns)

3.22.14.1 Global Reset

Bit 0

When a 1 is written to this bit, a single pulse will reset the module to a known power-up state. *Global Reset* is always read 0, and writing 0 has no effect.

The same effect can be produced using the VME *System Reset**.

0	Read value, no effect on writing
1	Resets the module to the initial power-up state

3.22.14.2 TTC Reset

Bit 1

When a 1 is written to this bit, a single pulse will reset the TTCrx chip to power-up state. *TTC reset* is always read 0, and writing 0 has no effect.

0	Read value, no effect on writing
1	Resets the TTCrx chip

3.22.14.3 G-Link Reset

Bit 2

When a 1 is written to this bit, a single pulse will reset the G-Link chips to power-up state. *G-Link reset* is always read 0, and writing 0 has no effect.

0	Read value, no effect on writing
1	Resets the G-Link chips

3.22.15 FPGA Revision Registers

Bits 31-24 Revision number (Starts at 01)
Bits 23-16 Function code.
Bits 15-0 "2413" (should match with the ROD mother ID).

3.22.15.1 Function Codes (Bits 23-16)

Code (Binary)	FPGA function
"00110000"	S-Link FPGA (+ PCI)
"00110010"	Controller FPGA
"00110001"	Data FPGA
"00110011"	VME Registers

3.22.16 Program_Reg

If required, this register is used to program the FPGAs as well the EEPROMs via the VME. The register bit definition will be assigned at the design phase.
Note: the default FPGA configuration method will be via EEPROMs at power-up

3.22.17 Crate_ModuleID

This register holds the crate and module number, which is passed on to Level-2 and DAQ.

Bits 0 - 1 Crate ID Channel 1
Bits 2 - 3 Crate ID Channel 2
Bits 4 - 5 Crate ID Channel 4
Bits 6 - 7 Crate ID Channel 5
Bits 8 - 11 Module ID Channel 1
Bits 12 - 15 Module ID Channel 2
Bits 16 - 19 Module ID Channel 3
Bits 20 - 23 Module ID Channel 4

3.22.18 Slice_Register

Holds the number of slices which will arrive from the CPMs on a given run. This could between one and five

3.22.19 RoI_overflow

This register hold the maximum number of RoIs to be transfererd to Level-2

3.22.20 Interrupt_Register

This register controls the interrupts from this module. The bit field will be defined later

3.22.21 BCID_Buffer

see3.6

3.22.22 Event_number

see 3.7

3.22.23 Trigger_type

see 3.8

3.22.24 Data_Buffers 1-4

see 3.9

3.22.25 Spy Event Buffer

see 3.15

3.23 ROD Daughter Boards.

The daughter boards must comply with the IEEE P1386/Draft 2.0, 4 April-1995, standard for a Common Mezzanine Card (CMC) family.

The types of CMC cards used on the ROD module are given below:
1. DSS to ROD interface module on top side of ROD
2. ROD to S-link interface (DAQ) module on top side of ROD
3. ROD to second S-link interface (RoI) module on bottom side of ROD
4. PMC card also can be used in place of the second S-link card when using a commercial PMC DSP Co-processor.

Figure 8 and 9 shows the daughter board positioning on the ROD module, and the following section shows the connector definitions.

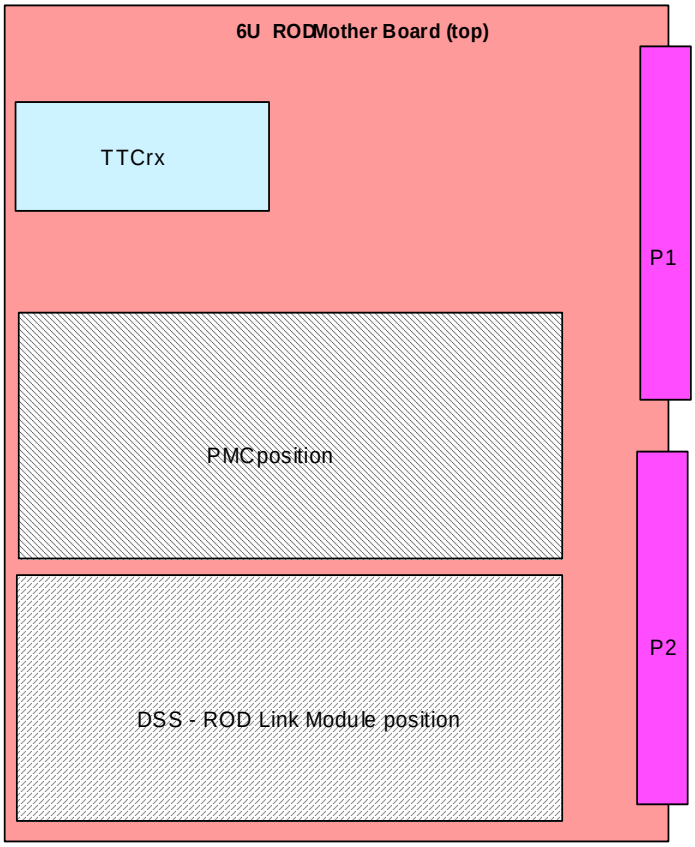


Figure 8. Motherboard (top view) - Daughter Card Positions

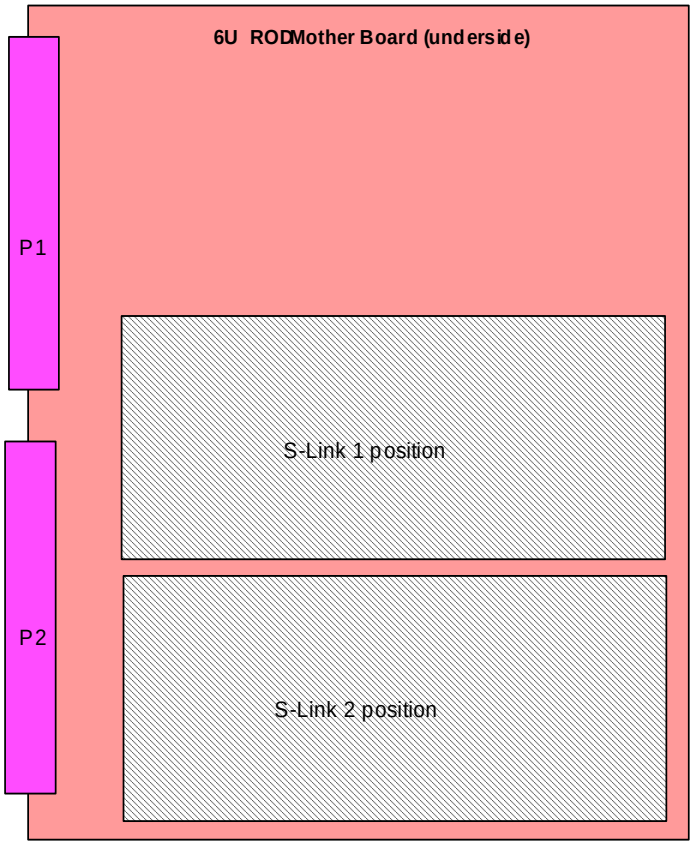


Figure 9. Motherboard (underside view) Daughter Card Position

3.23.1 Connector Definitions.

3.23.1.1 S-Link Source Card (LSC) Connector - S

Pin	Signal	Signal	Pin
1	LRL3	LRL2	2
3	VCC	LRL1	4
5	VCC	LRL0	6
7	LDOWN#	GROUND	8
9	GROUND	LFF#	10
11	UCLK	GROUND	12
13	GROUND	UWEN#	14
15	URESET#	GROUND	16
17	UDW1	UTEST#	18
19	UCTRL#	UDW0	20
21	UD31	VCC	22
23	GROUND	UD30	24
25	UD29	UD28	26
27	UD27	GROUND	28
29	UD26	UD25	30
31	GROUND	UD24	32
33	UD23	UD22	34
35	UD21	GROUND	36
37	UD20	UD19	38
39	VCC	UD18	40
41	UD17	UD16	42
43	UD15	GROUND	44
45	UD14	UD13	46
47	GROUND	UD12	48
49	UD11	UD10	50
51	UD9	VCC	52
53	UD8	UD7	54
55	GROUND	UD6	56
57	UD5	UD4	58
59	UD3	GROUND	60
61	UD2	UD1	62
63	VCC	UD0	64

Table 1. S-Link Source Card pin-out

3.23.1.2 G-Link Receiver Board Connector J1

Pin	Signal	Signal	Pin
1	GLinkRESET* (C)	-12V	2
3	GROUND	GLinkRdyA* (S)	4
5	DBID-1	GLinkRdyB* (S)	6
7	Busmode1#	+5V	8
9	DBID-2	GLinkRdyC* (S)	10
11	GROUND	GLinkRdyD* (S)	12
13	GLinkRefCLK	GROUND	14
15	GROUND	GLinkDAVA* (F)	16
17	DBID-3	+5V	18
19	V(I/O)-1	GLinkDAVB* (F)	20
21	GLinkErrA	GLinkDAVC* (F)	22
23	GLinkErrB	GROUND	24
25	GROUND	GLinkDAVD* (F)	26
27	GLinkErrC	DBID-4	28
29	GLinkErrD	+5V	30
31	V(I/O)-1	DBID-5	32
33	DC_DATA_D0	GROUND	34
35	GROUND	DC_DATA_D1	36
37	DC_DATA_D2	+5V	38
39	GROUND	DC_DATA_D3	40
41	DC_DATA_D4	DC_DATA_D5	42
43	DC_DATA_D6	GROUND	44
45	V(I/O)-1	DC_DATA_D7	46
47	DC_DATA_D8	DC_DATA_D9	48
49	DC_DATA_D10	+5V	50
51	GROUND	DC_DATA_D11	52
53	DC_DATA_D12	DC_DATA_D13	54
55	DC_DATA_D14	GROUND	56
57	V(I/O)-1	DC_DATA_D15	58
59	DC_DATA_D16	DC_DATA_D17	60
61	DC_DATA_D18	+5V	62
63	GROUND	DC_DATA_D19	64

Table 2. G-Link Destination Board Connector J1 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

3.23.1.3 G-Link Receiver Board Connector J2

Pin	Signal	Signal	Pin
1	+12V	DisMotherProm1	2
3		DisMotherProm2	4
5	PromDONE	GROUND	6
7	GROUND	PromDATA	8
9	PromINIT	DIV0 (C)	10
11	Busmode2#	+3.3V	12
13	EqA(C)	Busmode3#	14
15	+3.3V	Busmode4#	16
17	EqB(C)	GROUND	18
19	GLinkStrbA (F)	GLinkStrbB (F)	20
21	GROUND	EqC(C)	22
23	GLinkStrbC (F)	+3.3V	24
25	EqD(C)	Ser_En	26
27	+3.3V	GLinkStrbD (F)	28
29	DC_DATA_C0	GROUND	30
31	DC_DATA_C2	Mod20Sel (C)	32
33	GROUND	DC_DATA_C1	34
35	PromCCLK	+3.3V	36
37	GROUND	DC_DATA_C3	38
39	DC_DATA_C4	GROUND	40
41	+3.3V	DC_DATA_C5	42
43	DC_DATA_C6	GROUND	44
45	DC_DATA_C8	DC_DATA_C7	46
47	GROUND	DC_DATA_C9	48
49	DC_DATA_C10	+3.3V	50
51	DC_DATA_C12	DC_DATA_C11	52
53	+3.3V	DC_DATA_C13	54
55	DC_DATA_C14	GROUND	56
57	DC_DATA_C16	DC_DATA_C15	58
59	GROUND	DC_DATA_C17	60
61	DC_DATA_C18	+3.3V	62
63	GROUND	DC_DATA_C19	64

Table 3. G-Link Destination Board Connector J2 pin-out

(S) - Status Register
(F) - Data FPGA
(C) - Control Register

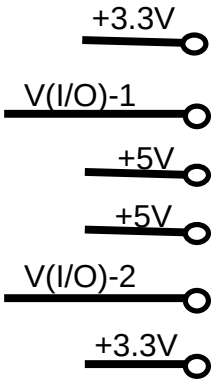
Note 1. Busmode [4:2]# signals are driven by the motherboard, Busmode 1# is returned by the daughter card to indicate presence of the card. These signals are not used in the G-Link daughter card design.
2. User Defined pins are spare pins for future use.

3.23.1.4 G-Link Receiver Board Connector J3

Pin	Signal	Signal	Pin
1	DC_DATA_A0	GROUND	2
3	GROUND	DC_DATA_A1	4
5	DC_DATA_A2	DC_DATA_A3	6
7	DC_DATA_A4	GROUND	8
9	V(I/O)-2	DC_DATA_A5	10
11	DC_DATA_A6	DC_DATA_A7	12
13	DC_DATA_A8	GROUND	14
15	GROUND	DC_DATA_A9	16
17	DC_DATA_A10	DC_DATA_A11	18
19	DC_DATA_A12	GROUND	20
21	V(I/O)-2	DC_DATA_A13	22
23	DC_DATA_A14	DC_DATA_A15	24
25	DC_DATA_A16	GROUND	26
27	GROUND	DC_DATA_A17	28
29	DC_DATA_A18	DC_DATA_A19	30
31	DC_DATA_B0	GROUND	32
33	GROUND	DC_DATA_B1	34
35	DC_DATA_B2	DC_DATA_B3	36
37	DC_DATA_B4	GROUND	38
39	V(I/O)-2	DC_DATA_B5	40
41	DC_DATA_B6	DC_DATA_B7	42
43	DC_DATA_B8	GROUND	44
45	GROUND	DC_DATA_B9	46
47	DC_DATA_B10	DC_DATA_B11	48
49	DC_DATA_B12	GROUND	50
51	GROUND	DC_DATA_B13	52
53	DC_DATA_B14	DC_DATA_B15	54
55	DC_DATA_B16	GROUND	56
57	V(I/O)-2	DC_DATA_B17	58
59	DC_DATA_B18	DC_DATA_B19	60
61		GROUND	62
63	GROUND		64

Table 4. G-Link Destination Board Connector J3 pin-out

Note: The V(I/O) pins on P1 and P3 should be tracked as shown below for selecting additional voltage pins if necessary



3.23.1.5 Spare J4 connector G-Link

Pin	Signal	Signal	Pin
1	VME-DATA_0	VME-DATA_1	2
3	VME-DATA_2	VME-DATA_3	4
5	VME-DATA_4	VME-DATA_5	6
7	VME-DATA_6	VME-DATA_7	8
9	VME-DATA_8	VME-DATA_9	10
11	VME-DATA_10	VME-DATA_11	12
13	VME-DATA_12	VME-DATA_13	14
15	VME-DATA_14	VME-DATA_15	16
17	GROUND	GROUND	18
19	VME-Write*	VME-DS	20
21			22
23			24
25			26
27			28
29			30
31			32
33			34
35			36
37			38
39			40
41	GROUND	GROUND	42
43	TDI	TCK	44
45	TMS	TDO	46
47	C/S-0	C/S-1	48
49	C/S-2	C/S-3	50
51	C/S-4	C/S-5	52
53	C/S-6	C/S-7	54
55	C/S-8	C/S-9	56
57	C/S-10	C/S-11	58
59	C/S-12	C/S-13	60
61	C/S-14	C/S-15	62
63	GROUND	GROUND	64

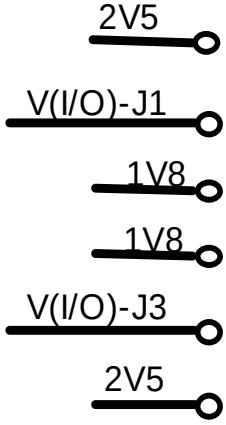
Connector J4 pin-out

3.23.1.6 PMC Connector J1

Pin	Signal	Signal	Pin
1	TCK	-12V	2
3	GROUND	INTA#	4
5	INTB#	INTC#	6
7	Busmode1#	+5V	8
9	INTD#	PCI-RSVD*	10
11	GROUND	PCI-RSVD*	12
13	CLK	GROUND	14
15	GROUND	GNT#	16
17	REQ#	+5V	18
19	V (I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GROUND	24
25	GROUND	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V (I/O)	AD[17]	32
33	FRAME#	GROUND	34
35	GROUND	IRDY#	36
37	DEVSEL#	+5V	38
39	GROUND	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	GROUND	44
45	V (I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[9]	+5V	50
51	GROUND	C/BE[0]#	52
53	AD[6]	AD[05]	54
55	AD[4]	GROUND	56
57	V (I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GROUND	REQ64#	64

Table 5. PMC Connector J1 pin-out

Note: The V (I/O) pins should be tracked as shown below for selecting additional voltage pins if necessary



3.23.1.7 PMC Connector J2

Pin	Signal	Signal	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GROUND	6
7	GROUND	PCI-RSVD*	8
9	PCI-RSVD*	PCI-RSVD*	10
11	Busmode2#	+3.3V	12
13	RST#	Busmode3#	14
15	+3.3V	Busmode4#	16
17	PCI-RSVD*	GROUND	18
19	AD[30]	AD[29]	20
21	GROUND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GROUND	30
31	AD[16]	C/BE[2]#	32
33	GROUND	PMC-RSVD*	34
35	TRDY#	+3.3V	36
37	GROUND	STOP#	38
39	PERR#	GROUND	40
41	+3.3V	SERR#	42
43	C/BE[1]#	GROUND	44
45	AD[14]	AD[13]	46
47	GROUND	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PCI-RSVD	52
53	+3.3V	PCI-RSVD	54
55	PMC-RSVD	GROUND	56
57	PMC-RSVD	PMC-RSVD	58
59	GROUND	PMC-RSVD	60
61	ACK64#	+3.3V	62
63	GROUND	PMC-RSVD	64

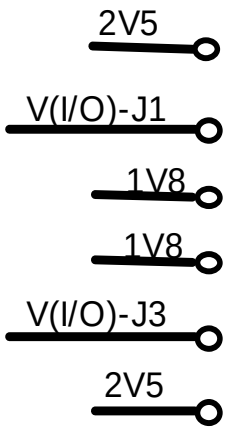
Table 6. PMC Connector J2 pin-out

3.23.1.8 PMC Connector J3

Pin	Signal	Signal	Pin
1		GROUND	2
3	GROUND		4
5			6
7		GROUND	8
9	V(I/O)		10
11			12
13		GROUND	14
15	GROUND		16
17			18
19		GROUND	20
21	V(I/O)		22
23			24
25		GROUND	26
27	GROUND		28
29			30
31		GROUND	32
33	GROUND		34
35			36
37		GROUND	38
39	V(I/O)		40
41			42
43		GROUND	44
45	GROUND		46
47			48
49		GROUND	50
51	GROUND		52
53			54
55		GROUND	56
57	V(I/O)		58
59			60
61		GROUND	62
63	GROUND		64

PMC Connector J3 pin-out

Note: The V (I/O) pins should be tracked as shown below for selecting additional voltage pins if necessary



3.23.1.9 J4 connector

Pin	Signal	Signal	Pin
1	VME-DATA_0	VME-DATA_1	2
3	VME-DATA_2	VME-DATA_3	4
5	VME-DATA_4	VME-DATA_5	6
7	VME-DATA_6	VME-DATA_7	8
9	VME-DATA_8	VME-DATA_9	10
11	VME-DATA_10	VME-DATA_11	12
13	VME-DATA_12	VME-DATA_13	14
15	VME-DATA_14	VME-DATA_15	16
17	GROUND	GROUND	18
19	VME-Write*	VME-DS	20
21			22
23			24
25			26
27			28
29			30
31			32
33			34
35			36
37			38
39			40
41	GROUND	GROUND	42
43	TDI	TCK	44
45	TMS	TDO	46
47	C/S-0	C/S-1	48
49	C/S-2	C/S-3	50
51	C/S-4	C/S-5	52
53	C/S-6	C/S-7	54
55	C/S-8	C/S-9	56
57	C/S-10	C/S-11	58
59	C/S-12	C/S-13	60
61	C/S-14	C/S-15	62
63	GROUND	GROUND	64

Connector J4 pin-out

3.23.1.10 TTC dec card J1 Connector

Pin	Signal	Signal	Pin
1	GND	Clk L1 Acc	2
3	Brcst Str 1	GND	4
5	Db Err Str	Sb Err Str	6
7	GND	D Out Str	8
9	Brsct <3>	Brsct <2>	10
11	Sub Addr <1>	Sub Addr <0>	12
13	Sub Addr <3>	Sub Addr <2>	14
15	Sub Addr <4>	GND	16
17	Sub Addr <6>	Sub Addr <5>	18
19	GND	Sub Addr <7>	20
21	DQ <1>	DQ <0>	22
23	DQ <3>	DQ <2>	24
25	D Out <1>	D Out <0>	26
27	GND	D Out <2>	28
29	D Out <4>	D Out <3>	30
31	D Out <6>	D Out <5>	32
33	D Out <7>	GND	34
35	Reset_b	P_Bus_A	36
37	TTC_Ready	P_Bus_B	38
39		GND	40
41	VCC	VCC	42
43	VCC	VCC	44
45	PECL_VCC	PECL_VCC	46
47			48
49			50

3.23.1.11 TTC dec card J2 Connector

Pin	Signal	Signal	Pin
1	Clk 40 Des 2	GND	2
3	GND	Clk 40 Des 1	4
5	Clk 40	GND	6
7	GND	B Cnt Str	8
9	Ev Cnt L Str	Ev Cnt H Str	10
11	Ev Cnt Reset	GND	12
13	B Cnt Reset	L1 Accept	14
15	Brcst Str 2	Brcst <4>	16
17	Brcst <5>	Brcst <6>	18
19	Brcst <7>	GND	20
21	B Cnt <0>	B Cnt <1>	22
23	B Cnt <2>	B Cnt <3>	24
25	B Cnt <4>	B Cnt <5>	26
27	GND	B Cnt <6>	28
29	B Cnt <7>	B Cnt <8>	30
31	B Cnt <9>	B Cnt <10>	32
33	B Cnt <11>	GND	34
35	Test Out/SDA	Serial B Channel	36
37	SCL	JTAGTRST	38
39	JTAGTDI	JTAGTMS	40
41	JTAGTDO	JTAGTCK	42
43			44
45	GND	GND	46
47			48
49			50

3.24 Manufacturing

An outside manufacturer will carry out the manufacture of the PCBs and the component assembly.

3.25 Testing

3.25.1 Test Strategy

Testing will be done in stages:
1. Test the ROD data transfer using LabView environment
2. System tests with software provided by the customer in the customers environment
3. System tests including data transfer to a single board computer
4. Test ROI transfer to level-2
5. Event buffer data processing

Tests one and two will include loading test patterns on to the DSS module and transmitting data on to the ROD module under the control of the ROC logic on the DSS module. The zero suppressed and formatted data from the ROD module will be received on the DSS module for verification.

The third test will include test two and also the transfer of data to the single board computer via the VME and off line analysis of the ‘event’ data.

Test four will require developing the firmware to handle the ROI format, however the same hardware will be used. This will be done at a later stage when the specification for the ROI format is written.
In the final system there will be one ROD design for transferring data to DAQ and transferring ROIs to level-2, with the appropriate firmware loaded on to the RODs handling the data to the appropriate destination.

Test five will also require development of firmware to carry out DSP type of applications.

A test plan will be provided at the FDR stage

3.25.2 Test equipment

(1) VME crate
(2) 32 bit VME interface
(3) Computer to run software
(4) Data Source and Sink module
(5) Logic analyser
(6) Oscilloscope
(7) TTC system (TTCvi, TTCvx, TTCrx)
(8) TCM from the demonstrator system
(9) VME Extenders

3.26 Software

A test engineer from the System Support Group will develop the LabView test software to carryout the initial standalone tests.
The test software for other tests will be required from the customer.

3.27 Installation

The ROD module is designed to be used in a 6U crate with VME J1 and J2 back plane. The module will be provided with a front panel containing sockets and monitoring LEDs. The module will most probably be a double width module to accommodate the G-Link receiver mezzanine cards. It will be triple width if rear PMC or the second S-link is in place.

3.28 Maintenance and further orders

This is a prototype module with an expected life span of no more than two years, hence there in no long-term maintenance requirement. Maximum of four ROD modules will be required.

4. Project Management

4.1 Personnel

		RAL Ext.	RAL Location
Customer:	C. N. P. Gee	6244	R1, 1.39
Project Manager:	V. Perera	5692	R68, 2.31
Project Engineer	J. Edwards	6814	R68, 2.09

4.2 Deliverables

4.2.1 To the Customer:

1. Four ROD Modules, and necessary firmware
2. Specification Document

4.2.2 From the Customer:

Test Software *, Powered VME crate (with J1 and J2 connectors) and a software platform to allow the test software to drive the ROD Module.

* see sections 3.25 and 3.26

4.3 Project plan (Milestones)

1. Preliminary Design Review (PDR)	Q1 1999
2. Final Design Review (FDR)	Q1 2000
3. Start Testing	Q3 2000
4. Concluding Review (CR)	

4.4 Design Reviews

The customer must be present at the PDR and the CR. If the customer wishes, he may attend the FDR.
The progress of the project will be reported on a monthly basis in the ATLAS Calorimeter First-level Trigger project monitor form.

4.5 Training

Training will be carried out as required on the job.

4.6 CAE

Cadence for schematic capture, VHDL and FPGA design tools and LabView for test software.

4.7 Costs and finance

All manufacturing, assembly and component costs will be charged to FK40000.

4.8 Intellectual Property Rights (IPR) and Confidentiality

All background and foreground Intellectual Property Rights in this project will remain with CLRC. The customer will have unrestricted rights to items listed under deliverables (4.2). If the customer requires other data, then an appropriate protective agreement should be in place before releasing such data.

4.9 Safety

General laboratory safety codes apply.

4.10 Environmental impact

4.10.1 Disposal

RAL will dispose of the modules at end of their life.

4.10.2 EMC

Since these modules are prototypes, they will be outside the scope of the EMC regulations. However since the electronics must function as designed, without malfunction or unacceptable degradation of performance due to electromagnetic interference (EMI) within their intended operational environment, the electronics shall comply with specifications intended to ensure electromagnetic compatibility.

4.11 Handling Precautions

Anti-static precautions must be taken when handling the module to prevent damage to expensive components.