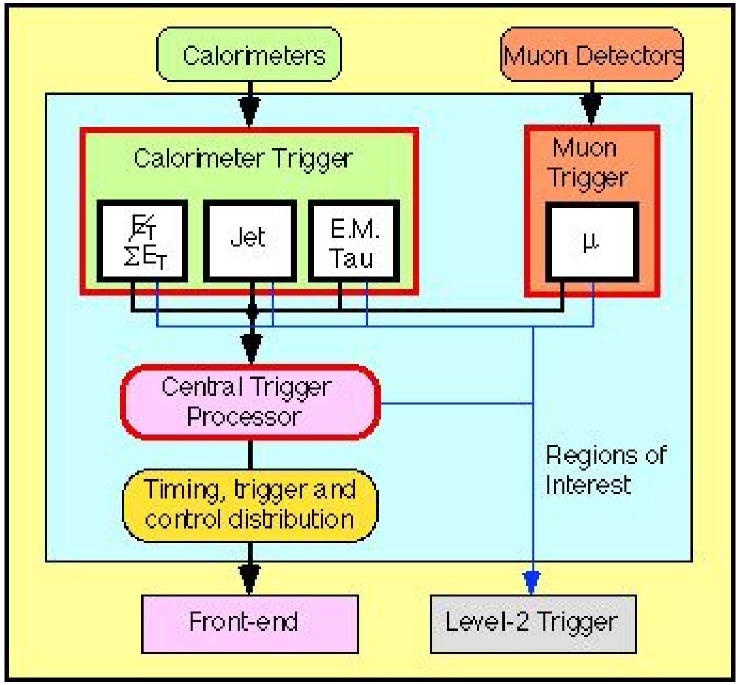
# "One Size Fits All": Multiple Uses of Common Modules in the ATLAS Level-1 Calorimeter Trigger

- Introduction
- The Level-1 Calorimeter Trigger
- Counting e/γ clusters, τ/hadron clusters and jets
- $E_T$ summation
- CMM architecture
- The common backplane
- Other common modules: TCM, CP/JEP ROD
- Status
- Conclusions

# The ATLAS Level-1 Calorimeter Trigger (1)

Calorimeter trigger objects:

- Multiplicity of e/γ
- Multiplicity of τ/hadrons
- Multiplicity of jets
- Multiplicity of forward jets
- Total $E_T$
- Missing $E_T$
- Total jet $E_T$

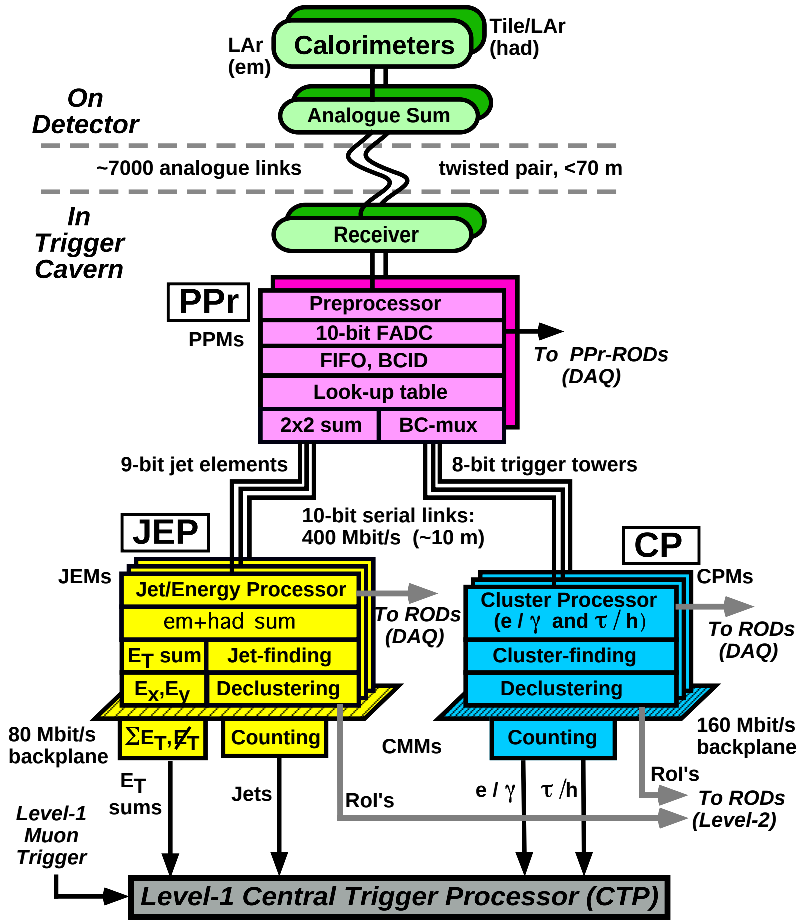


# Level-1 Calorimeter Trigger Architecture

Pre-Processor

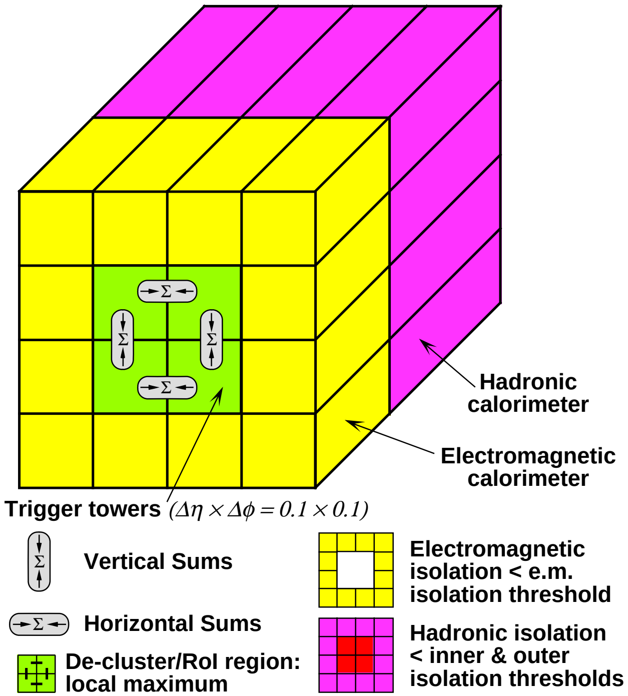
Jet / Energy Processor

Cluster Processor



# Cluster Algorithm Diagrams

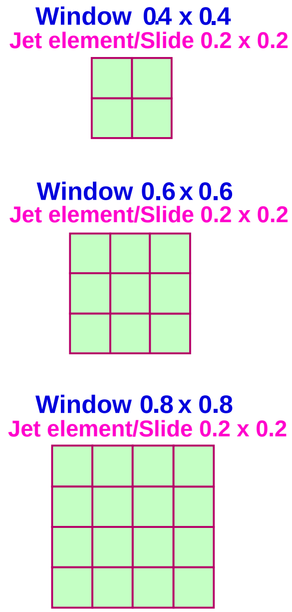
## Electron/photon Algorithm




*Tau/hadron algorithm adds 1x2/2x1 e.m. clusters to 2x2 inner hadronic region. Isolation uses e.m. and outer hadronic 'rings'.*

## Jet Algorithm

**Programmable choice of jet window sizes**



# Hit Merging (1)

Cluster Processing Module:

- Examines area of calorimeter: 1 quadrant in $\phi \times \sim 0.4\ \Delta\eta$
- Looks for isolated energy clusters passing 16 thresholds
- Results = 3-bit multiplicity $\times$ 16 threshold sets $\times$ 14 modules $\times$ 4 crates
- Hit merging $\rightarrow$ 3 bits $\times$ 16 threshold sets $\rightarrow$ CTP

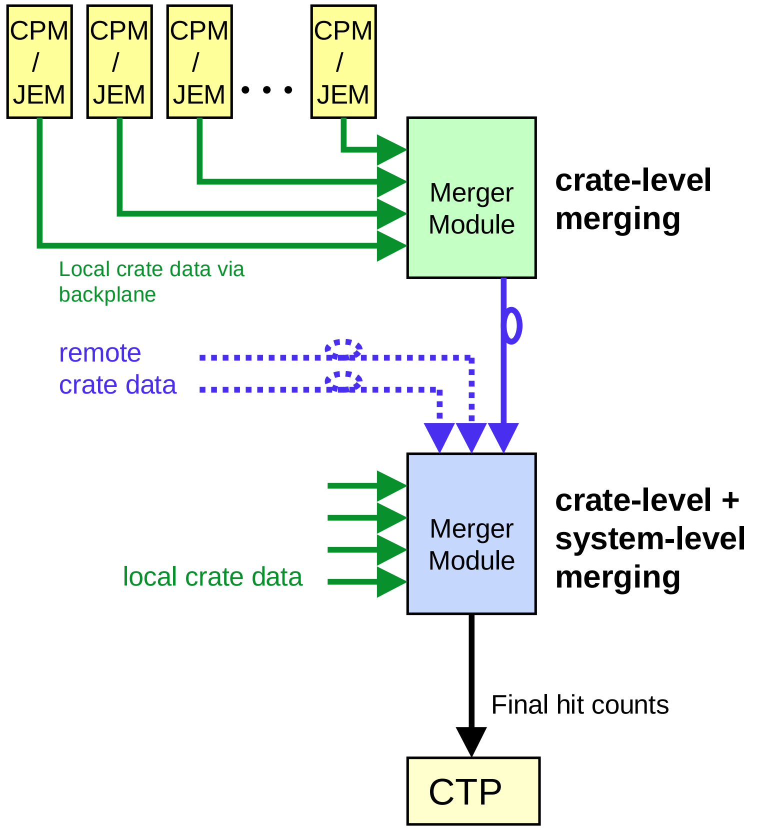
Jet/Energy Module:

- Examines area of calorimeter: 1 quadrant $\phi \times \sim 0.8\ \Delta\eta$
- Looks for energy clusters passing 8 thresholds
- Results = 3-bit multiplicity $\times$ 8 thresholds $\times$ 16 modules $\times$ 2 crates
- Hit merging $\rightarrow$ 3 bits $\times$ 8 thresholds $\rightarrow$ CTP

- Merging algorithms the same
- Tasks differ only in quantity of data to be merged

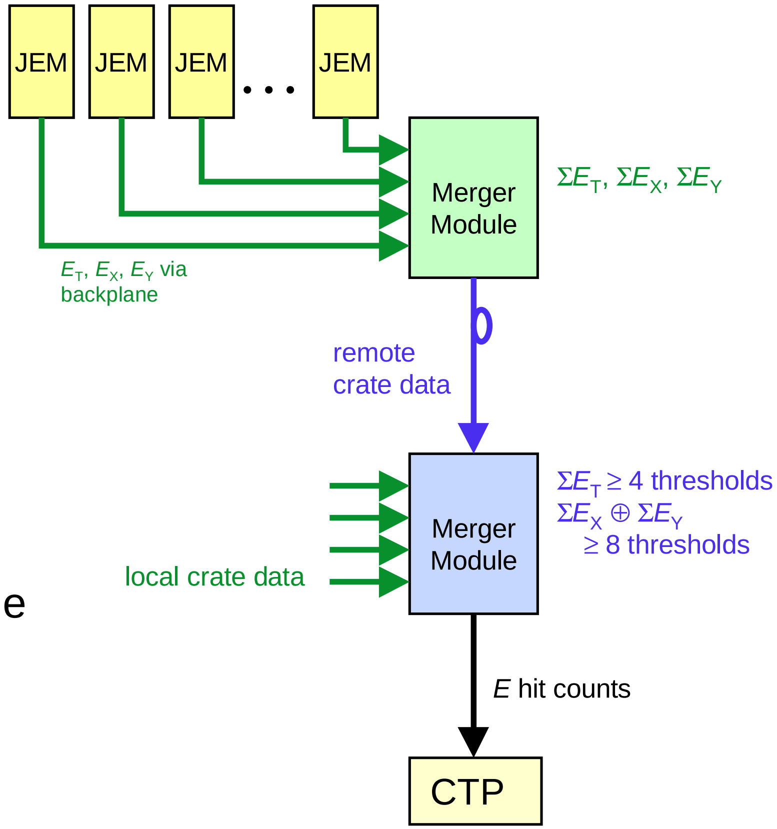
# Hit Merging (2)

- Original, TDR proposal:
  - CP: merging in remote crate
  - JEP: local crate merging followed by system-level merging
- Now adopted JEP approach for CP:
  - Reduces cable links
  - Allows common merger module & backplane
  - Large no. of LONG SINGLE-ENDED backplane links tested with Cadence simulation
- 2 CMMs per crate, each processing data for 8 thresholds
- Single design performs crate-level and system-level summing
  - System logic only used in final module in tree
  - Reduces design effort

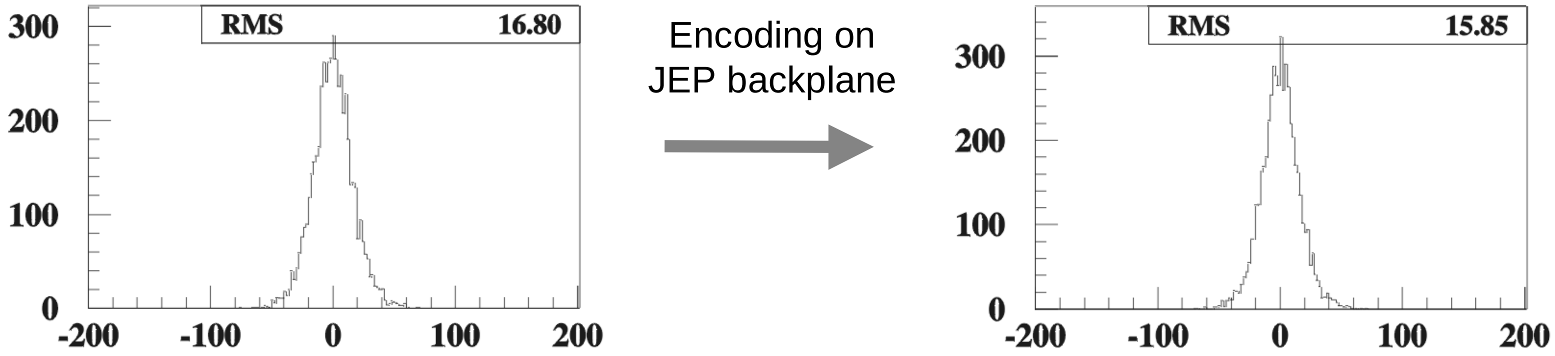


# Energy Summation

- Total $E_T$ trigger:
  - Sum $E_T$ over crate + system
  - Compare with 4 thresholds
- Missing $E_T$ trigger:
  - Sum $E_X$ & $E_Y$ over crate + system
  - Vector sum $E_X \oplus E_Y$
  - Compare with 8 thresholds
- Compared to hit counting require...
  - Additional functionality (LUTs)
  - Greater volume of data
- TDR had separate energy merger module
- Number of input pins very high:
  3 ($E_T$, $E_X$, $E_Y$) × 12 bits × 16 JEMs = 576 bits.
  (c.f. hit counts = 3 × 8 × 16 = 384 bits)
- Encode data to reduce volume



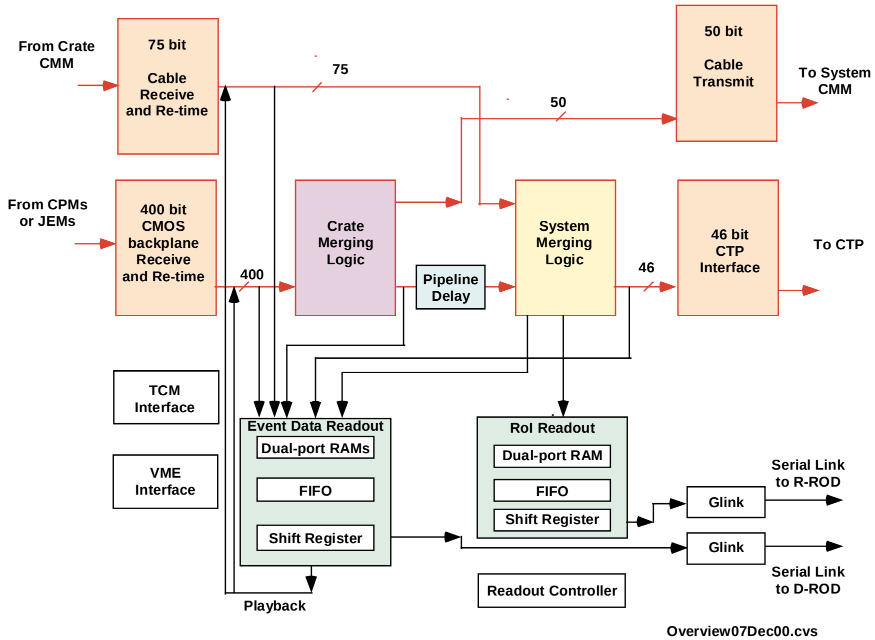
# Energy Summation: Resolution



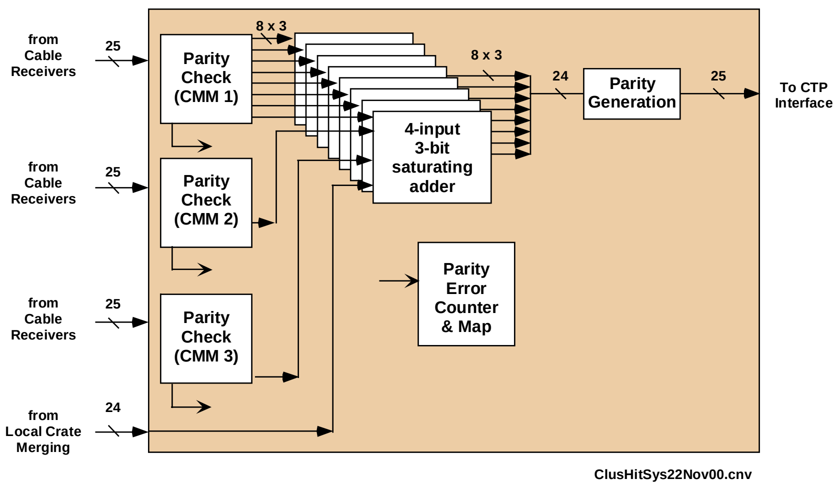

- Encoding scheme: 6 data bits + 2 scale bits
  - according to scale bits, data multiplied by 1, 4, 16 or 64
  - multiplication performed by bit-shifting
  - low latency
- Used Level-1 simulation with ATLFAST and QCD 2-Jet events from PYTHIA to evaluate resolution of encoding data over JEP backplane
- No significant degradation of energy resolution or trigger performance

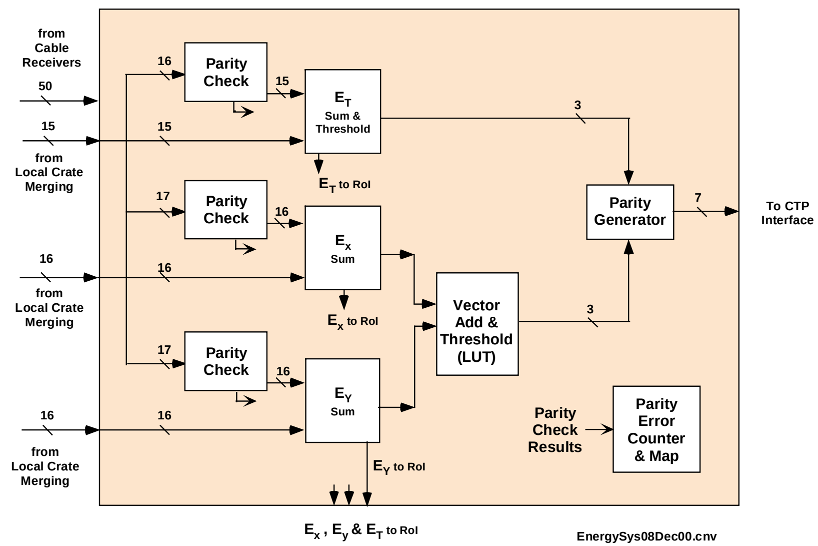
# The Common Merger Module

- Crate logic and system logic implemented in FPGAs
  - Gate counts comparable to ASICs
  - Avoid NRE costs
  - Increased flexibility
- Bulk of logic implemented in two XCV1000E devices:
  - ~1.5 million gates
  - 96 × 4kbit block RAM
  - User IO = 660 pins (fine-pitch BGA)
- Crate logic: large pin count required
- System logic: large number of LUTs required
- Flash memories contain all configurations
- CMM configured to required type according to geographical address & crate no.



# Hit Counting & Energy Summation Logic



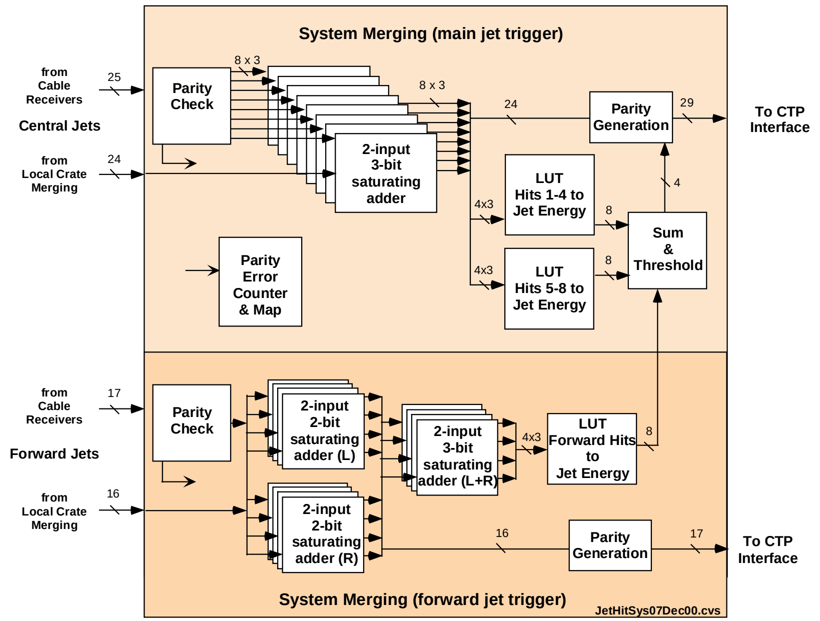




- e/γ & τ /hadron cluster counting, system-level logic
- Energy summation, system-level logic

(FPGAs also contain readout logic)

# New Trigger Algorithms

- Flexibility of CMM has enabled new trigger algorithms to be developed:
  - Forward jets
  - Approximate total jet $E_T$
  - Total $E_T$ exceeding local thresholds
- Spare capacity in
  - FPGA logic (~40%)
  - CMM–CMM IO
    (42 bits used; 8 spare)
- Other algorithms may be added later




- Forward jet trigger:
  - Not in TDR proposal
  - Interesting physics
    (EW symmetry breaking)
  - Algorithm added to JEP CMM

# The Common Backplane (1)

- CP and JEP backplanes functionally very similar:
  - Serial cable links from the Pre-Processor system (PPR) → CPM/JEM
  - Data fan-in/out between neighbouring CPMs/JEMs
  - Data from CPM/JEM → CMM
  - TTC, CPU, DCS (CANbus)
- Differences:

CP:

- 14 CPMs,
- Input from PPR = 80 serial links via 20 cable assemblies
- CPMs → CMMs: 700 single-ended point-to-point links @ 40 MHz
- Fan-in/out = 320 single-ended point-to-point links @ 160 MHz

JEP:

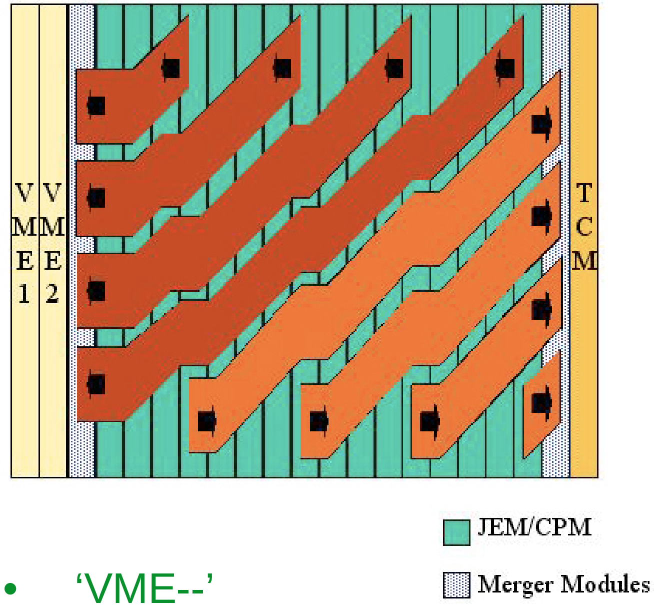
- 16 JEMs,
- Input from PPR = 88 serial links via 24 cable assemblies
- JEMs -> CMMs: 800 single-ended point-to-point links @ 40 MHz
- Fan-in/out = 330 single-ended point-to-point links @ 80 MHz

- Except for speed, CP requirements are subset of JEP requirements

# The Common Backplane (2)

- Feasibility of using 800 single-ended long links across 16 slots @ 40 MHz proved using Cadence simulation

- 9U high (400.05 mm)
- Space for 21 modules
- 820 pins per module
- AMP Z-pack connectors used
  - 5 rows of pins
  - 2 mm pitch
- 4 signal : 3 ground ratio
- Full VME bus cannot be accommodated; use custom bus...



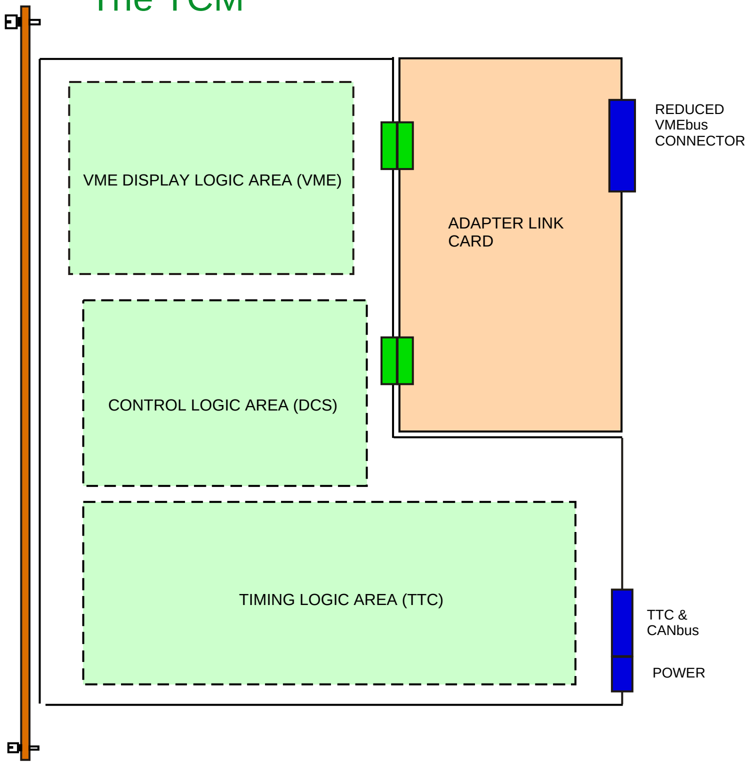

- 'VME--'
  - SYSRESET
  - A[23:1]
  - D[15:0]
  - DS0*
  - WRITE*
  - DTACK*

# Other Common Modules: TCM & ROD

Timing Control Module (TCM)

- Functions:
  - Houses TTCrx; fans out electrical TTC signals for crate
  - CAN interface for crate to DCS
  - Display VME activity
- Used in JEP, CP and Preprocessor subsystems, 1 per crate
- Adapter Link Card overcomes difference in VME format between Preprocessor and JEP/CP crates

The TCM




JEP/CP ROD:

- See talk by Gilles Mahout

# Status and Testing

- Common Merger Module and Common Backplane in final stages of design process.
- TCM currently undergoing stand-alone tests.

- Slice tests in Heidelberg Spring 2002 will provide opportunity to test
  - CMM and backplane in both JEP and CP systems
  - ROD in both JEP and CP systems
  - TCM in all three subsystems

# Conclusion

- Common modules can provide savings in design effort
- Advances in FPGA technology have allowed modules to be more flexible
- Common Backplane and CMM have enabled new triggers to be developed
- Future development of new triggers is possible due to flexibility and spare capacity built into all modules.

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