Prototype Readout Module for the ATLAS Level-1 Calorimeter Trigger Processors

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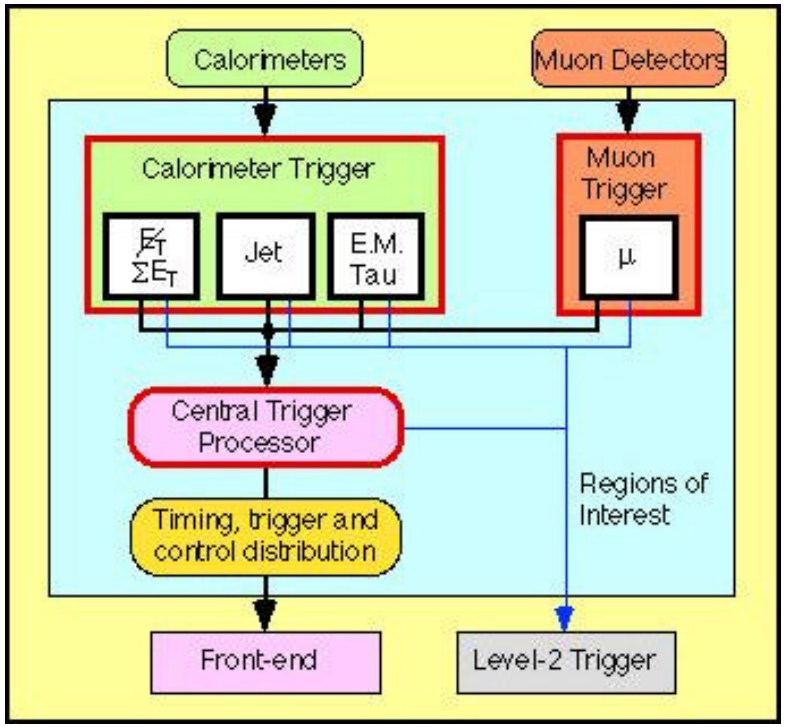
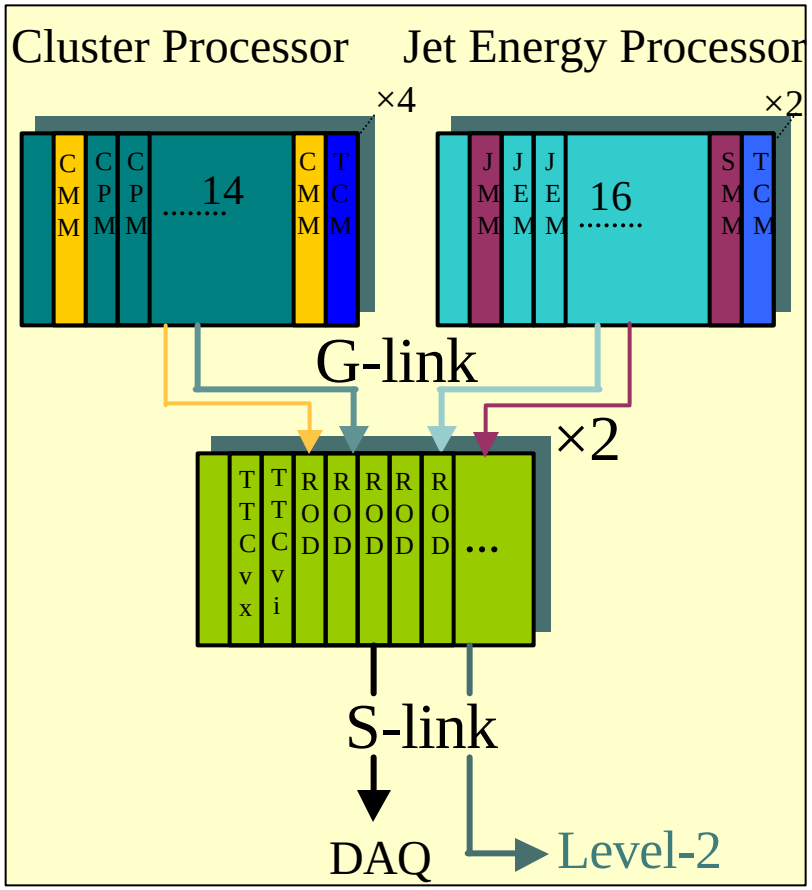
ATLAS Level-1 Calorimeter Trigger System

- **Level -1 Trigger Requirements**
  - Provide trigger multiplicity information to the CTP:
    - e/gamma and tau/hadron
    - jets
    - missing and total Et
    - Jet-Et
  - Provide Region of Interest (RoI) information to the Level-2 trigger system
  - Time slice data for monitoring and diagnostics



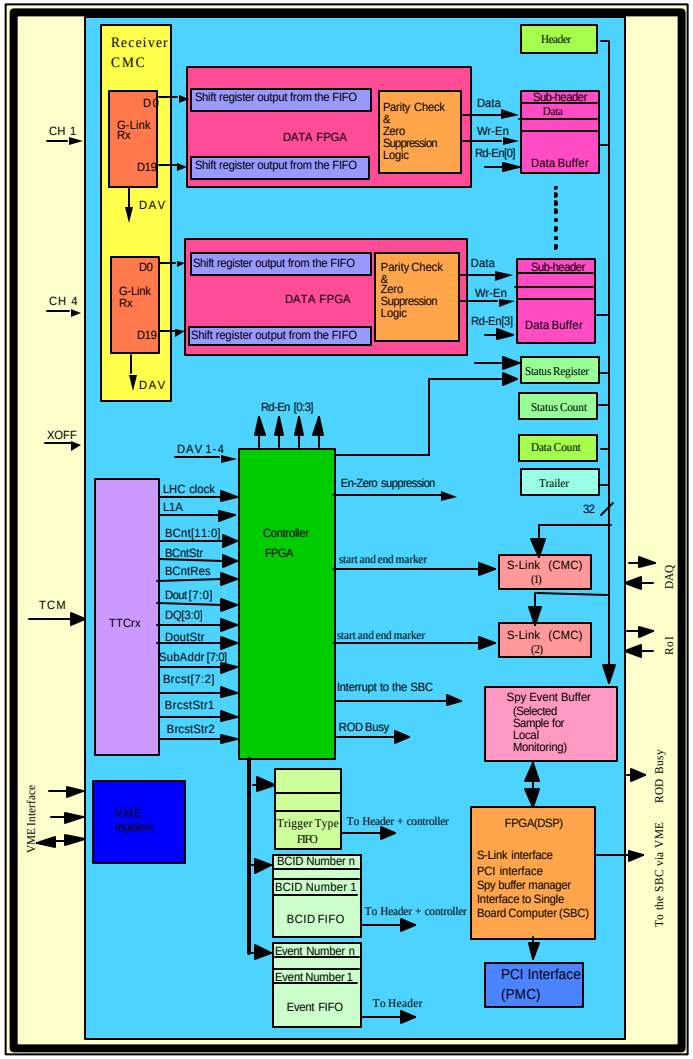
Prototype Readout Module for the ATLAS Level-1 Calorimeter Trigger Processor

- **Readout Driver (ROD) Requirements**
  - **Collect data from Cluster Processor (CP) and Jet Energy (JE) Processor via HP G-links**
  - **Data processing (zero suppressed or not)**
  - **Error detection**
  - **Merge and format event data**
  - **Interface to the readout link (S-link)**
  - **Local Monitoring of Data**
  - **Receive TTC signals**
  - **Interface to CTP (ROD Busy)**
  - **Operate at level-1 accept rate (75 kHz)**



Prototype ROD Functions

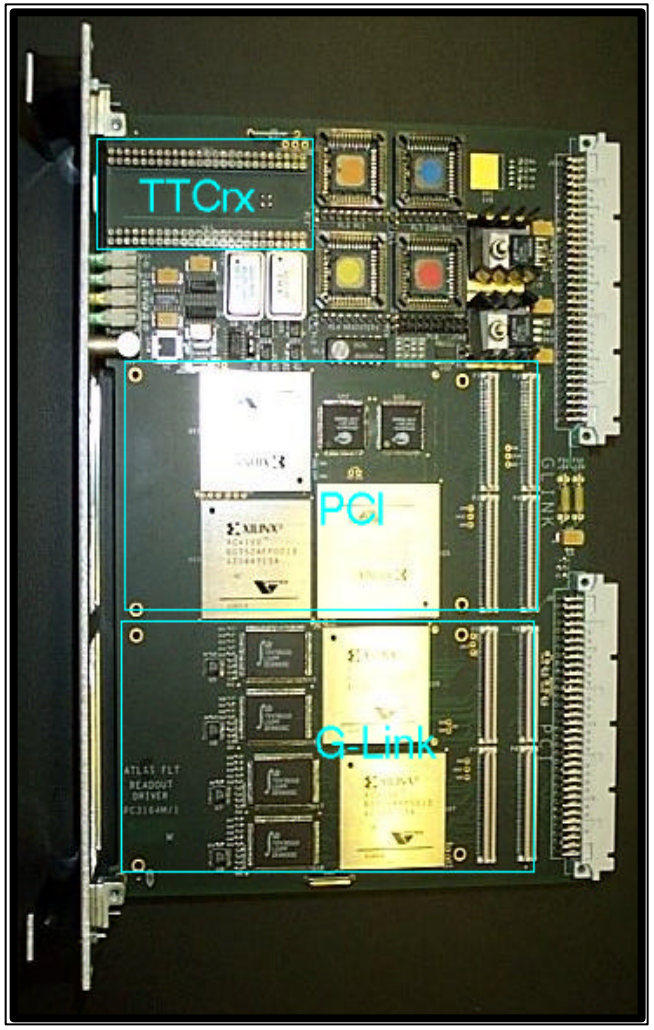
- 4-channel (= 4 processor modules) prototype, 18 channels for the final version:
  - G-Link (HDMP-1024) Receiver
- Data FPGA:
  - Perform Zero suppression
  - Perform Parity Check
- Buffer Data in Fifos
- Controller FPGA:
  - Control G-link access
  - Merge and format Data
  - Transfer using S-Link
- Interface to TTC
- 'Spy Event Buffer' for local Monitoring
  - FPGA based buffer manager
    - > Can provide PCI interface
    - > Can implement DSP core



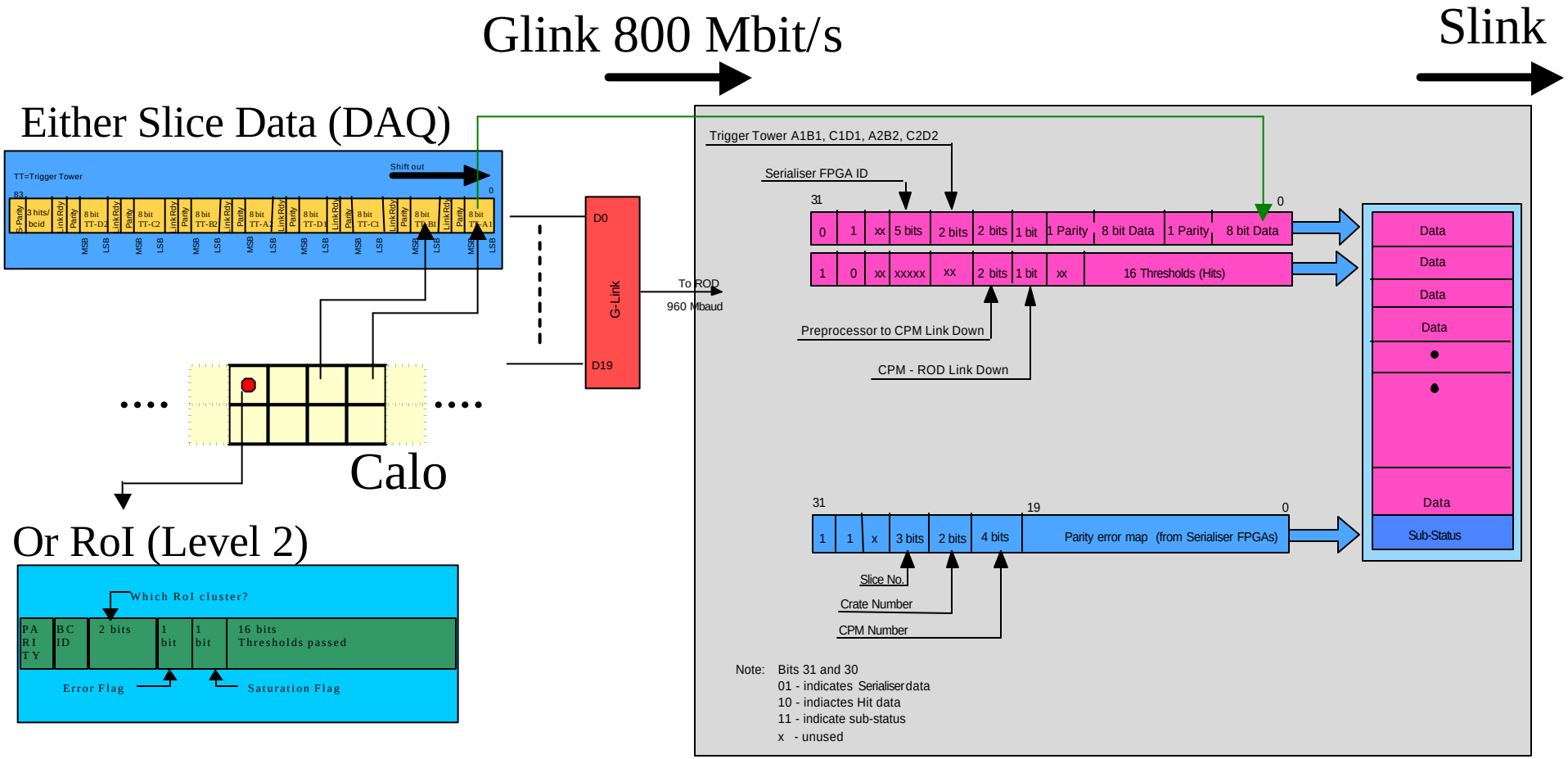
Prototype ROD Implementation

- Triple width 6U VME
- Four Common Mezzanine card (CMC) positions
  - Receive data via G-Link CMC daughter card (from 4 processor modules)
  - Two S-Link Positions for Slice Data or RoI Data
  - One position for a commercial PMC co-processor card
- All processing and data handling carried out by FPGAs
- Flexible design: same module, via different firmwares, will handle:
  - CP RoIs
  - JEP RoIs
  - CP Multiplicity
  - JEP Energy Slice
  - CP Slice Data
  - JEP Slice Data
  - JEP Multiplicity
  - JEP Energy RoIs
- Commercial S-Link card to transfer data out
- Spy on events for monitoring
  - Buffer four events
  - Data available for a PCI Mezzanine Card
- TTCdec (clock and command) card to interface to TTC system

Prototype ROD module for CP/JEP



DATA Format of the ROD



ROD DATA Output Format

- Standard ATLAS format for Events transmitted to DAQ or Level 2 via S-Link
- Copy to spy buffer

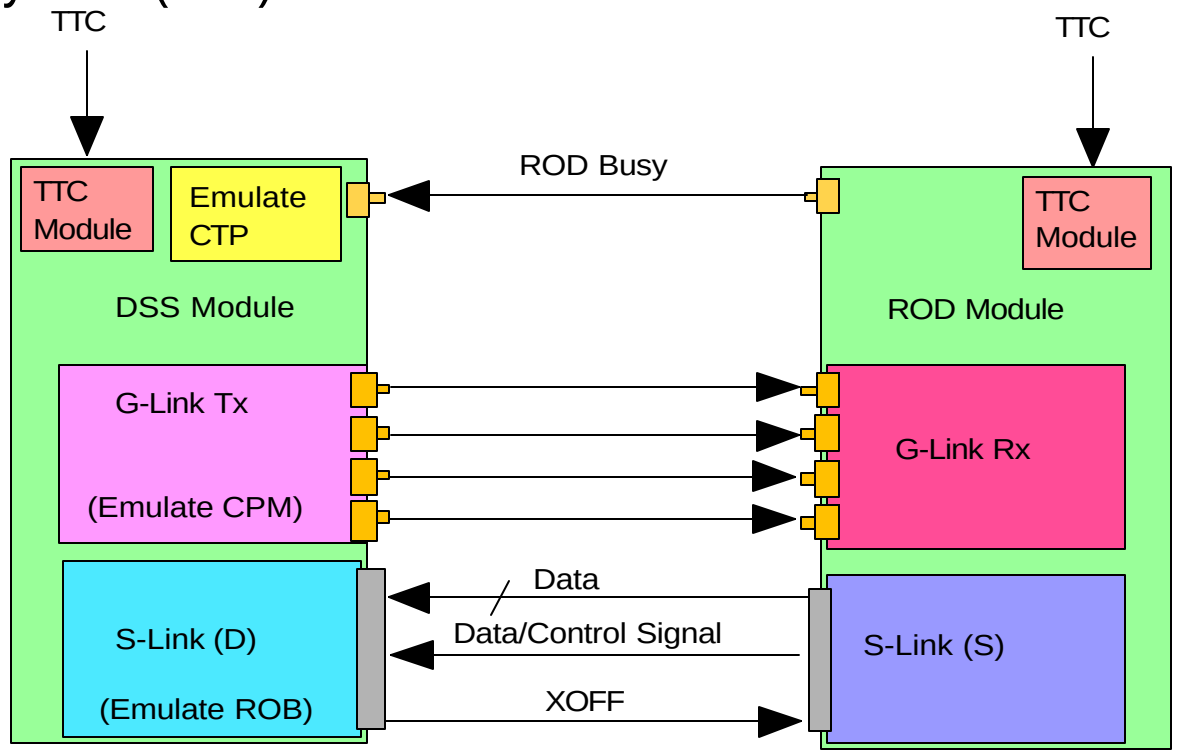
Content	Type
Begin of Fragment (B0F00000 Hex)	Control
Start of Header Marker (EEEEEEEE Hex)	Data
Header Size (0008 Hex - number of words in the header excluding control word)	Data
Format Version Number	Data
Source_ID - four byte field: [71][Crate ID][Module type][Module ID]	Data
ROD_L1ID (24 bit event)	Data
ROD_BCID (12 bit BCID)	Data
Leve1 Trigger Type	Data
Detector Specific Event Type (00000000)	Data
Data Words (from Data Buffers)	Data
Status Word-1	Data
Status Word-2	Data
Status Summary [31:16]/ Number of Status elements [15:0]	Data
Number of data elements	Data
Status block position	Data
End of Fragment (E0F00000 Hex)	Control

BCID, EVENTID { ROD_L1ID (24 bit event), ROD_BCID (12 bit BCID)

{ Data Words (from Data Buffers), Status Word-1, Status Word-2 — RoI or DAQ data

First prototype ROD tests

- Test Set-up
  - Lab set-up using a Data Source and Sink (DSS) module
  - DSS emulates CP Module (source), RoI-Builder or ReadOut Subsystem (sink)



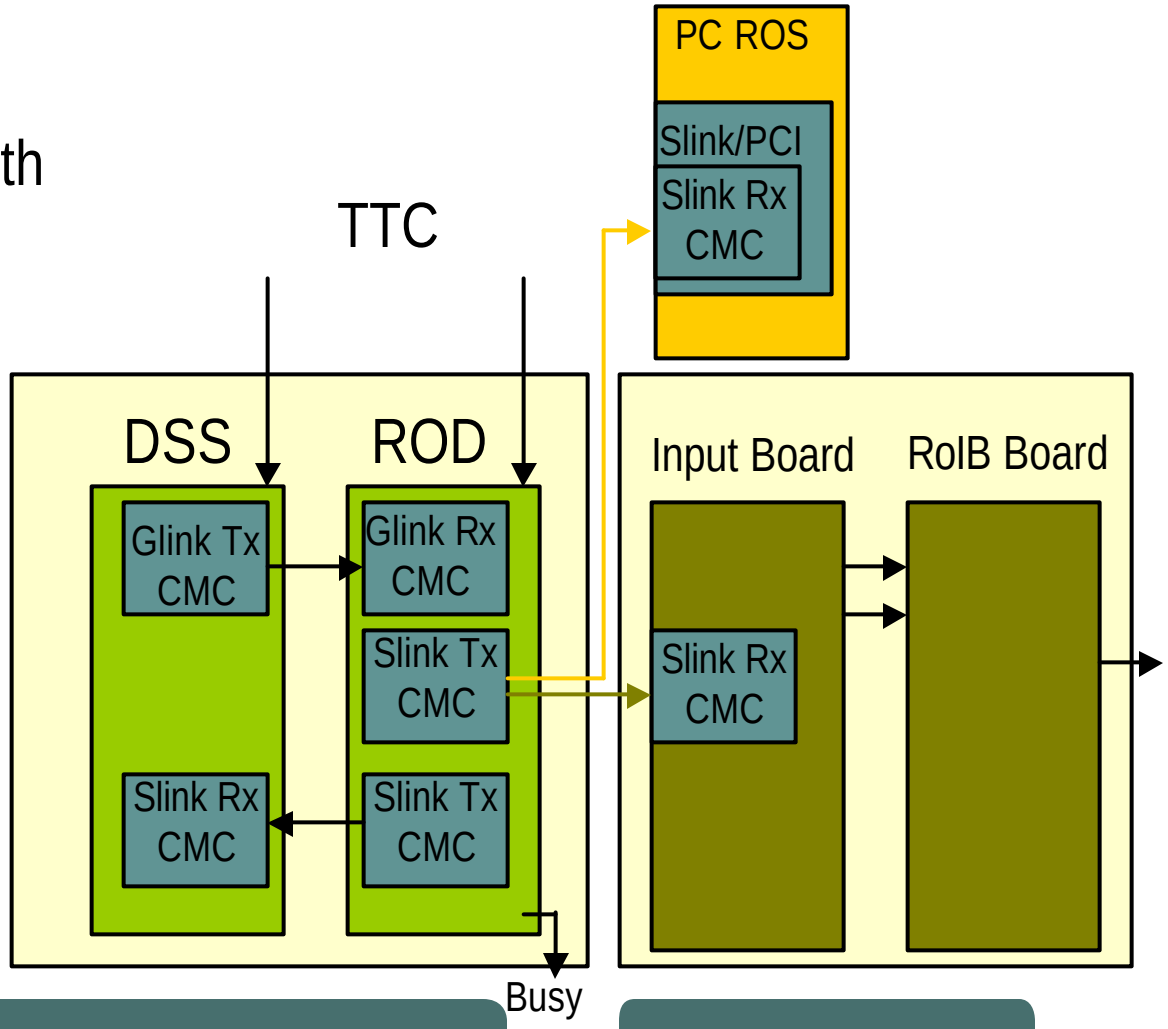
Local Test set up

Stand alone Test Results

- DSS Firmware set for RoI (22 bits data as input)
- TTC system distributes burst of L1A: 
- Events sent from the DSS, processed in ROD and sent back to DSS
- Events recovered and checked via S/W
- Bunch Crossing Number not checked but different data for each event of a burst
- Results:
  - Event ID increments correctly
  - Overnight test : no errors with frequencies beyond 100kHz
  - Single Slice data per event transmitted correctly

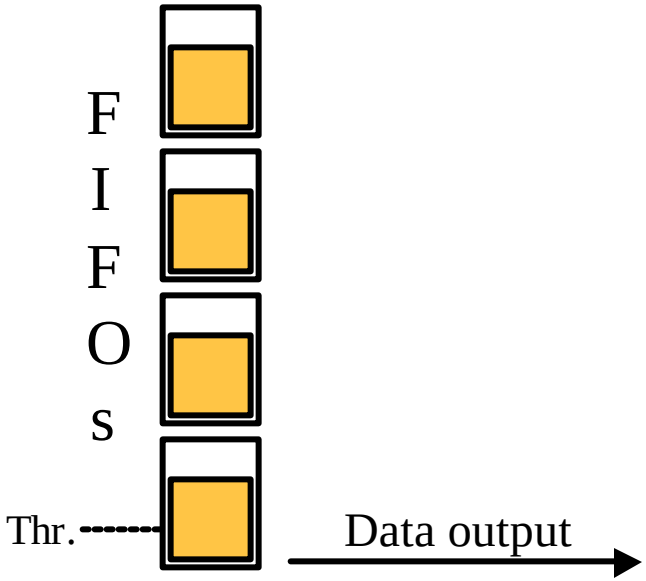
Integration tests at CERN

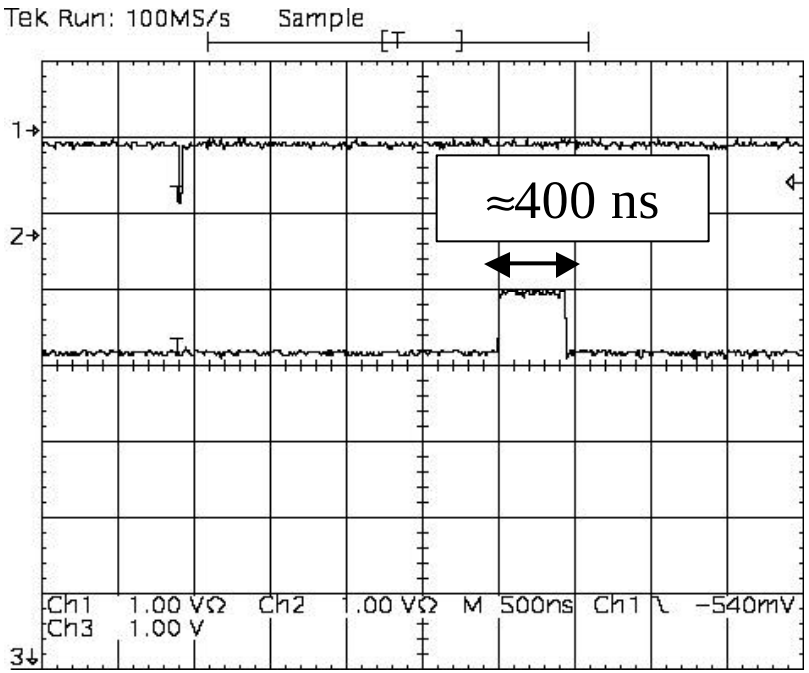
- Prototype ROD integrated with the RoIB and the ROS:
  - ROD busy study
  - Latency measurement
  - Long run test at low rate
- Slink flavour
  - CERN electrical
  - ODIN S-link
  - ANL:Argonne National Laboratory



Operation of the ROD Busy

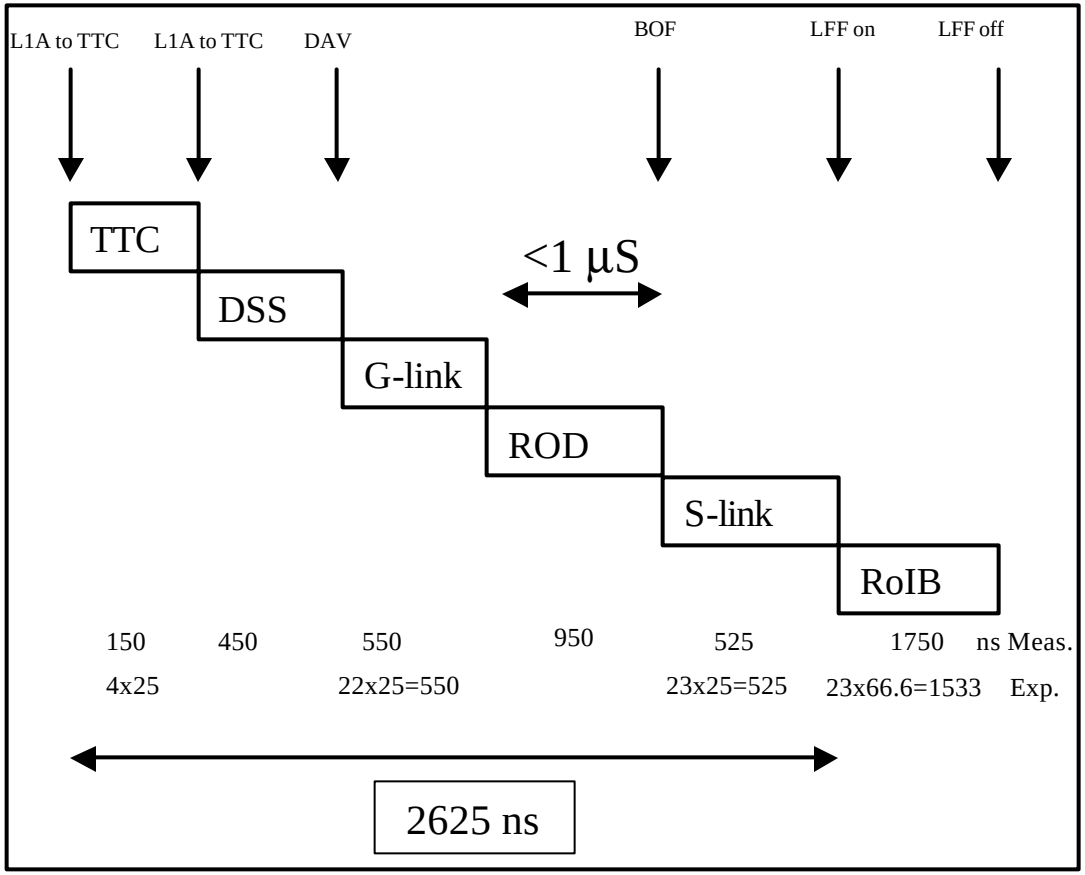
- Busy signal: inhibit CTP when FIFOs nearly full
- Busy threshold set to low value to check ROD performance:
  - 4 FIFOs filled with 4 RoIs each
  - threshold set to 3: τ_{busy}=325 ns

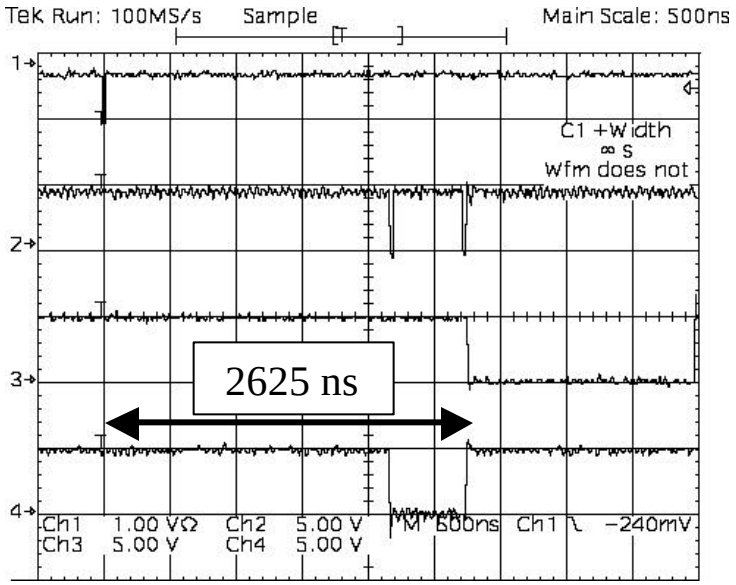




Latency measurement with RoIB

- 8 RoIs, From L1A to RoIB: 2625 ns





Combined run

- With the ROS front-end only
  - Events transmitted and checked up to 20 kHz in continuous mode
  - Up to 660kHz in burst mode
- Tests with the RoIB and ROS
  - 2 M events in burst transmitted with no errors
  - Firmware updated
  - ROD could drive two different outputs in parallel!

Conclusion

- ROD prototype shows feasibility of “one size fits all” concept
- Flexible design , RoI or Slice data readout, works successfully
  - RoI and slice data correctly transmitted
  - RoI data transmitted beyond Level-1 Accept trigger rate
- Integration tests have given good results but still need better understanding of the LVL1-LVL2 interface
- Firmware updated , no H/W problem
- Next steps:
  - Firmware variances
  - Soak tests
  - Complete testing with LVL1 modules, then RoIb and ROS
  - Complete 9U design (18-channel) for the final production next year.