

Level-1 Calorimeter Trigger

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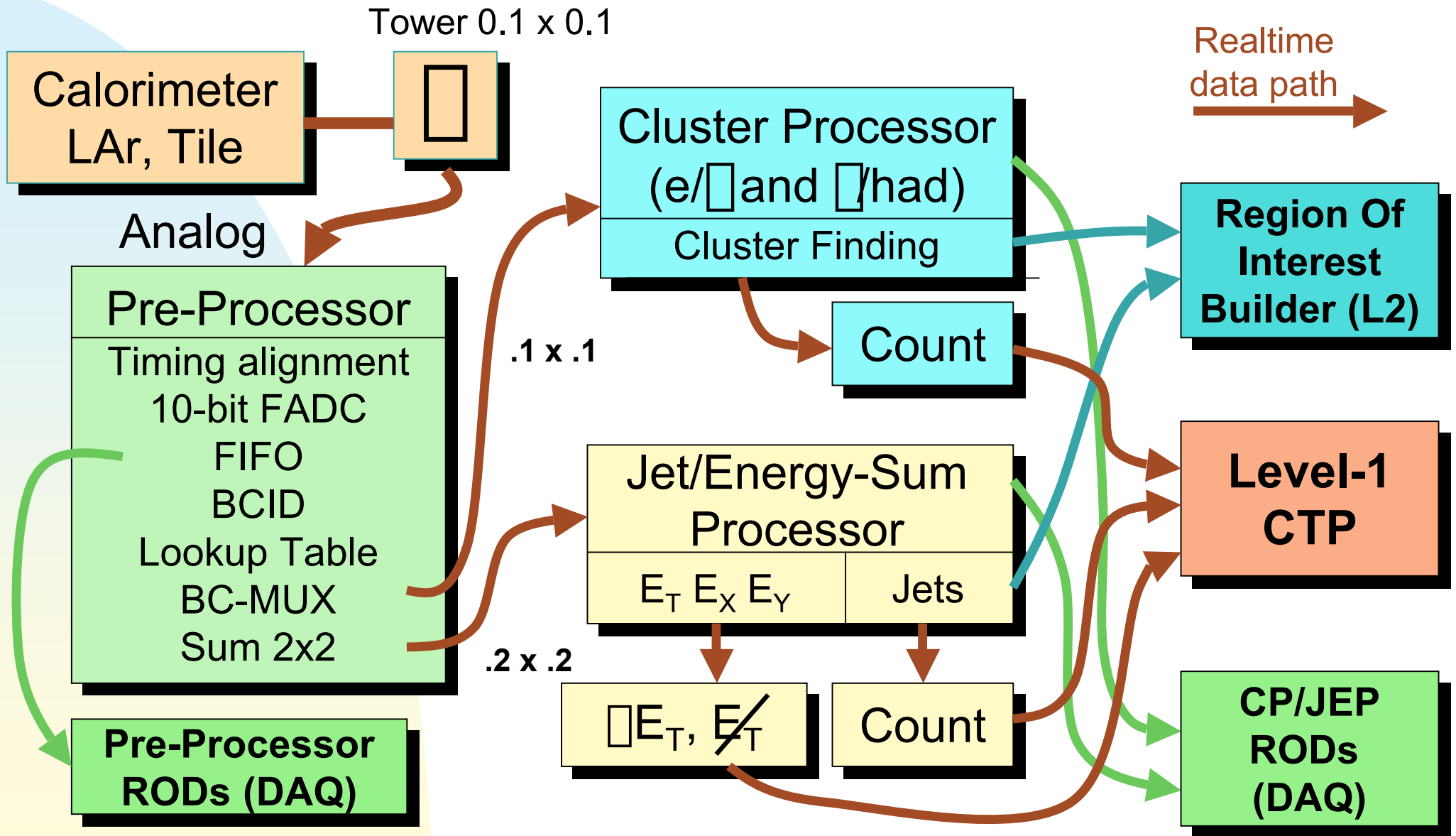
on behalf of

Birmingham, Heidelberg, Mainz,

Queen Mary (London), Rutherford, Stockholm

- Overview of trigger architecture
- Project status
- Pre-Processor
- e/□ Cluster Processor
- Jet/Energy-Sum Processor
- ROD prototype
- Software
- “Full-slice” tests
- Summary, Outlook

Overview of the trigger

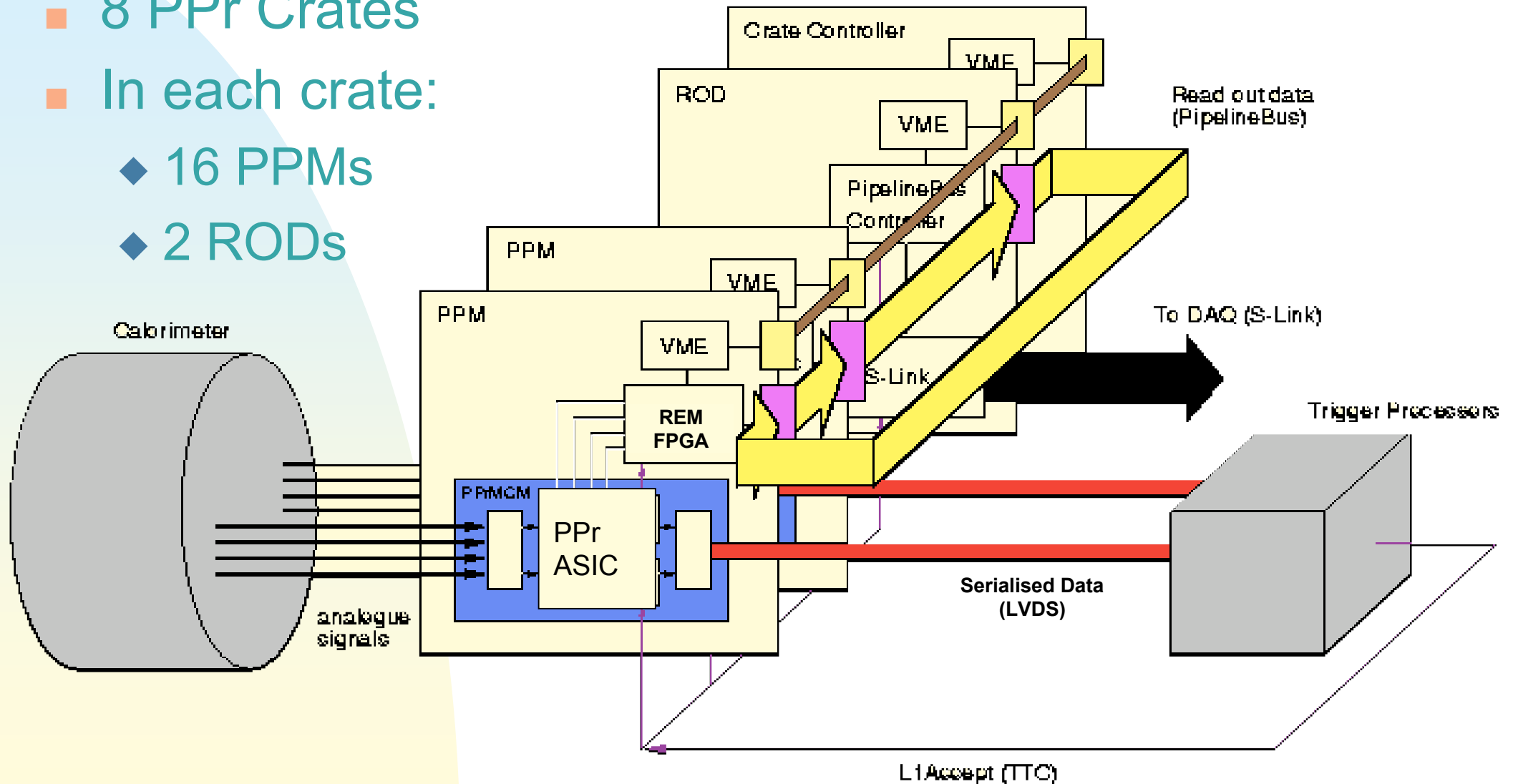


Project Status

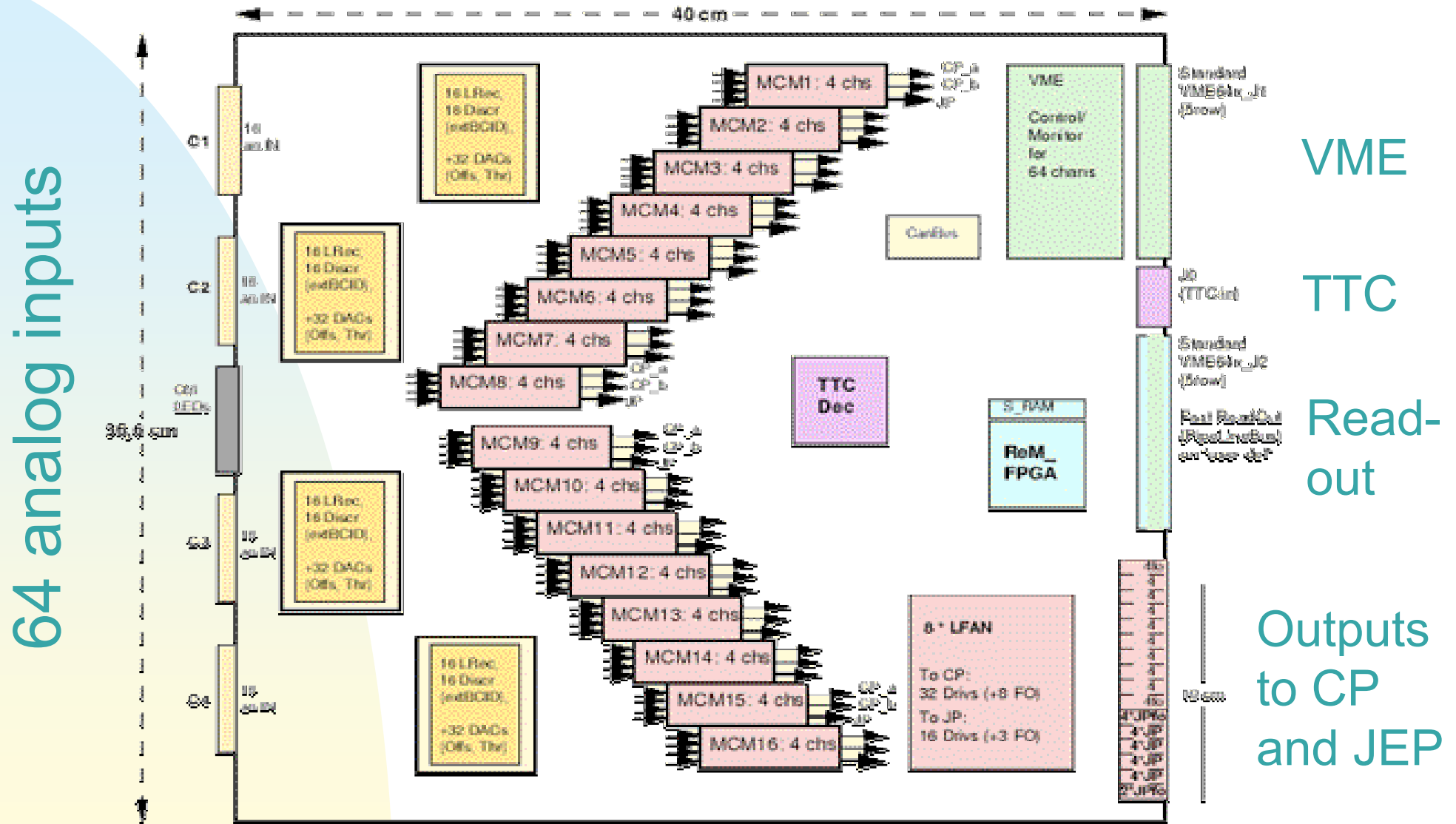
- Design reviews completed for prototype components “to Module-0 specifications”
- Most prototypes have been produced, remainder in advanced stages of design
- Hardware testing/integration and software development are main current activities
- Goal of present stage: complete “slice test” through Level-1 calorimeter trigger, from input signals to CTP

Pre-Processor sub-system

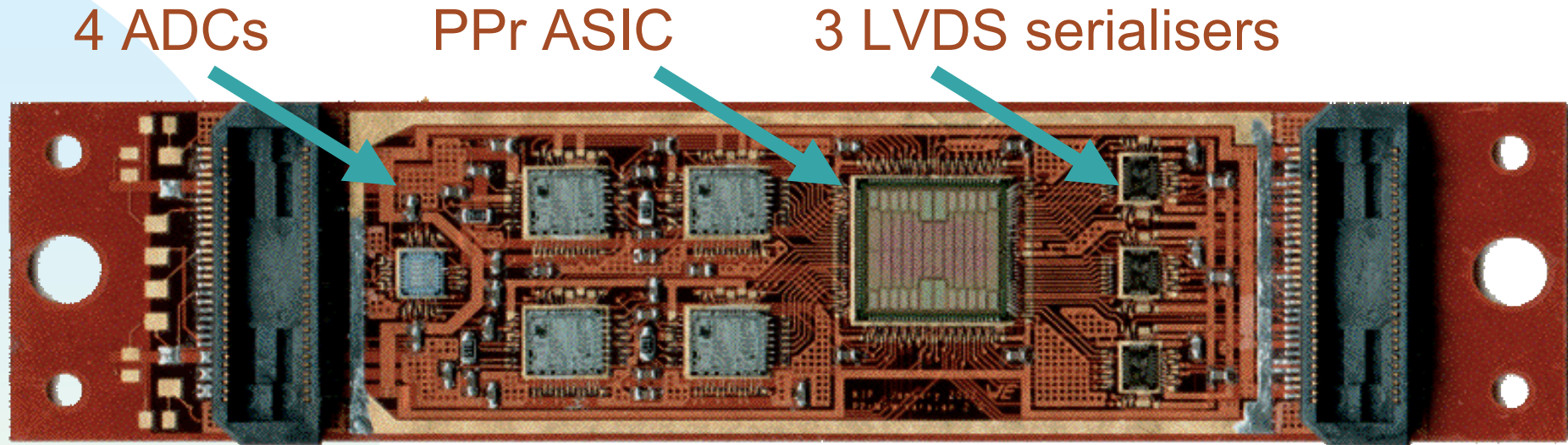
- 8 PPr Crates
- In each crate:
 - ◆ 16 PPMs
 - ◆ 2 RODs



PreProcessor Module

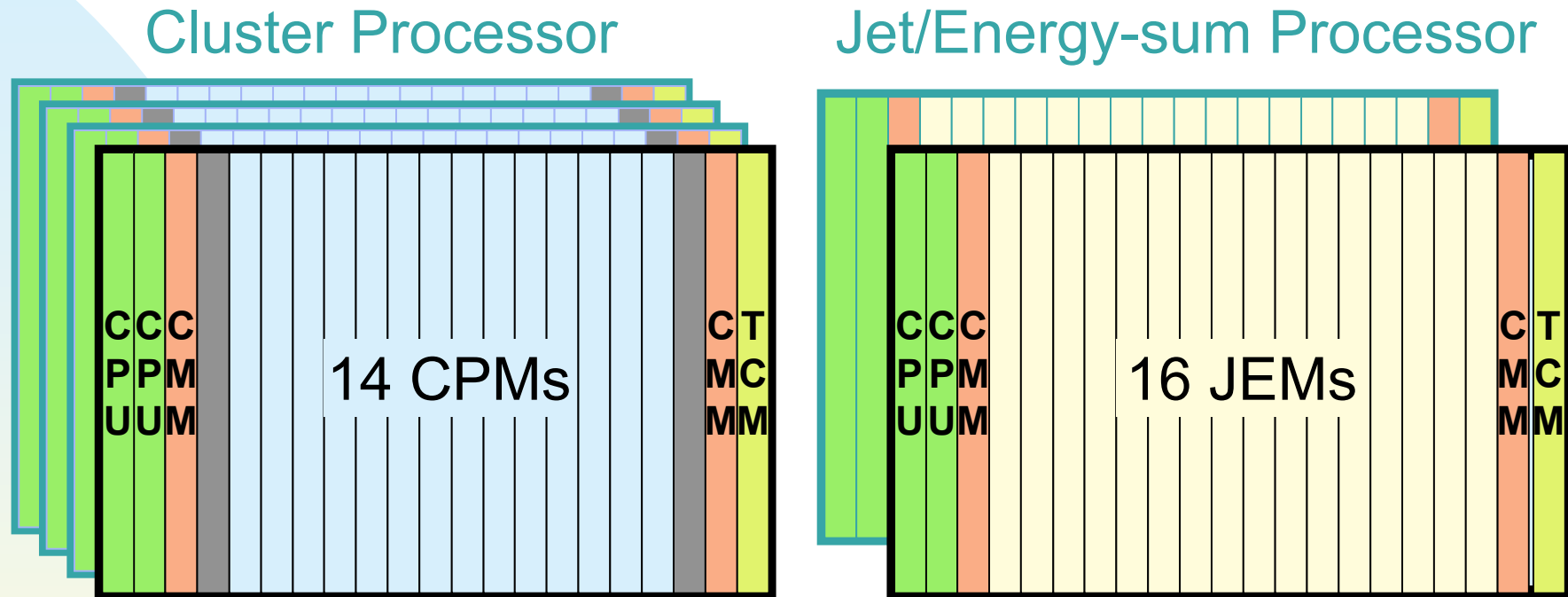


PreProcessor MCM



- ASICs produced in slice-test quantities (200 individual dies, 2 wafers with 200 dies/each)
- 2 MCMs soldered and bonded for tests
- Hardware for quantity testing nearly completed

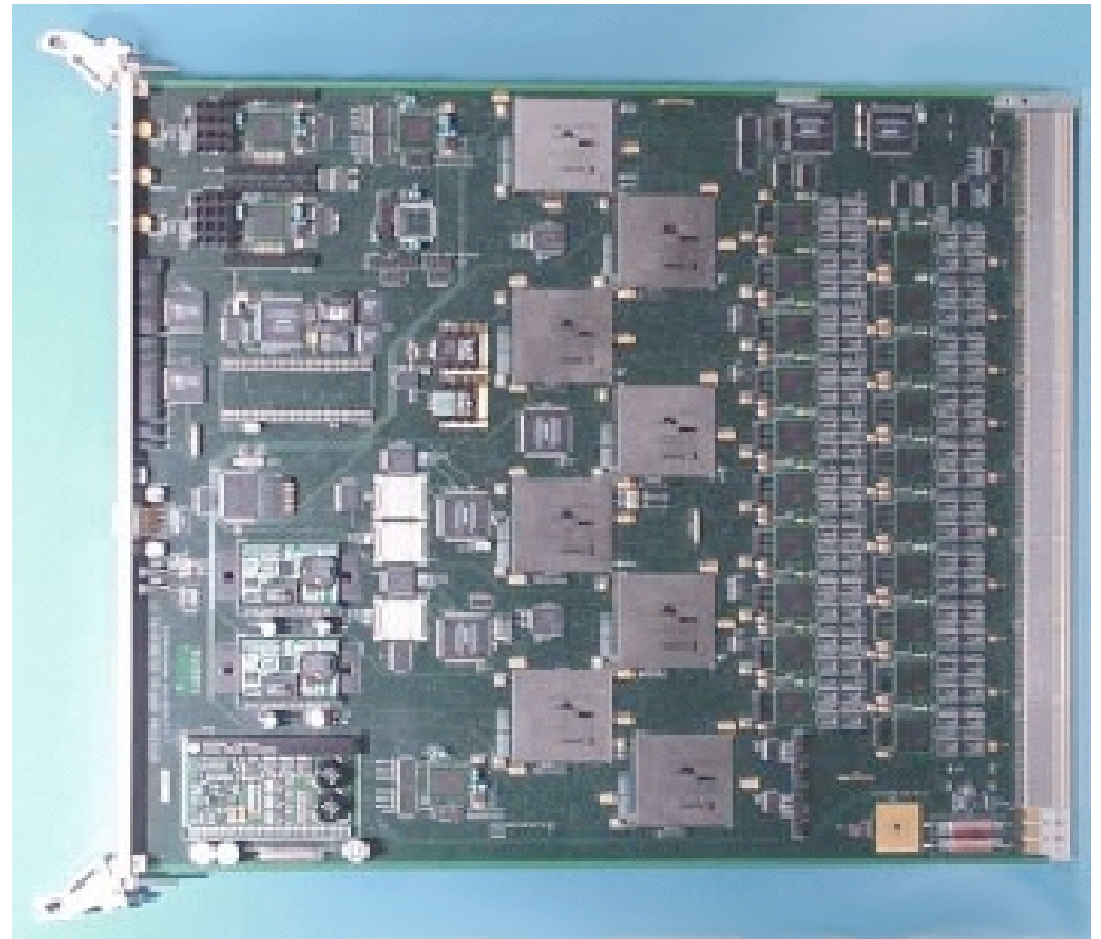
Cluster Processor and Jet/Energy-sum subsystems



- Systems have common architectures
- Most components common: backplane, data merging modules, timing/control module, CPU

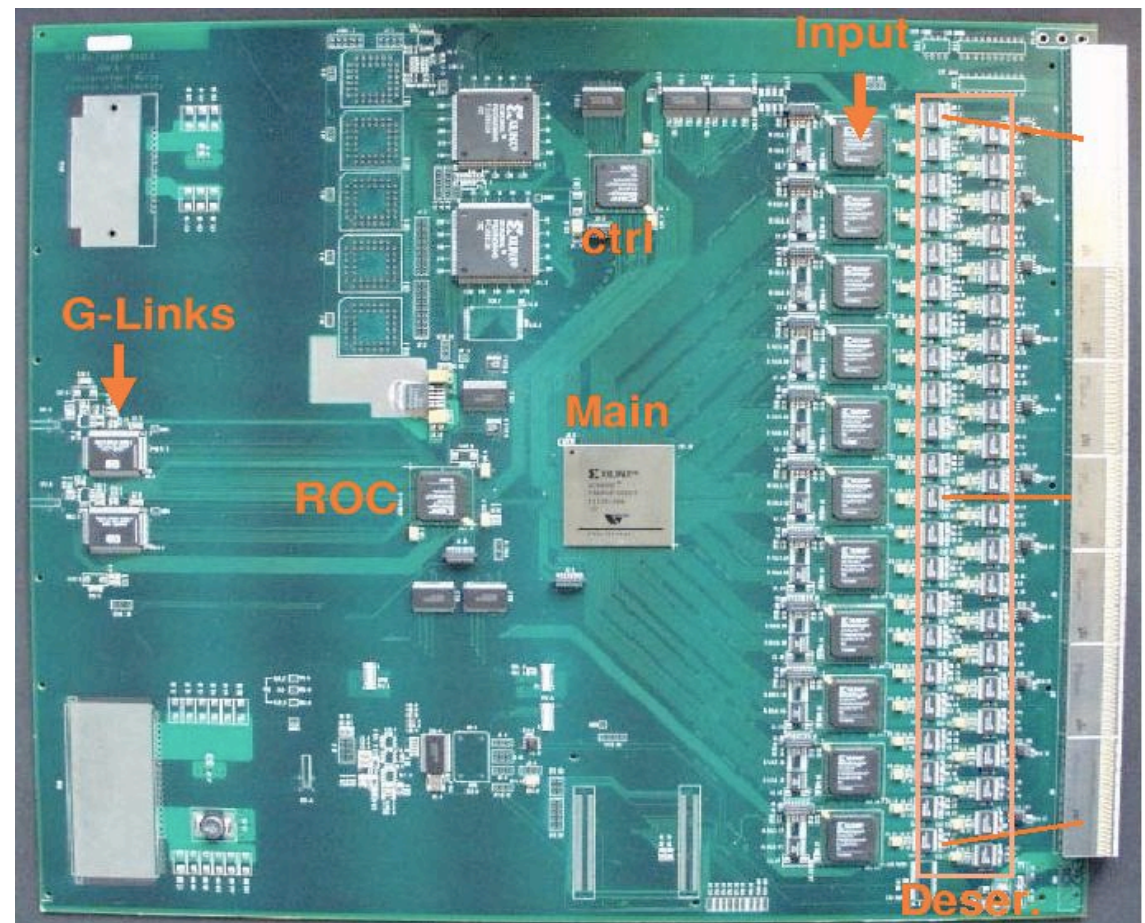
Cluster Processing Module

- Prototype assembled and powered
- JTAG tests finished, manufacturing errors have been fixed
- VME, CAN access, FPGA configuration tested
- Underway: LVDS input tests

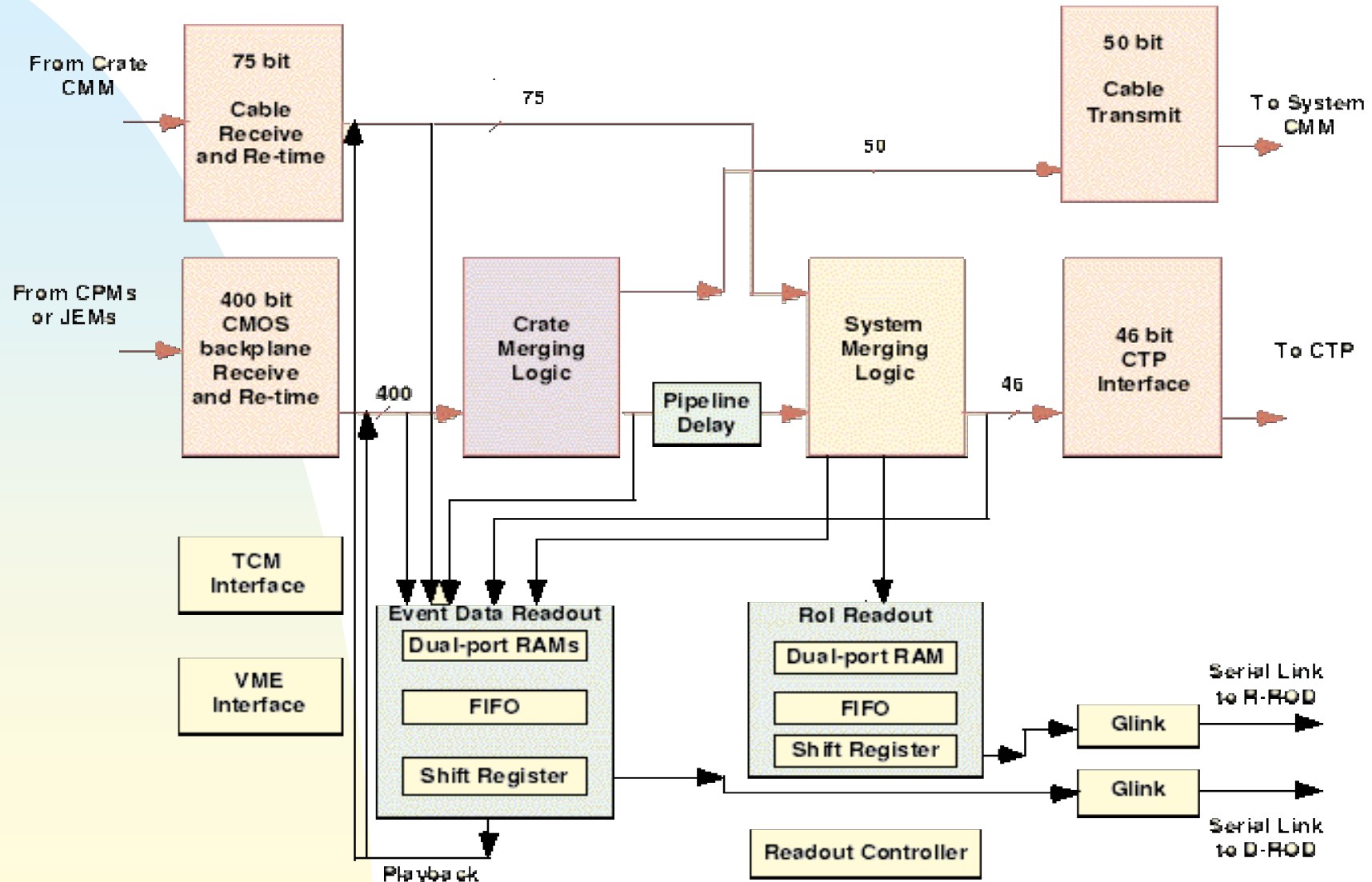


Jet/Energy-sum Module

- 2 JEMs assembled (not quite full-spec)
- VME access and FPGA configuration successfully tested, now testing real-time data paths
- Next: produce full-spec prototype for in-crate tests w/ multiple modules

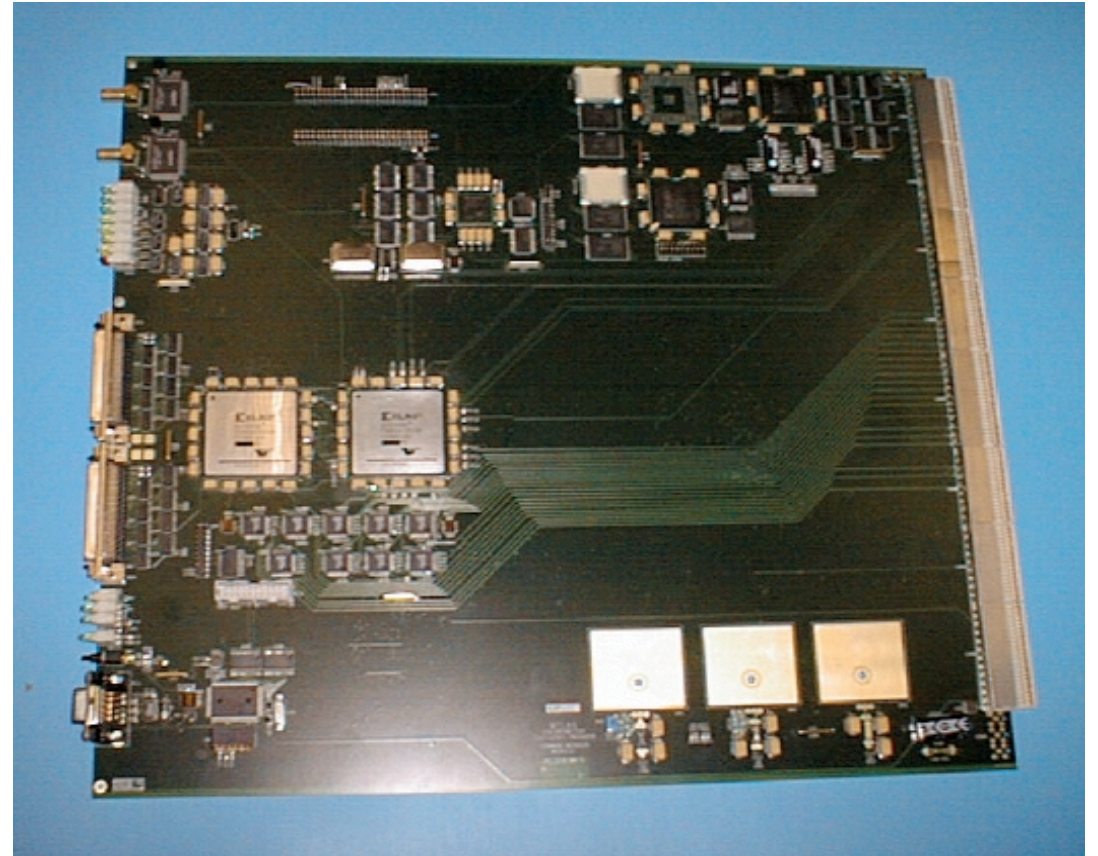


Common Merger Module



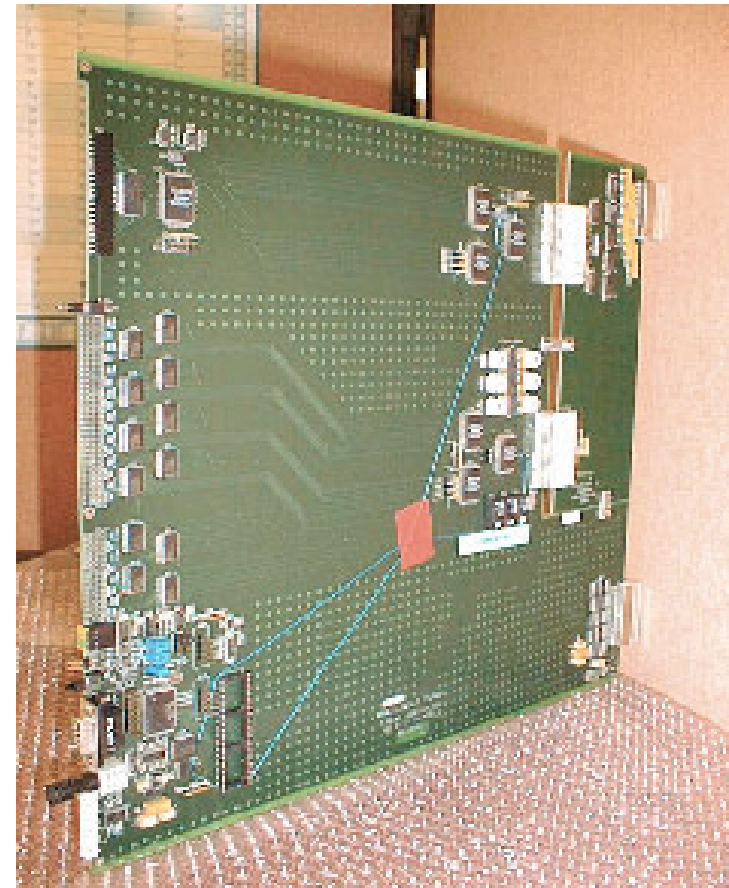
Common Merger Module

- VME access, CAN and basic board functions have been successfully tested.
- Rear transition module for system-level connection ready for manufacture
- Next step: testing real-time data paths



Timing and Control Module

- Distributes TTC and CAN signals to rest of crate, provides VME display
- TCM functions have been successfully tested, including CAN communication with other modules in crate.



Processor Backplane

9U, 21 slots, 18 layers (8 signal)

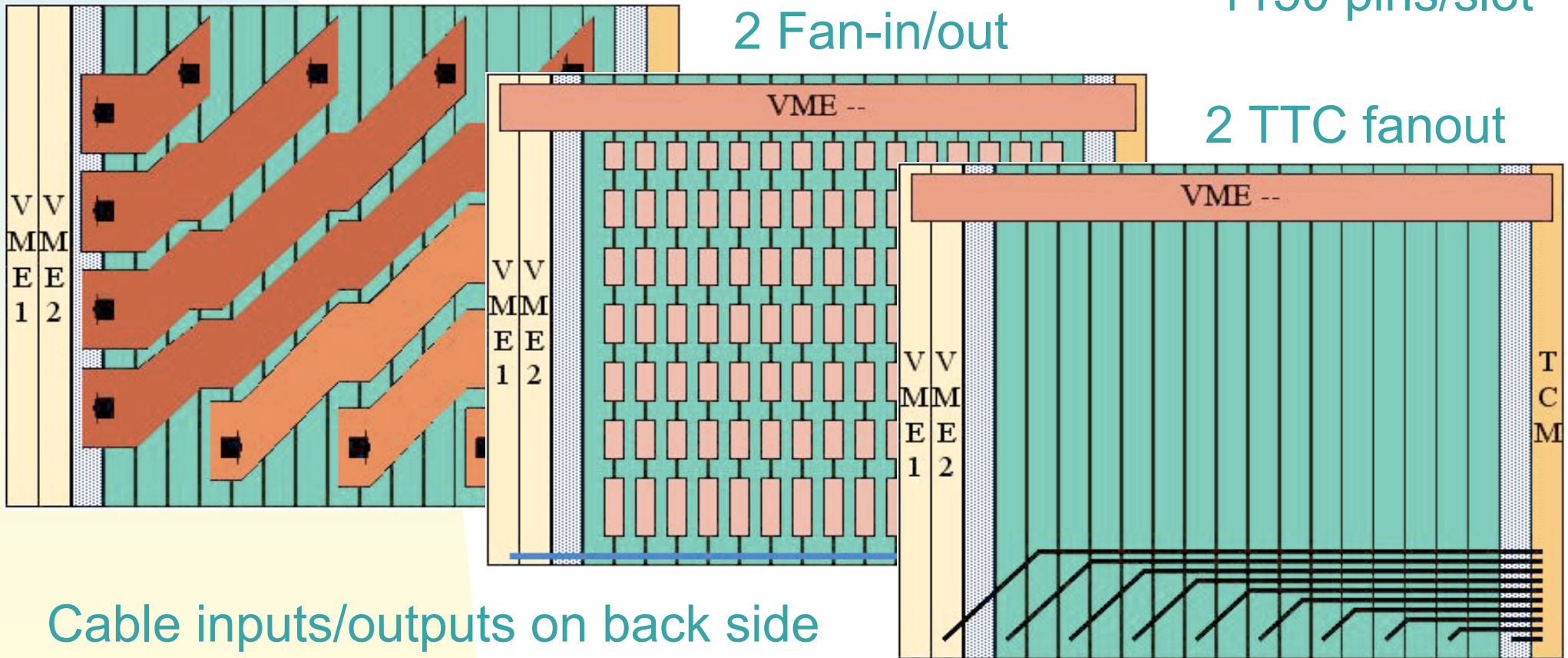
Reduced VME, TTC, CAN

~1150 pins/slot

4 Merging Layers

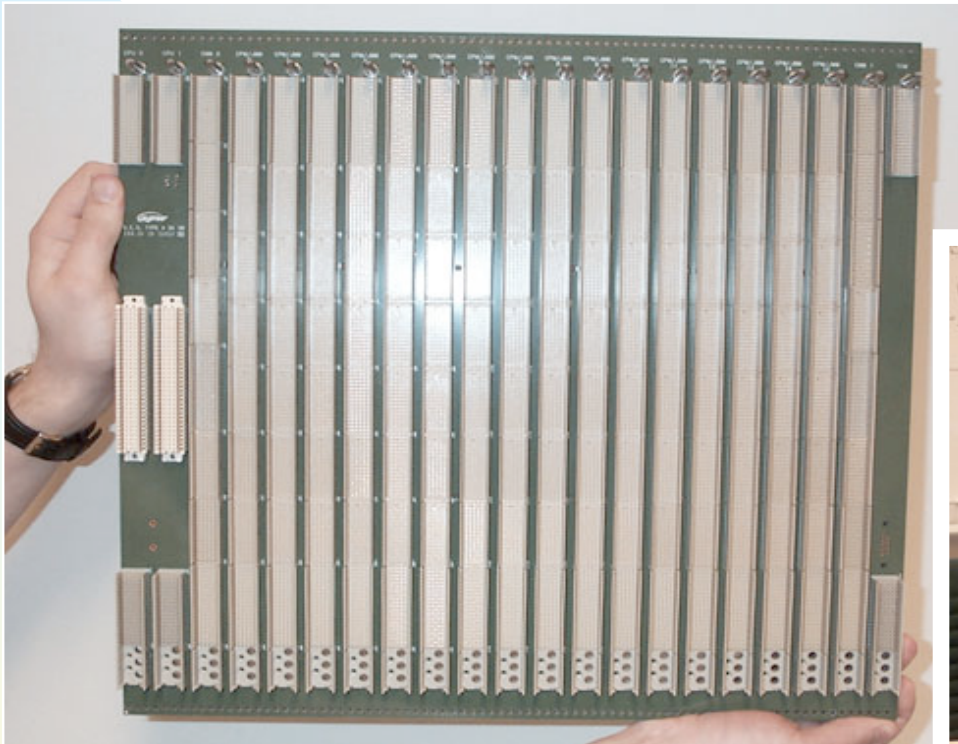
2 Fan-in/out

2 TTC fanout

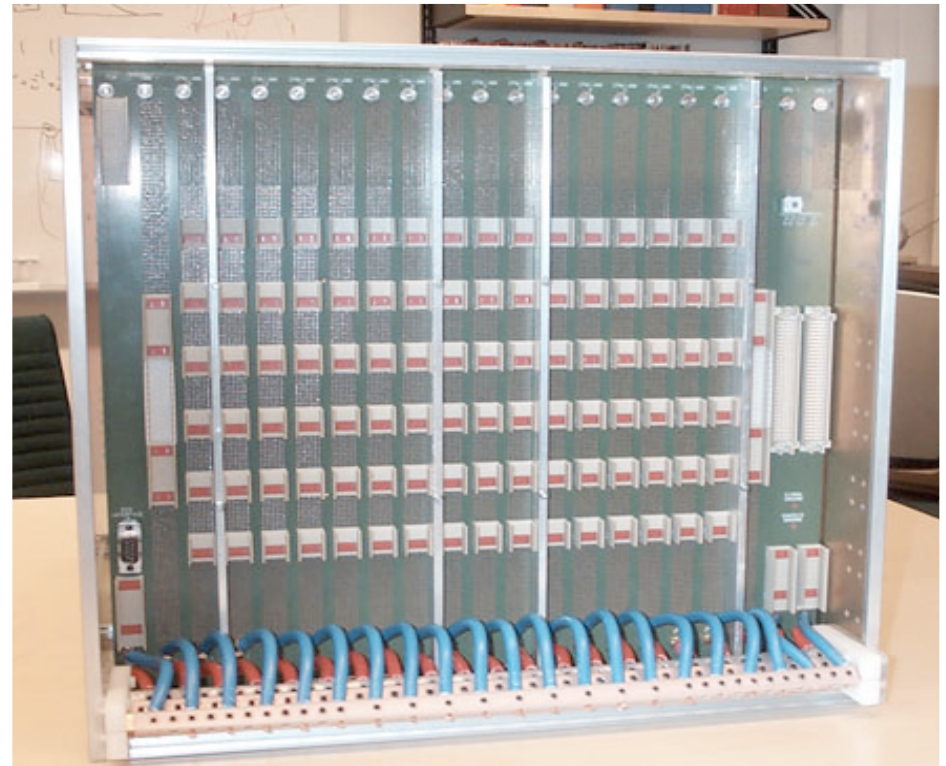


Cable inputs/outputs on back side

Processor Backplane



4 prototypes manufactured

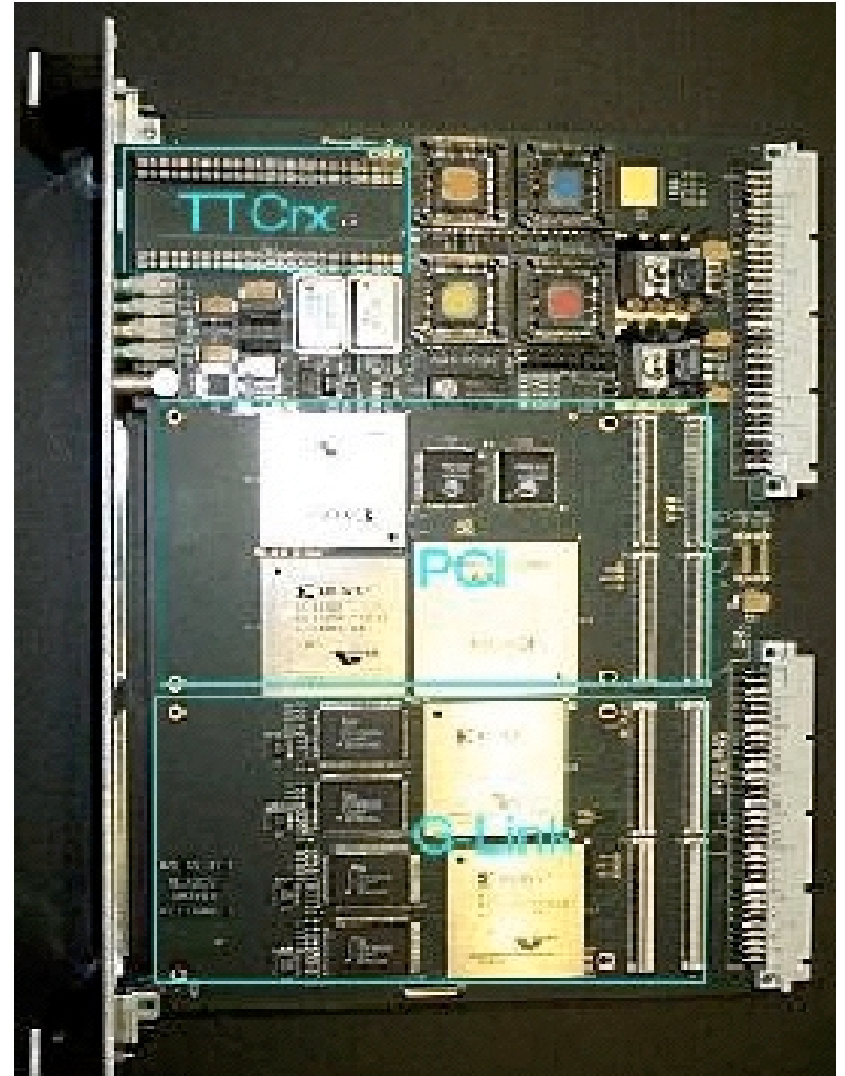


June 26, 2002

ATLAS Overview Week at Clermont-Ferrand

CP/JEP ROD prototype

- Common hardware for CP/JEP sub-systems, both DAQ and RoI
- Integration tests done with RoIB prototype and DAQ
- First prototype has been exhaustively tested
- Six new RODs assembled, testing underway



Software

- Slice tests aim to use a prototype of the final software.
- We need to configure, run and check a distributed system at full speed with a wide variety of test vectors.
- Extension of our interactive hardware diagnostics (HDMC) to provide higher level “module services”
- Detailed simulation of the hardware
- Integration of these with the Online Software run control framework and database

Summary and Outlook

- Prototype modules “to module-0 specification” for most components have now been manufactured and are in testing stages
- Prototype control and diagnostic software to be integrated into Online software for tests of multi-crate Level-1 slice system
- Integration of sub-systems planned for fall and winter 2002-2003.
- Goal of present stage: Full slice tests of Level-1 Calorimeter system to start in spring 2003