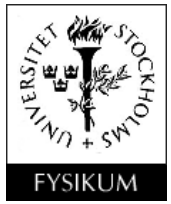
Level 1 Calorimeter Trigger

Overview

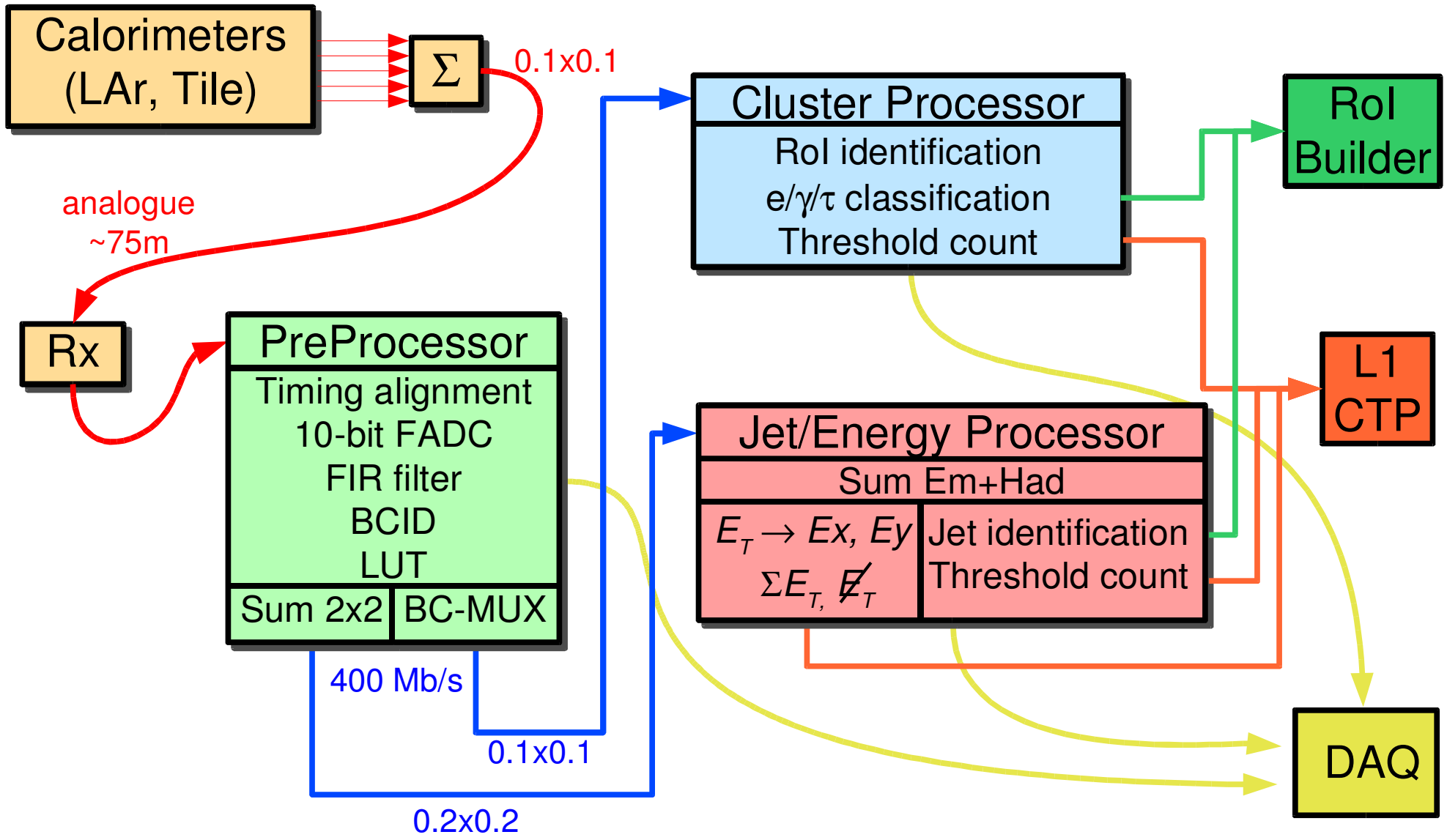
Project Status

Components

Schedule



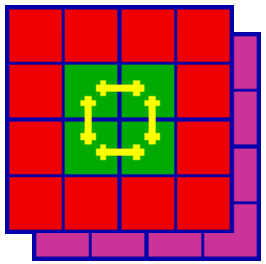
Calorimeter Trigger Overview



Architecture and Mapping

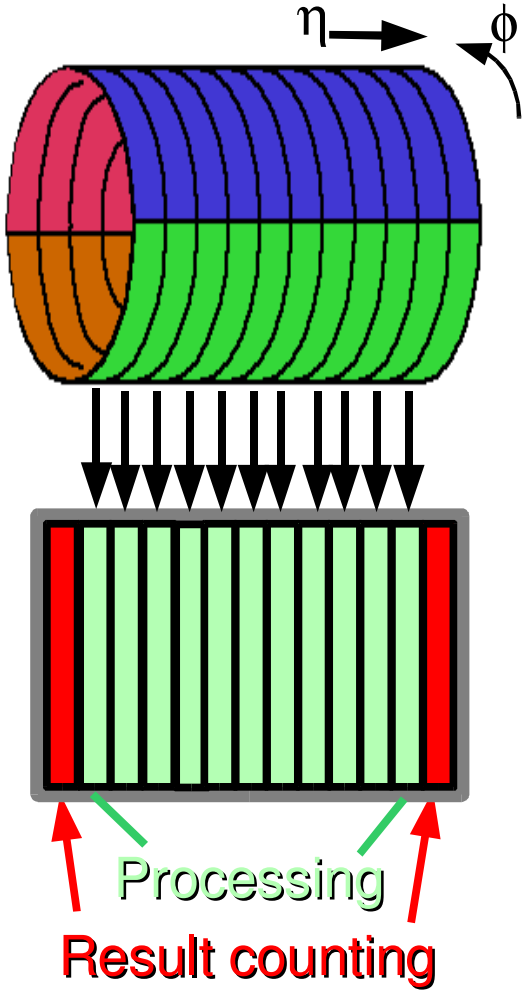
Algorithms based on overlapping windows

e/γ/τ: E_T cluster + isolation

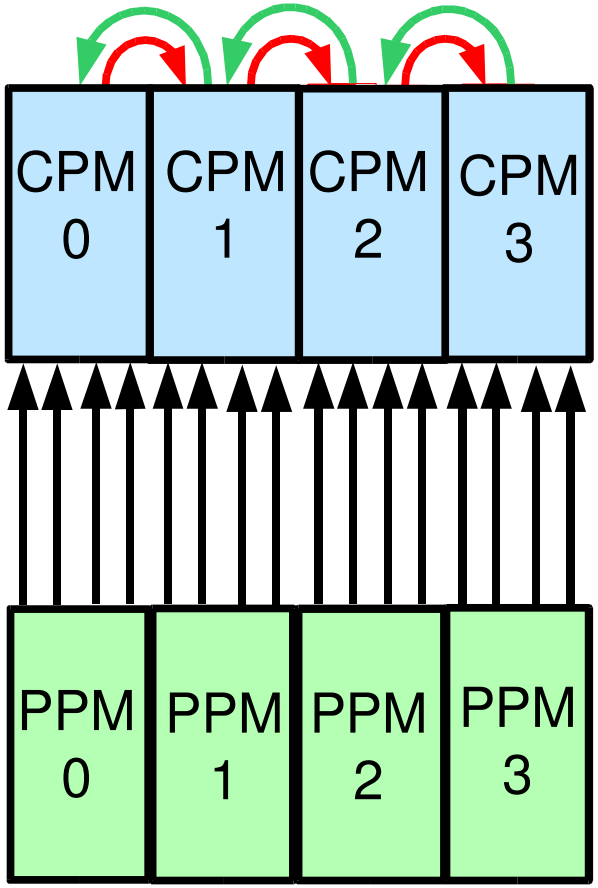


Hence data must be shared between processing elements

Crates & modules processes ϕ quadrants



Data shared via backplane (1↔1 links)



State of the Project

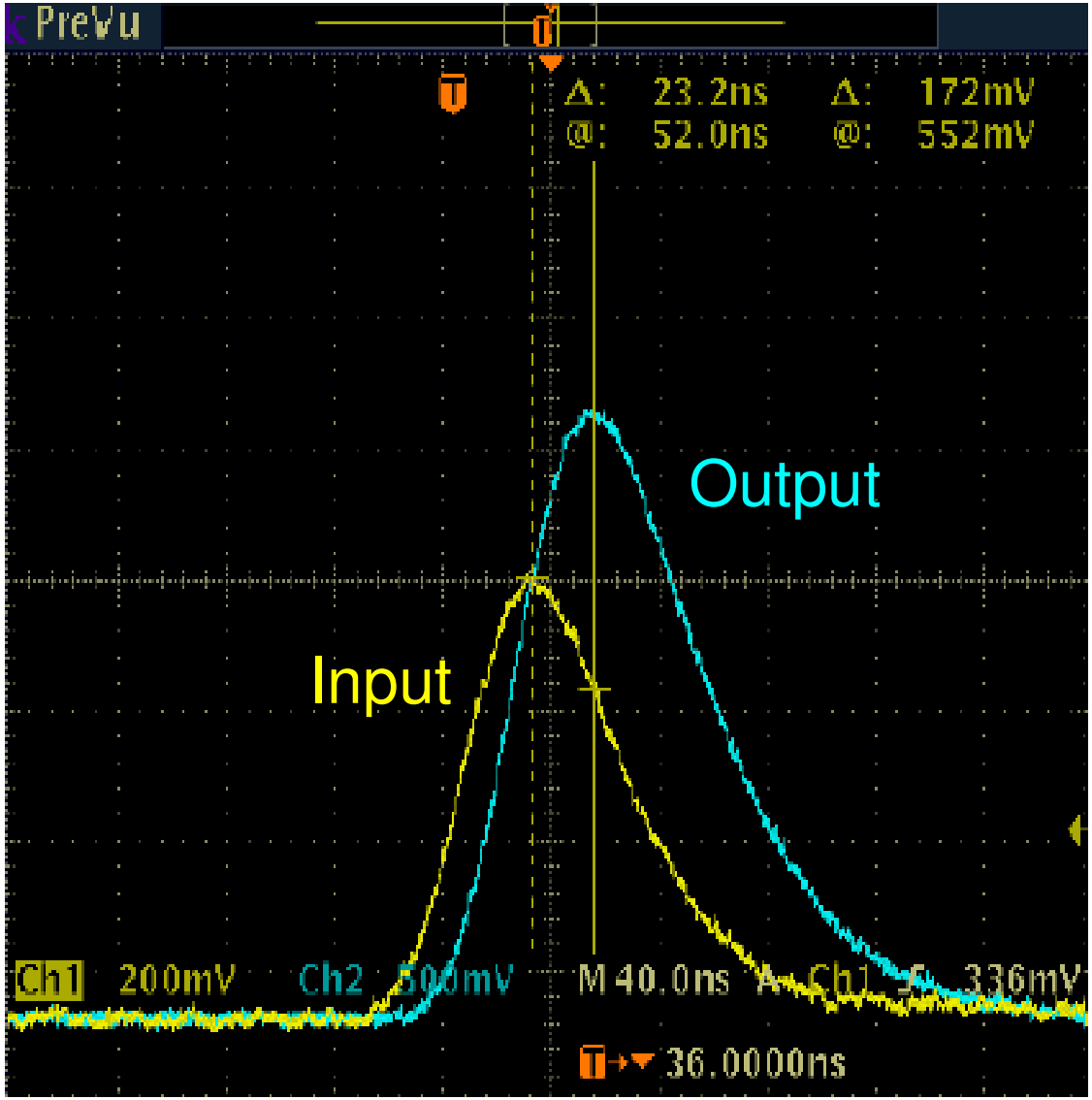
Full-Spec Prototype Testing

- Prototypes of most components have been constructed and tested
  - remaining ones currently being produced & assembled
- Fabrication problems encountered in several components
  - now understood
- Tests have identified places where designs can be improved
- “Integration testing” taking place now
- “Full slice” tests of system this winter

Tile Receiver Tests

Patch panel & gain adjustment

- Based on LAr receivers
- Transformer coupling produces undershoot
  - 10μs, 1% amplitude
  - should not be a problem
- Tested at Tile test-beam
  - using charge-injection pulses
  - pulse shapes, receiver latency as expected
  - will want to test further using beam



PreProcessor

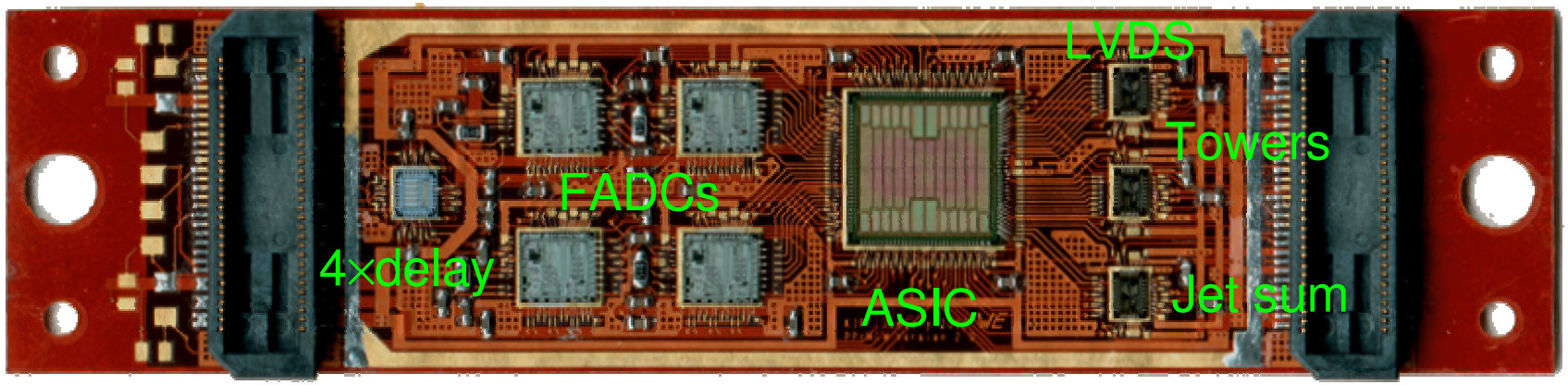
Digitisation, synchronisation, Bunch-Crossing ID, calibration, jet pre-summing, bunch-crossing multiplexing and serialisation

Use ASICs and MCMs to produce compact system:

- 4 towers/MCM × 16 MCMs/module × 16 modules/crate × 8 crates

Component production and testing:

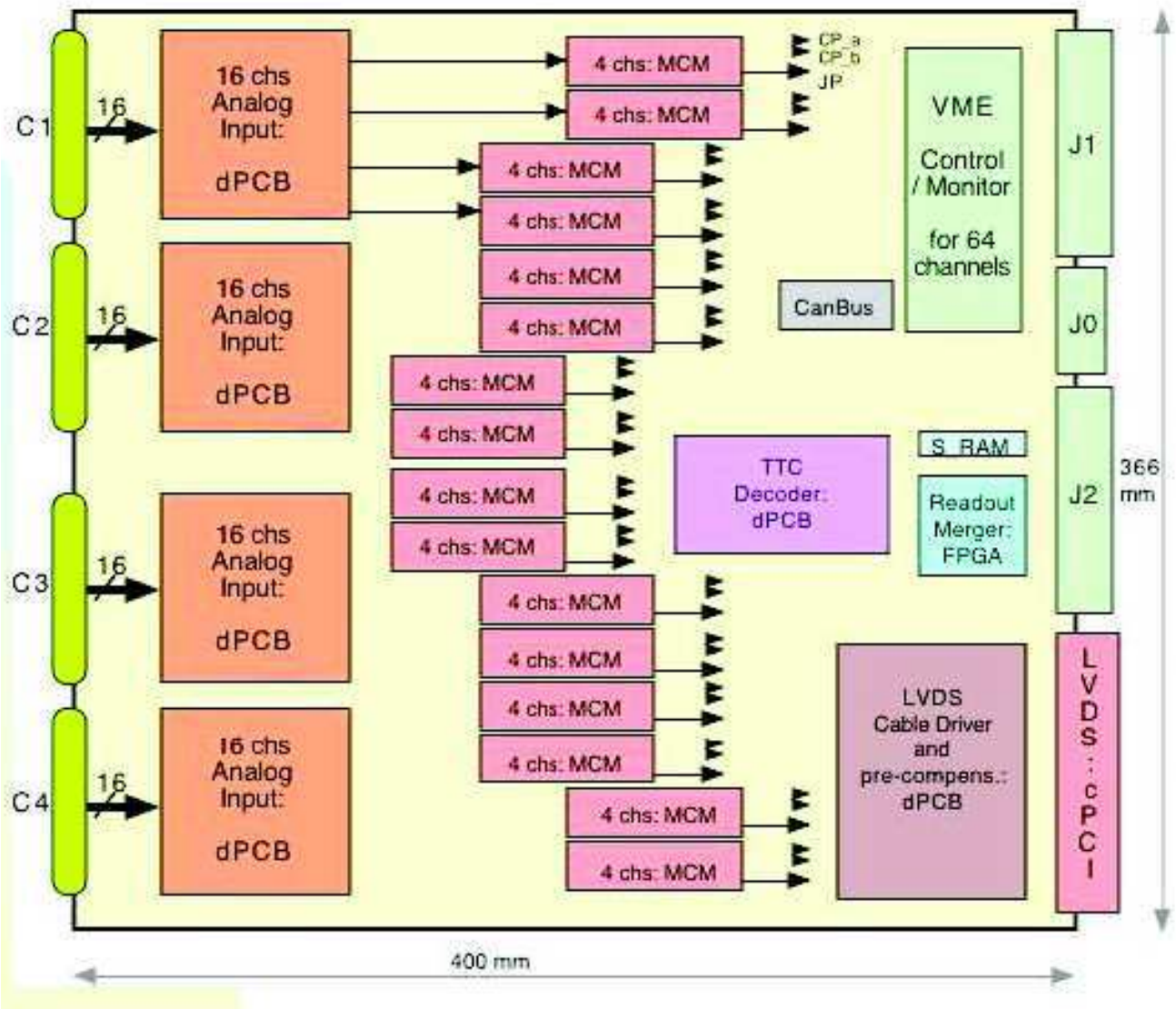
- 2 MCMs + ASICs tested for 1 year – only 1 minor problem
- Begun MCM manufacture for 4 PreProcessorModules (64 MCMs)
- Analogue input and LVDS output tested. Output BER < 10^{-14}



PreProcessor Module (PPM)

64 channel module

- 16x4 towers (em or had)
- 1 PPM ⇒ 1 CPM
  ⇒ 0.5 JEM
- First module imminent
- Four fully-populated and tested modules by end of year



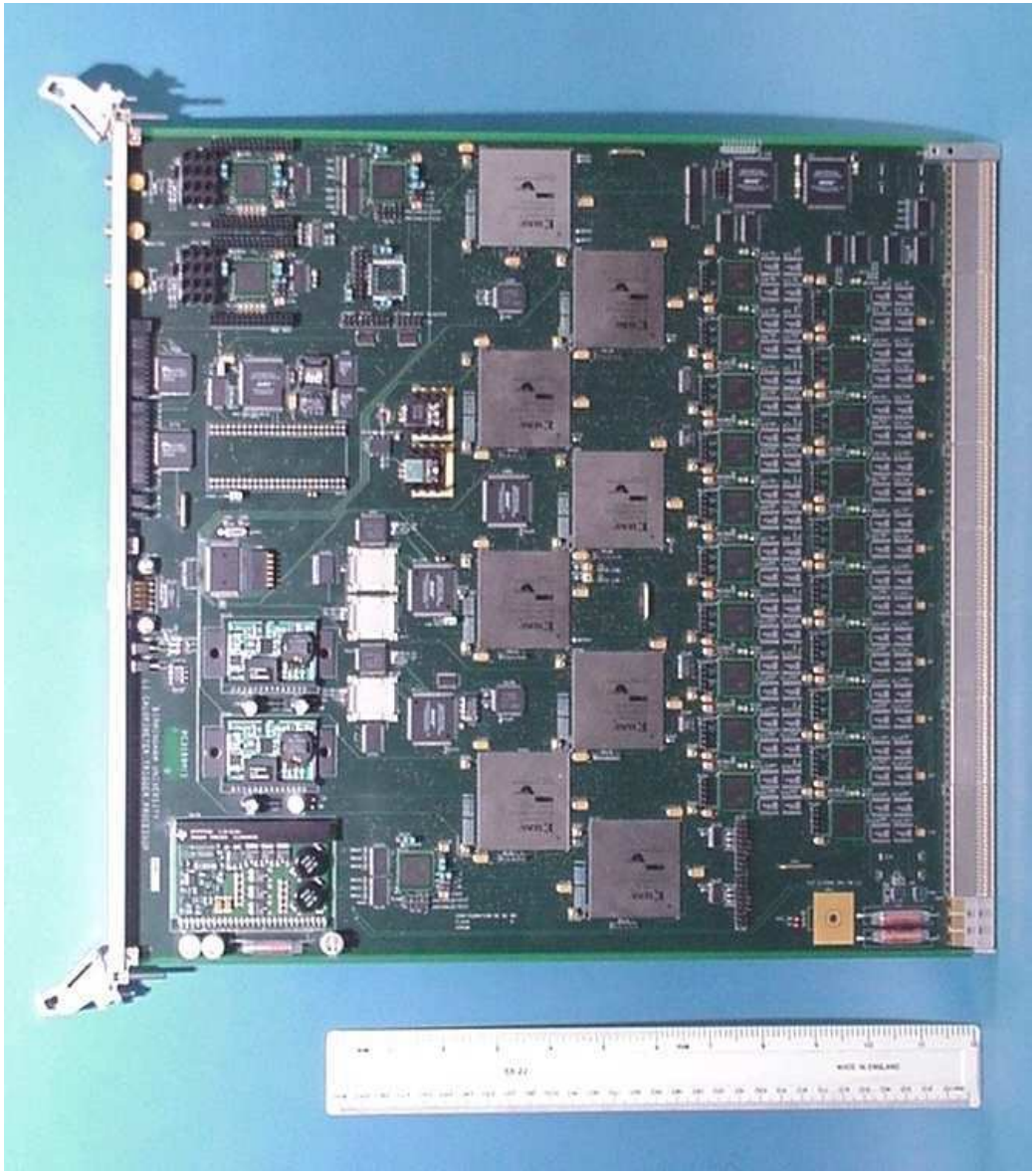
Cluster Processor Module

e/γ and τ/h identification

- 64 windows/module × 14 modules/crate × 4 crates
- entirely FPGA-based logic

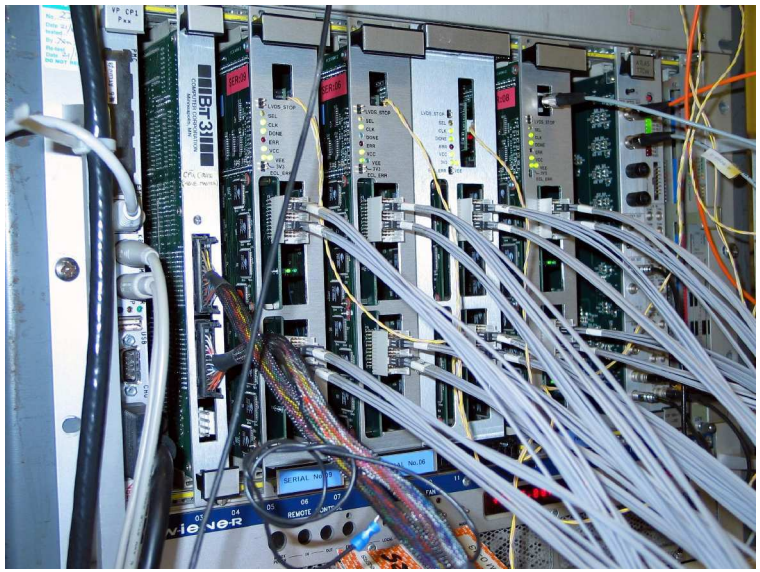
First module under test > 1 year

- 80 × 400 Mbit/s LVDS inputs: BER < 10^{-13}/channel
- 160 Mbit/s fan-in/out with adjacent modules error free
- Algorithm processing correct
- Readout to ROD tested > 100 kHz
- Error-free transmission of results to Common Merger Module

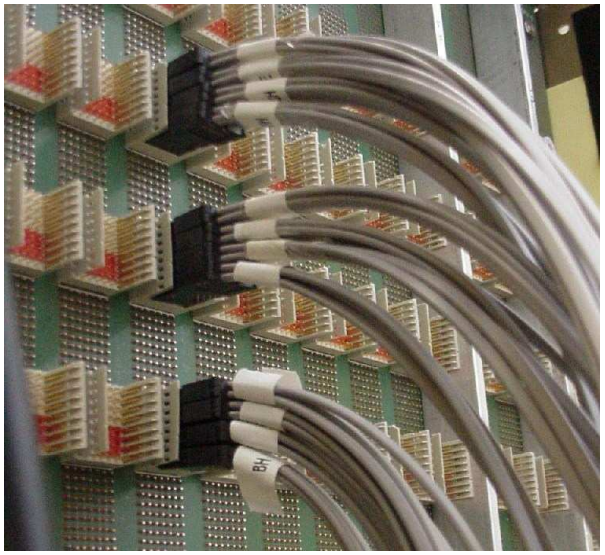


CPM Testing

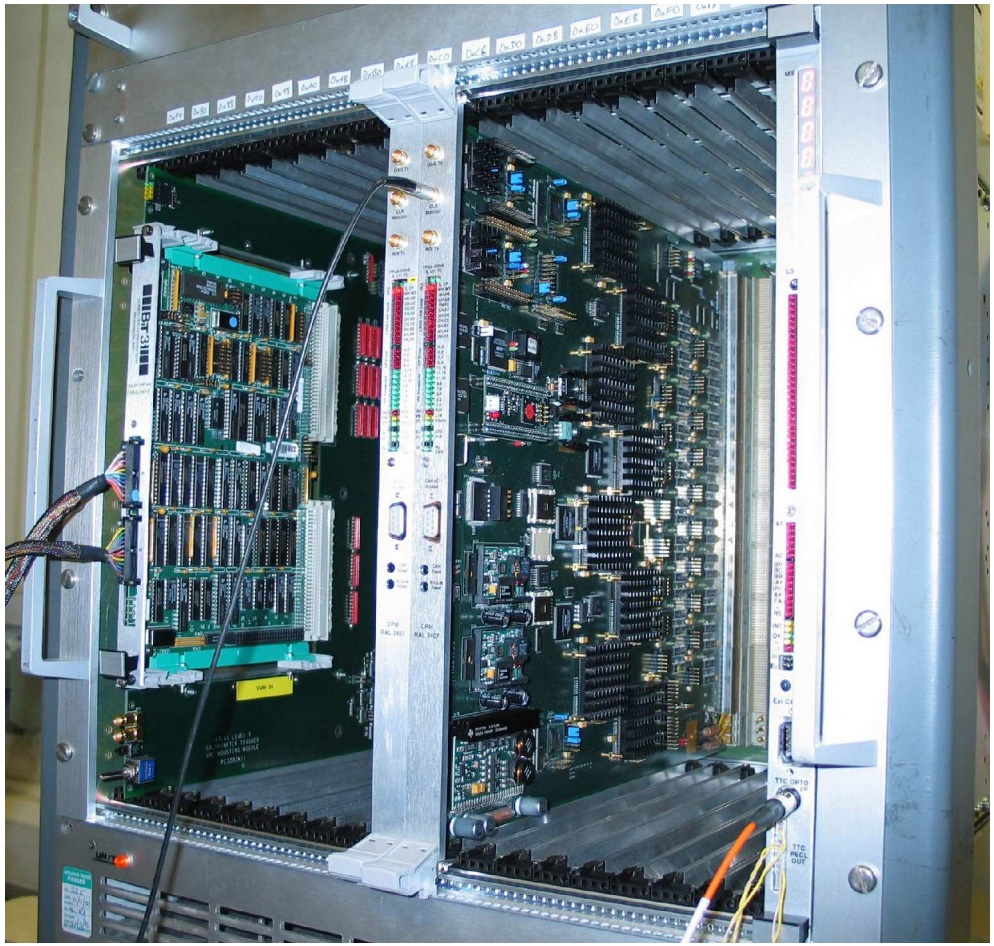
LVDS data sources



LVDS data input



Tests with 2 CPMs

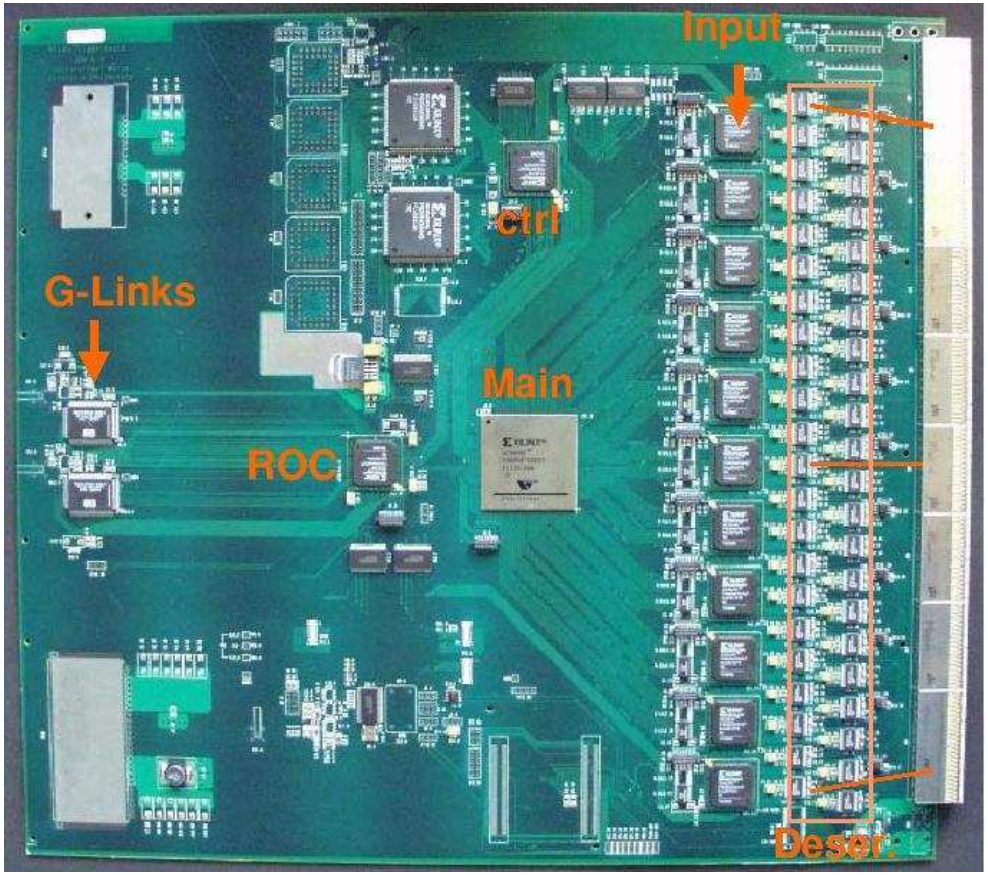


CPM Status

Several problems encountered

- Timing
  - Had to simplify synchronisation firmware for 160 Mb/s signals
  - Now works well, but margins very tight
  - Modified design will improve signal layout and clock distribution
- Fabrication
  - Extremely complex board, with large ball-grid FPGAs
  - First module was fine, but second and third had chip connectivity problems ($\Rightarrow$ expense and delay)
  - Using Sn-plated BGA contacts instead of Au/Ni solves problem
    - new process for large boards
    - 4^{th} CPM successful, 5^{th} being assembled

Jet/Energy Module



Jets, $\not{E}_T$, ΣE_T

- 32 windows/JEM × 16 JEM/crate × 2 crates

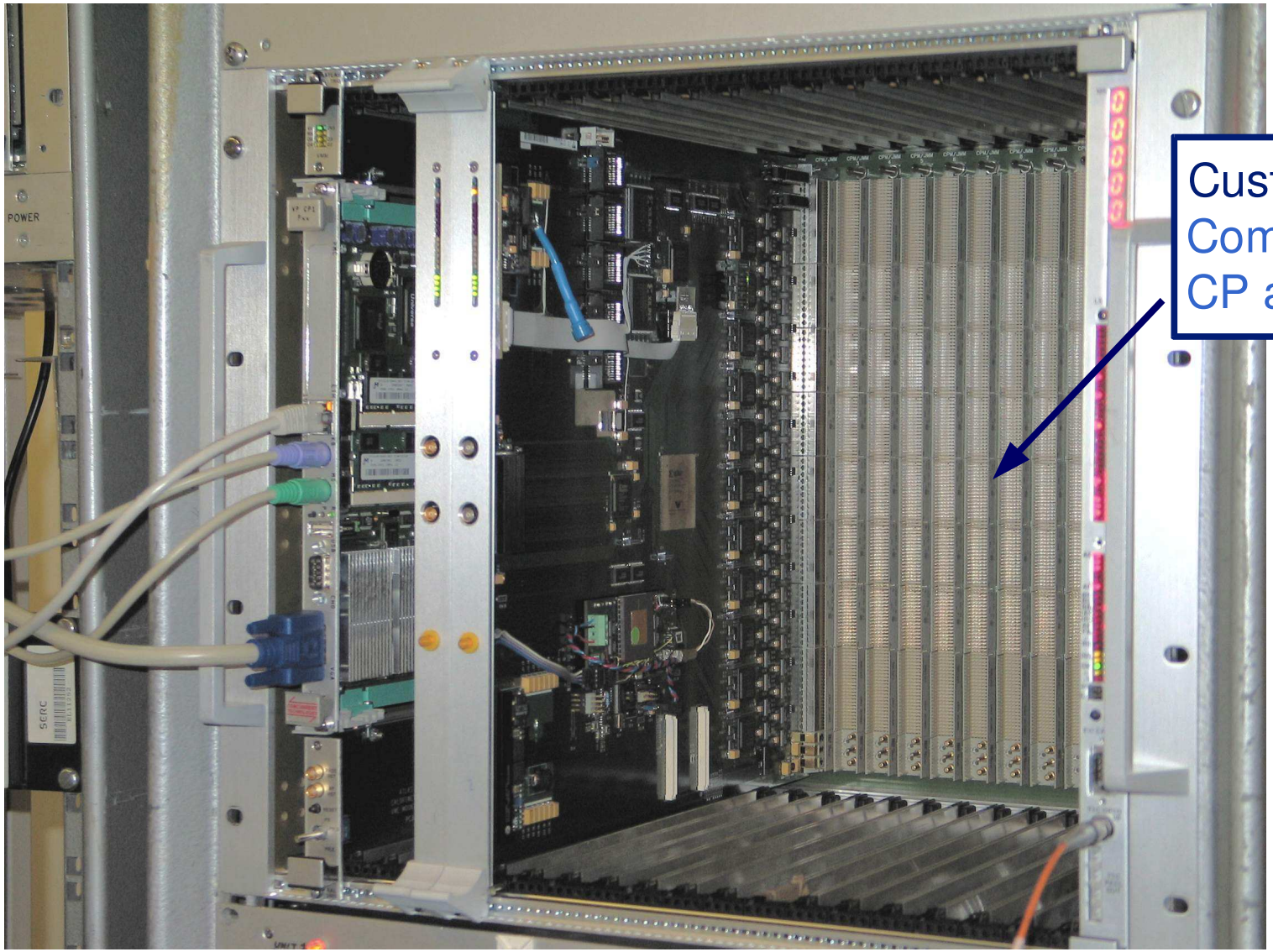
2 full-function modules exist

- near-final prototypes providing all interfaces
- realtime E_T trigger path successfully tested with physics test vectors.
- Jet algorithm firmware under test
- LVDS input and output to CMM successfully tested
- ROD output tests advanced

Final spec version being designed

- More powerful FPGAs, denser LVDS

JEM Tests – 2 JEMs in crate



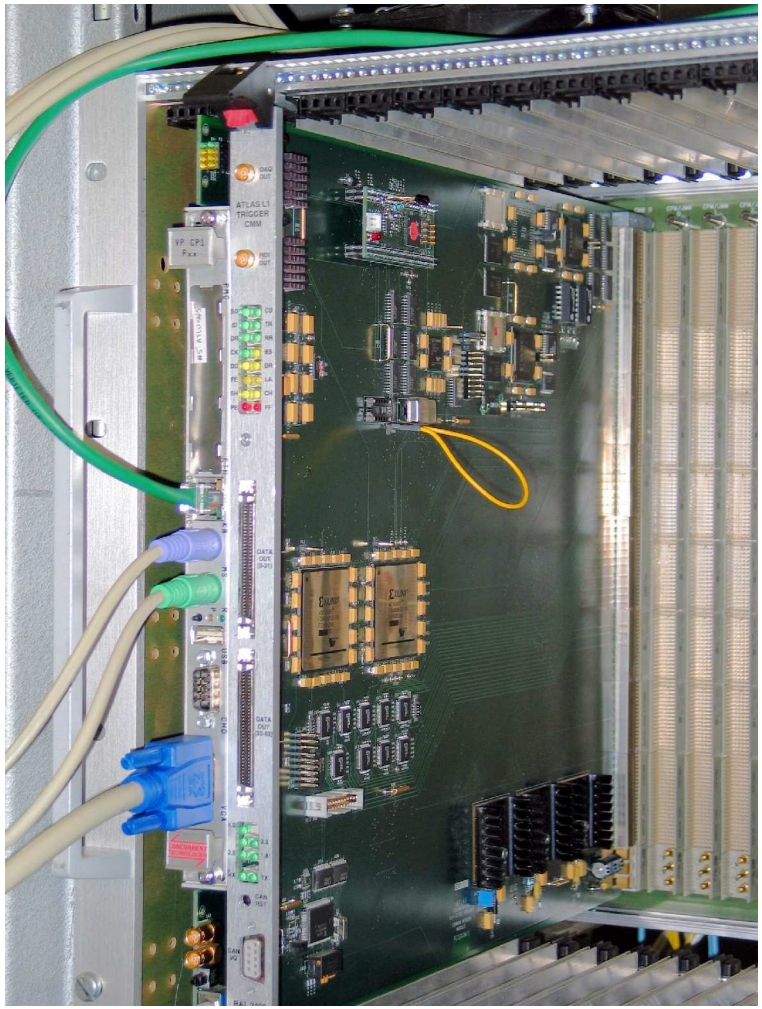
Custom Backplane:
Common design for
CP and JE systems

Common Merger Module

- e/γ and τ/h hit counting
- jet hit counting
- ΣE_T, $\not{E}_T$ final sum and threshold
  - One hardware design
  - Different firmware for different tasks

Status:

- Realtime data tested with Jet/Energy Cluster Processor hardware
- Readout to ROD under test
- Jet & E_T firmware to be tested



ReadOut Driver

CPM, JEM and PPM data → DAQ

RoI data → RoI Builder

- One design for all functions
- But 10 firmware variants

4-channel 6U prototype

- Initial tests with RoIB, ROS
- CPM, JEM, CMM firmware written and tested

Full-Spec 9U module

- 18 inputs/module = 1 full crate
- PDR completed July

Integration and Slice Tests

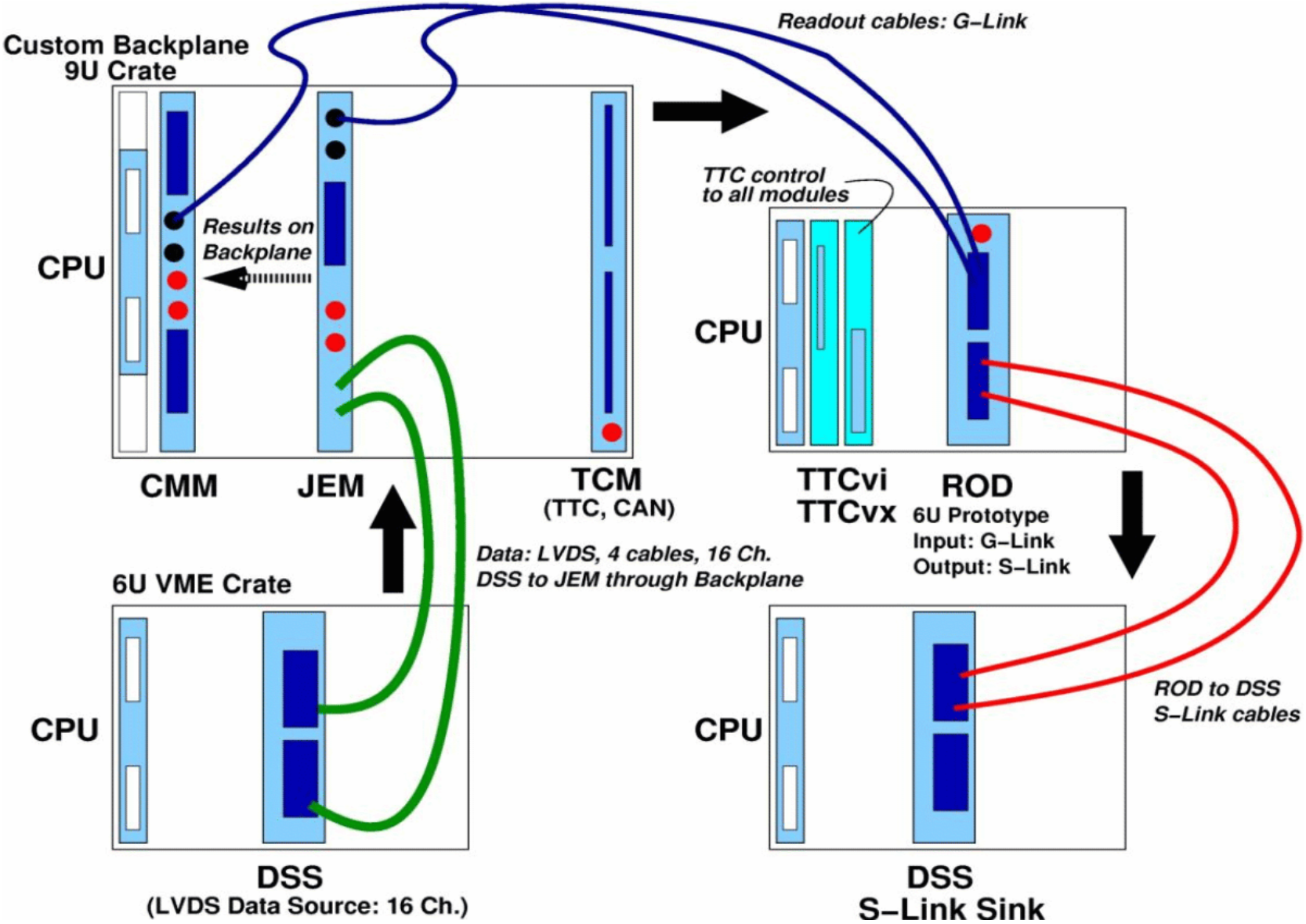
Individual Modules and Small Subsystems

- Inputs: random data, test patterns, patterns from physics simulations
- Test modules (e.g. Data Source/Sink) used to generate inputs or receive results (emulating other modules)
- Pairs of CPMs and JEMs used to test fanout via custom Backplane
- Results output CPM/JEM to CMM and ROD.
- CPM+CPM to CMM and RODs; JEM+JEM to CMM and RODs
- Major online software effort essential to tests

Next Steps

- Realtime tests with CTPD (*Oct/Nov*) and with RoIB and ROS.
- Initial PreProcessor Module to CPM and JEM (*autumn*)
- Full system slice tests with Preprocessor (*winter*)
- Participate in ATLAS combined test-beam in 2004

Example: JEM Integration Test Setup



Long-Term Schedule

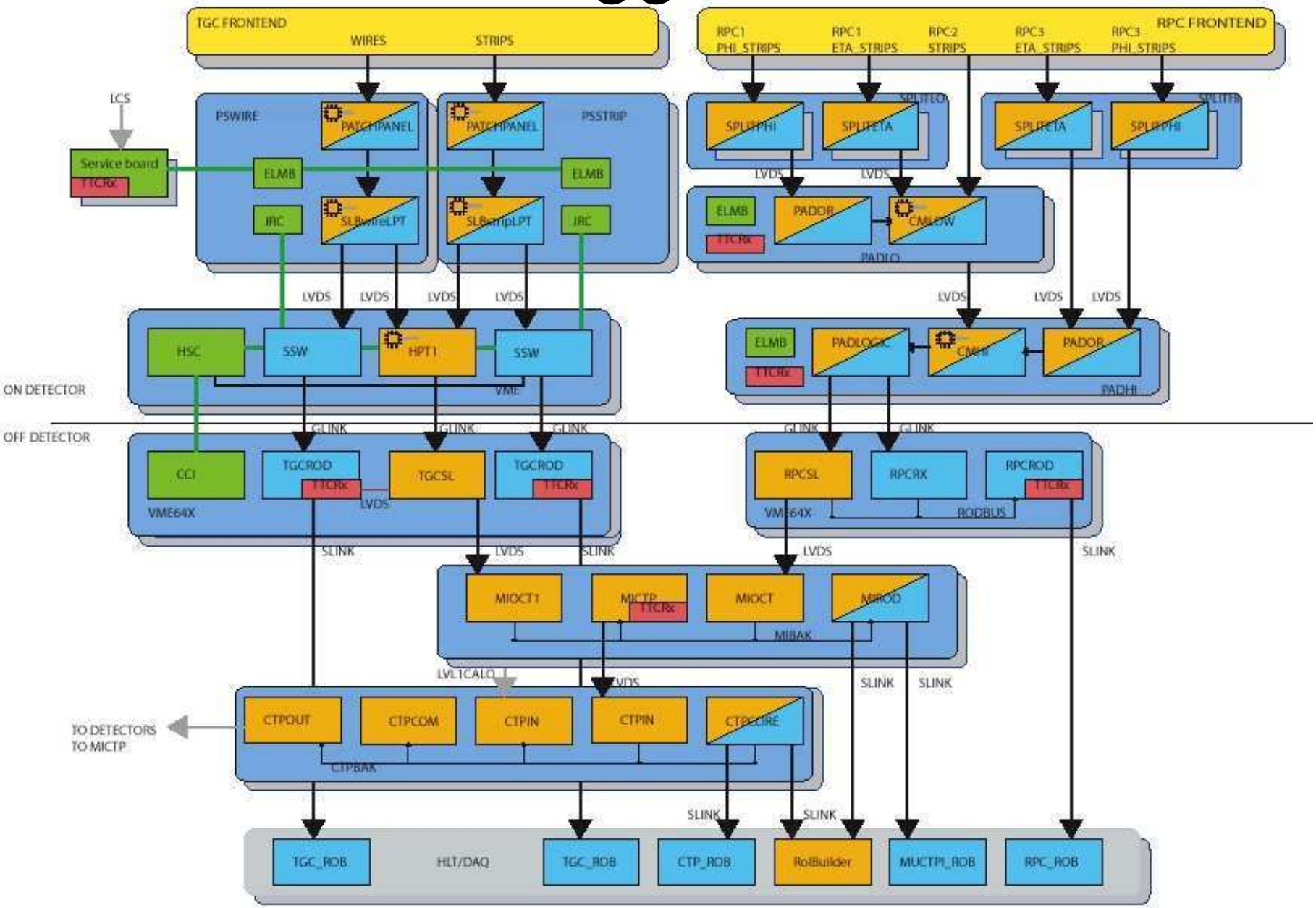
FDRs/PRRs for all final modules:	*Mid-2004*
Module Production and Tests:	*August 2004 – March 2005*
Subsystem Tests Start:	*March 2005*
Start integrating calorimeters with PPr Modules:	*May 2005*
Install fully tested CP and JEP Subsystems:	*March 2006*
Full calorimeter trigger system available:	*October 2006*

LVL1 Muon (and Central) Trigger

S. Veneziano
on behalf the LVL1 Muon trigger groups

Overview
Components
Project status
Recent news from test beam
Conclusions

Muon Trigger Overview



TGC

- Development
  - High-Pt ASIC has already been mass produced
  - Patch-Panel ASIC production completed December 2003
  - Final design of Slave Board ASIC will be submitted in December 2003
  - Full-function prototypes of all boards
- Radiation tests
  - Completed for all ASICs, LVDS and Glink serializer, EO/OE converter, HSC FPGA, many COTs
  - Other COTs and SSW FPGA by the end of 2003
- Procurement
  - International tendering on 25th September for Cables and assembly for connections from ASD boards to PS-Boards
  - Optical fibres from cavern to USA15 in FY2003

RPC

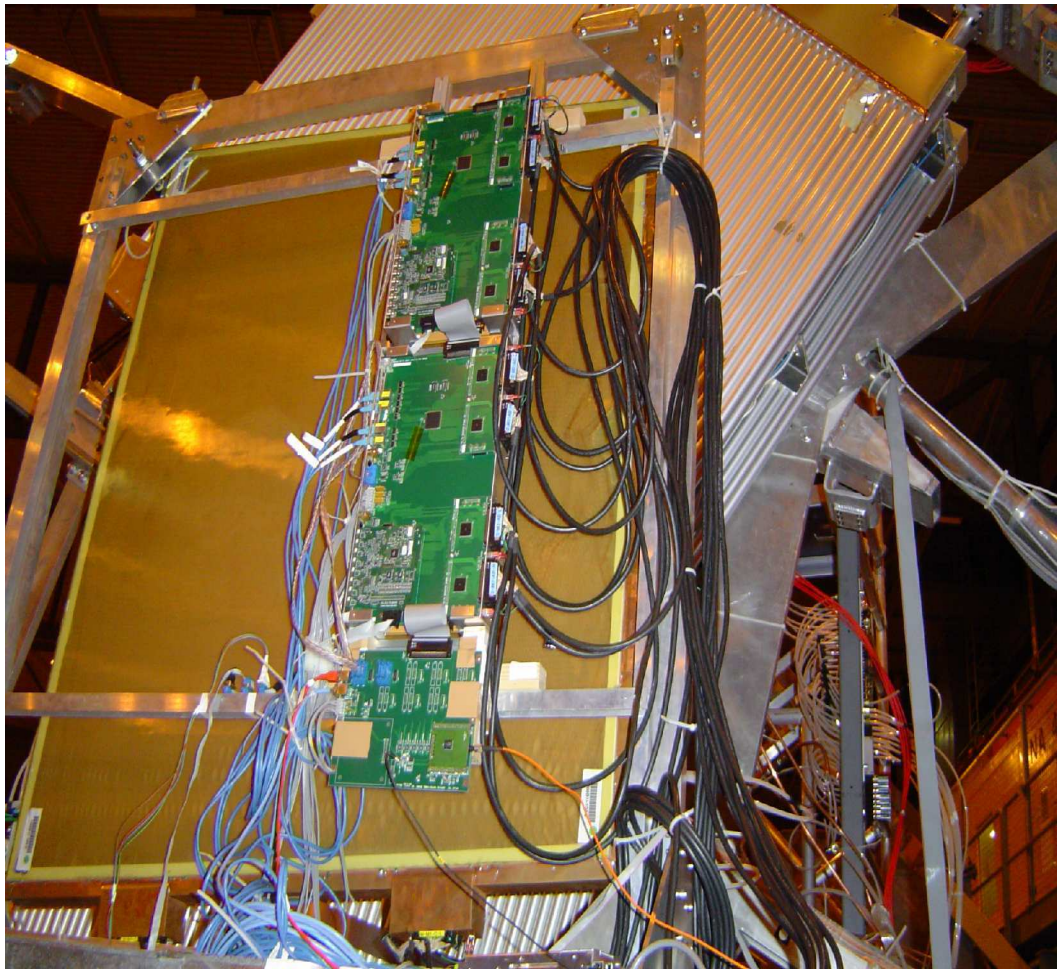
- Development
  - Final design of PAD motherboard delayed by six months due to cost/funding problems. Pre-production delayed.
  - Coincidence Matrix ASIC needs an increased pipeline depth, due to longer cables from FE and from Middle to Outer Station.
- Radiation tests
  - Completed in June for ASIC and all COTs
- Procurement
  - Splitter pre-production (5%) completed, tests done during the month of July.
  - Splitter board production starting in December 2003.

TGC tests

- Experience from first 25 ns run
  - LVDS serializers/deserializers replaced following power-supply accident
  - Various problems encountered in May are now understood and solved
    - Trigger path: synchronization failure due to mixture of LVDS serializers from different manufacturers (following repairs after accidents).
    - Coherent readout of raw data and trigger results achieved
    - Readout path: bug fixed in firmware of Star Switch
  - Improvements
    - QPLL ASIC introduced in TTC chain to improve timing
- Preparation for 25 ns run started
  - Online trigger verification implemented
  - System has been tuned and timing verified

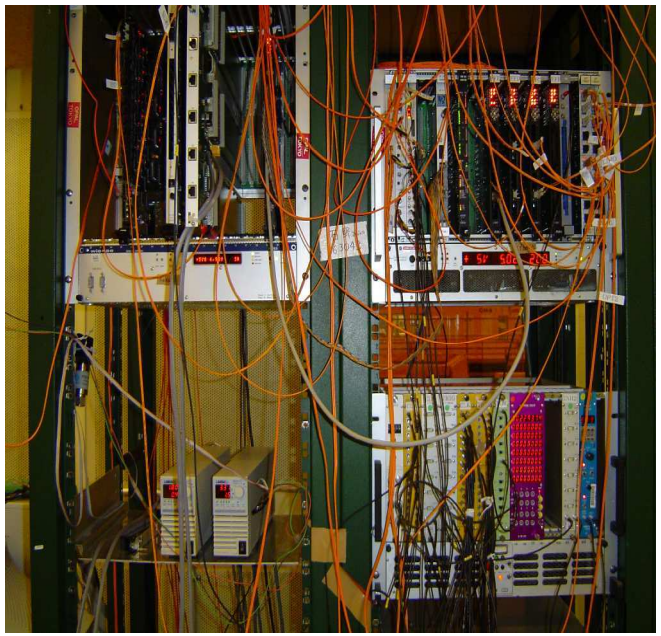
TGC trigger at H8 test-beam

FE mounted on chamber, HSC



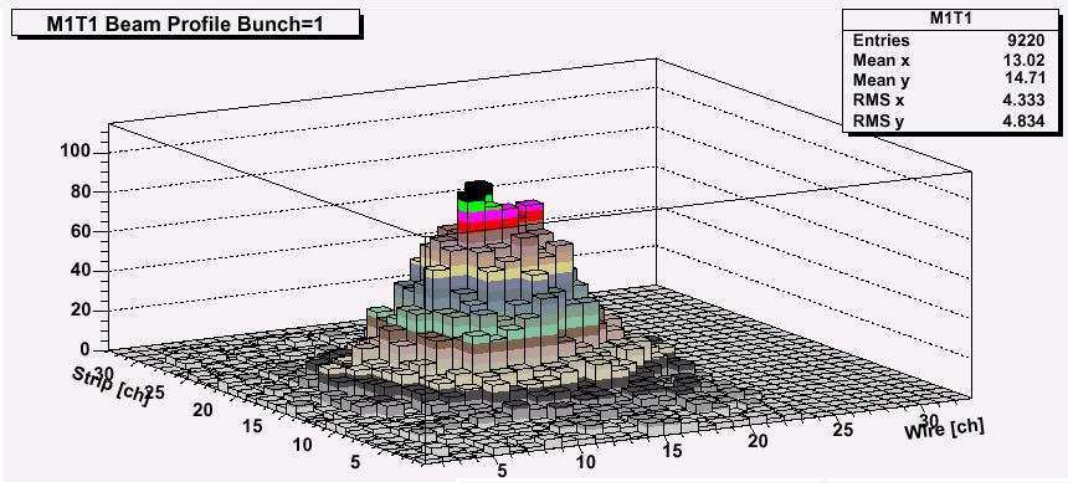
Opt. Fibers

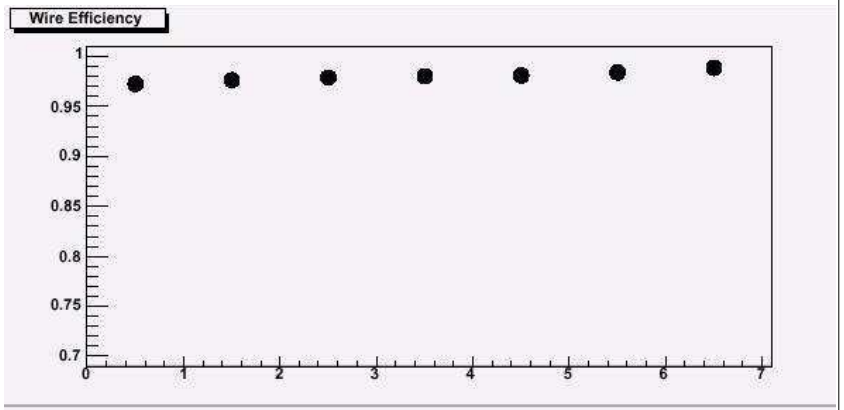
ROD, SL, in the Counting hut

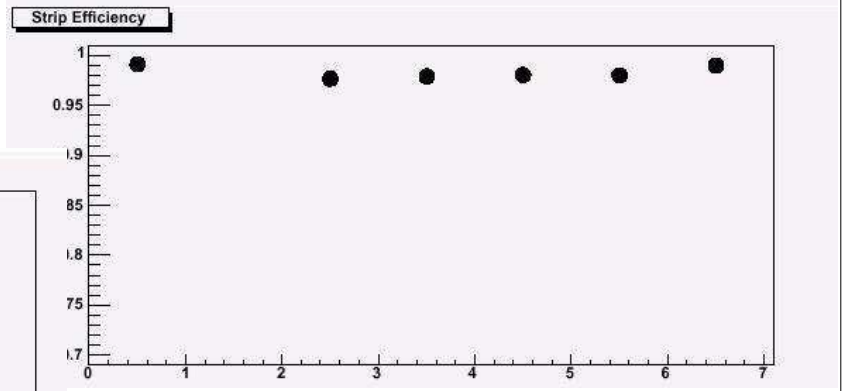


Examples of TGC results (from yesterday)

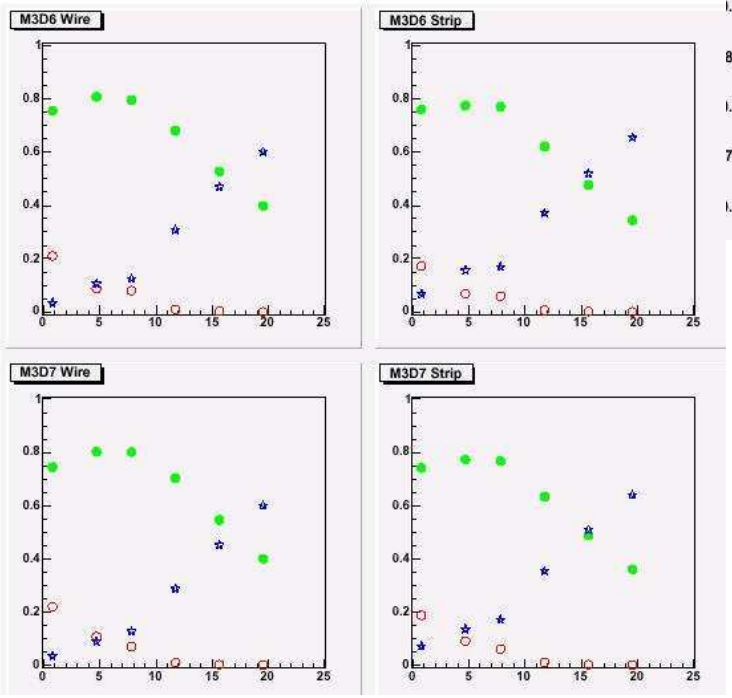
Beam profile, doublet







Wire and strip efficiency vs delay on TGC doublet, on three adjacent BCs



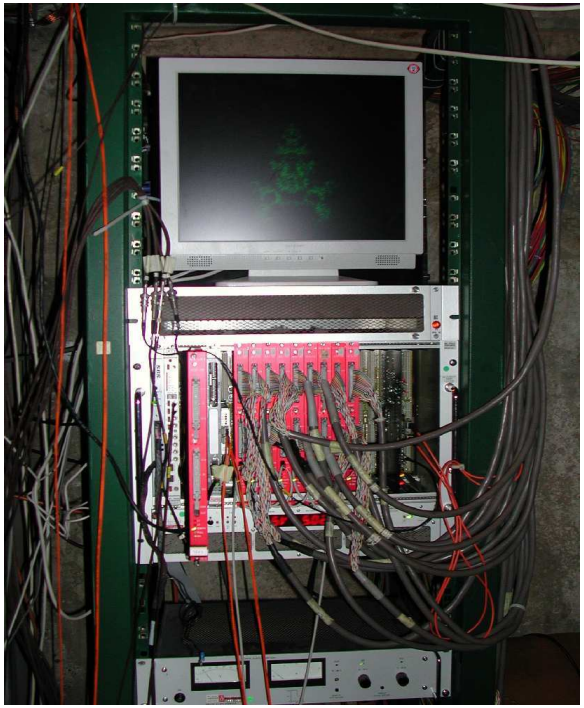
Wire and strip efficiency on full detector slice

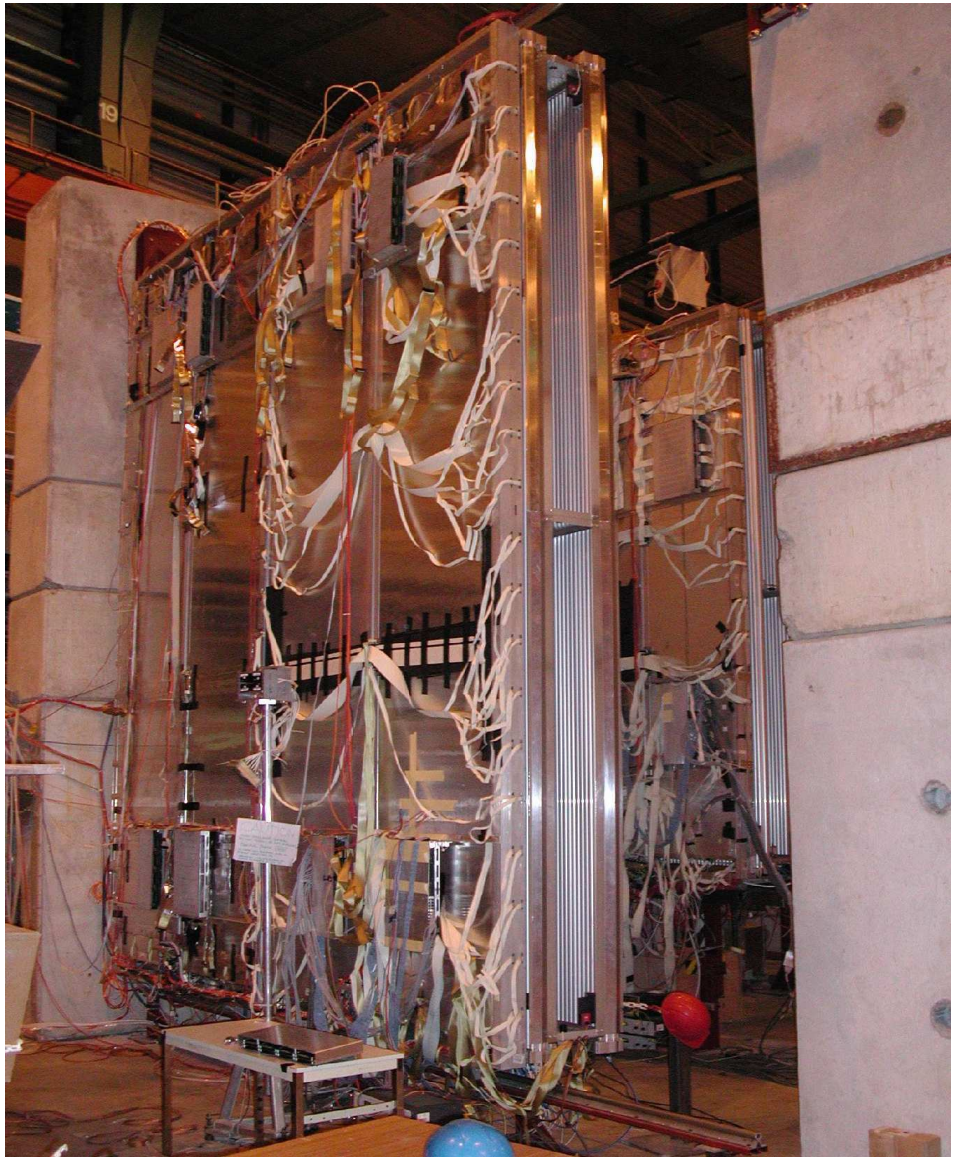
RPC tests

- Chambers and electronics commissioning during the month of July
  - Initial problems due to cabling from FE to readout and trigger electronics
  - Some instability of the system due to the use of early prototypes from Rome slice tests:
    - difficult initialization and synchronization procedures;
    - timing needs to be improved with QPLL ASIC;
    - optical link new operating mode is required;
- Four-week integrated MDT-RPC run in August with frequent expert intervention
  - Trigger used in flagging mode
  - Integrated raw data and trigger data, ATLAS data format
- 25 ns run in preparation with final version on CMETA, CMPHI mezzanines, new RX-SL prototype

RPC trigger at H8 test-beam

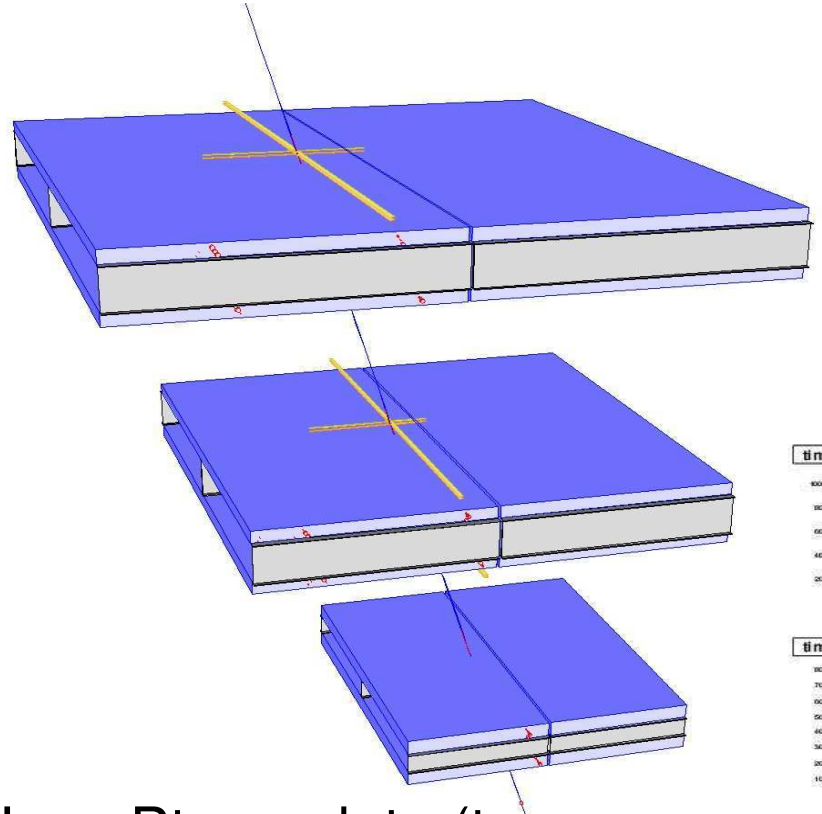
- Two BML and two BOL chambers installed
- Fully functional on-detector slice (LowPt, HighPt PADs with two CMETA and two CMPHI mezzanines)
- Parallel detector readout (RX-SL) with standard TDCs on confirmation planes

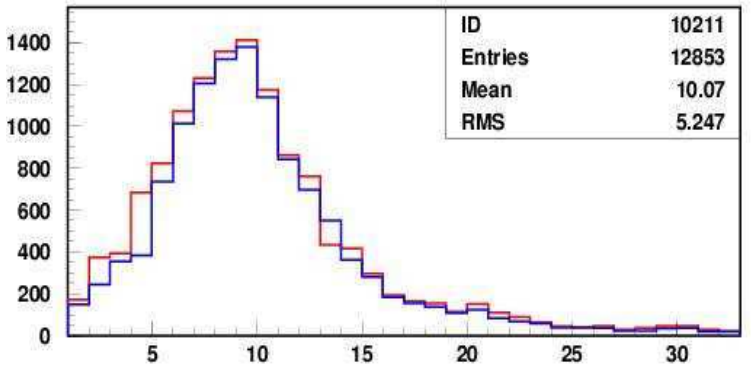




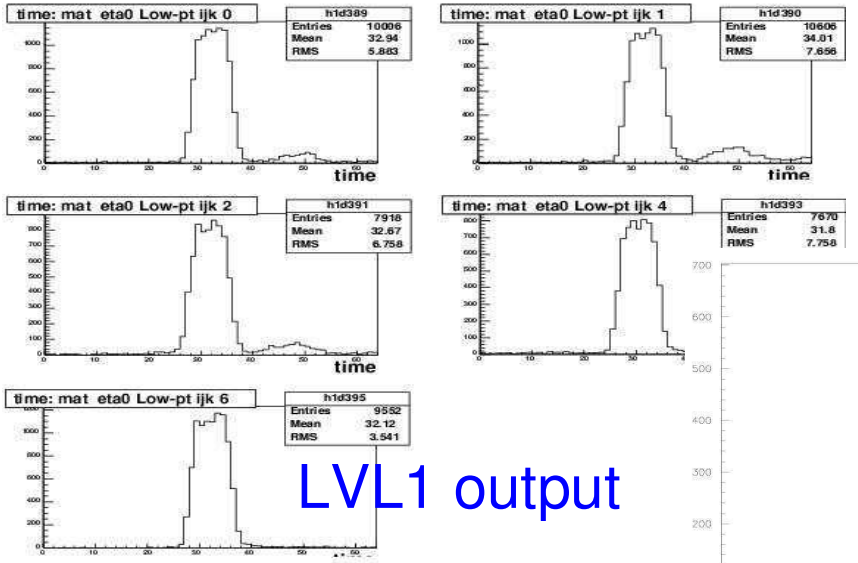
Examples of results from RPC trigger at test-beam

3D-track reconstructed with RPC and MDT data



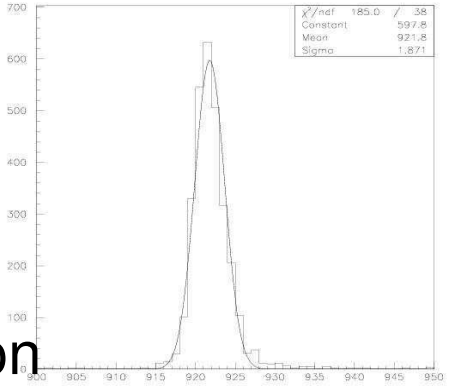


Beam profile reconstructed by CM and TDC readout



LVL1 output

Low-Pt raw data (two doublets) and trigger output time measurement (time unit is 1BC/8)

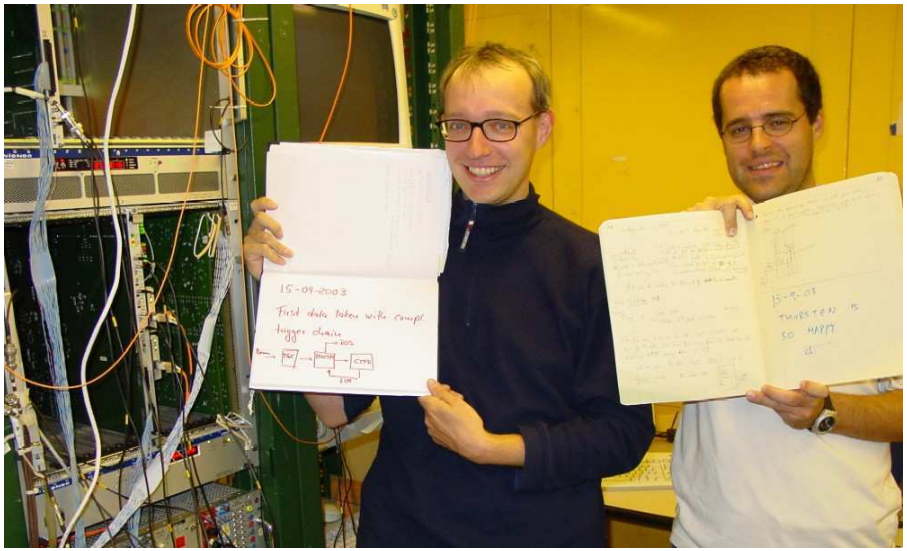


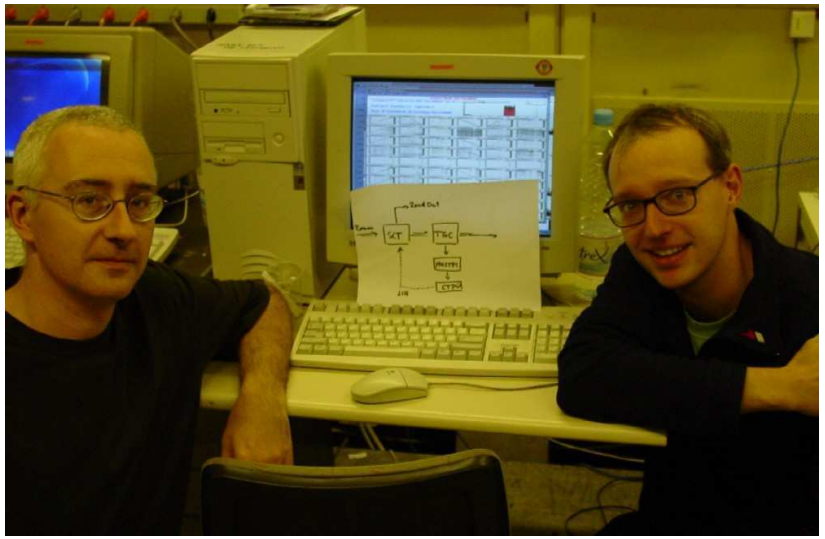
σ=1.9ns

CM-TDC comparison

MUCTPI and CTP at the H8 test beam

- Prototype deployed in H8 test beam in May & September
  - Input from TGC Slave Board
  - First successful run with TGC-MUCTPI-CTP trigger chain and TGC-MUCTPI-CTP-SCT readout chain on Tuesday (~2.2 μs total latency)
  - Will be used again in 25 ns run this week in flagging and triggering mode.

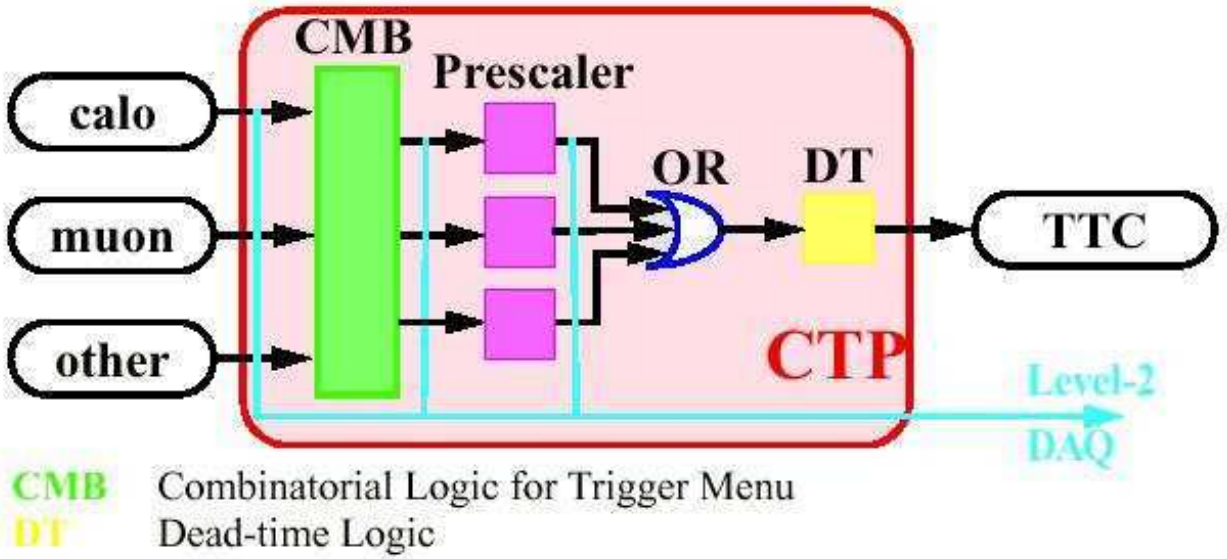




Conclusions

- System tests are in progress on End-cap and Barrel subsystems:
  - All TGC problems found during previous 25 ns run have been solved
  - TGC full slice + MUCTPI + CTP succesfully tested with standard beam this week
  - Four-week running of RPC on-detector readout and trigger electronics, integrated with MDT. Delays due to overcosts have not seriously affected system tests at H8.
- Milestones
  - October 2006: full LVL1 System available
  - August 2006: Endcap Muon LVL1 System available
  - December 2005: Barrel Muon LVL1 system available
  - June 2005: MUCTPI available
  - March-November 2005: Muon Barrel trigger commissioning
  - Summer 2004: full LVL1 slice test in H8 Combined run.

CTP



- Old demonstrator prototype installed in H8
  - Will use MUCTPI input and TGC data
  - Hope to use in flagging and in triggering mode in 25 ns run
- Final design follows MUCTPI development.
- Final Design Review early next year
- Full system and combined test-beam run next summer