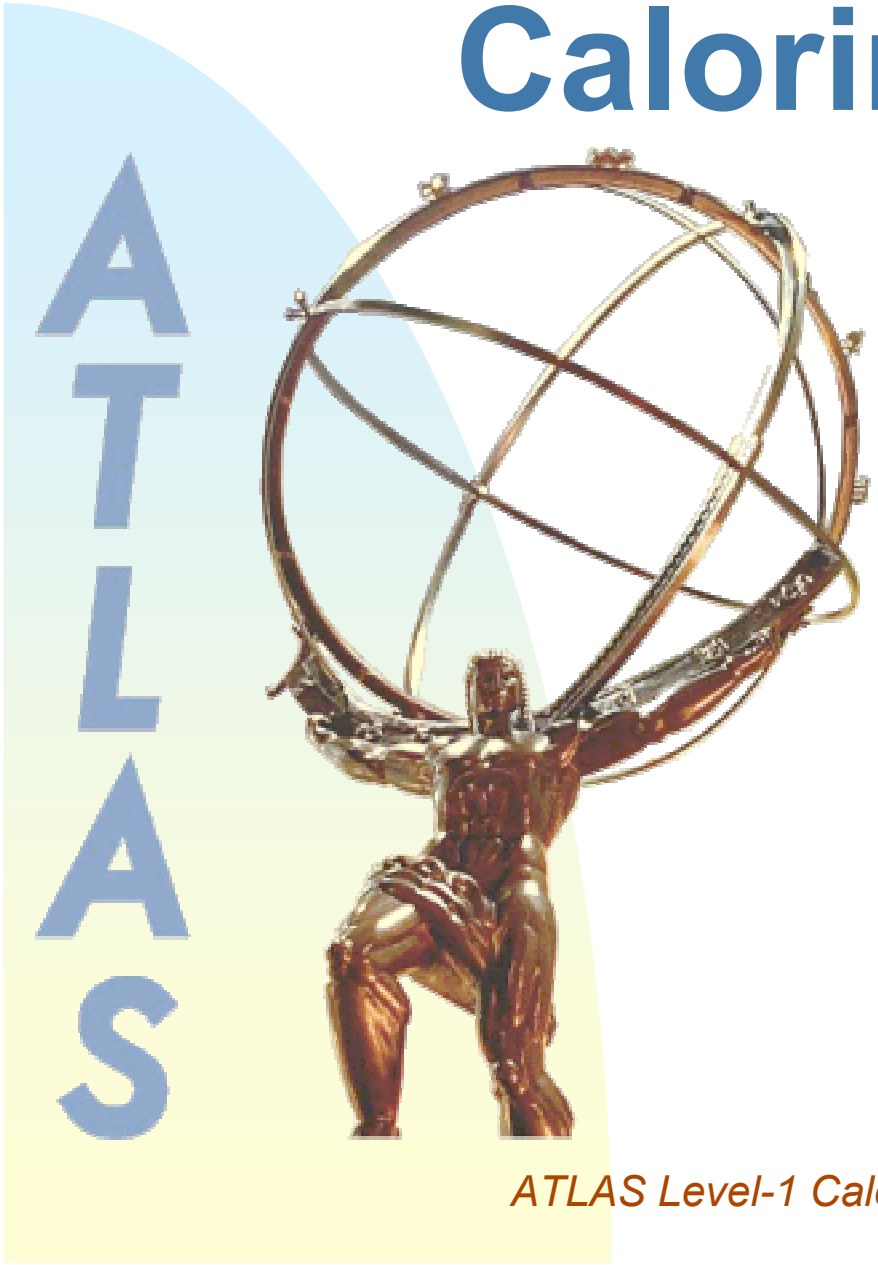
ATLAS Level-1 Calorimeter Trigger Architecture



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On behalf of

The ATLAS Level-1 Calorimeter Trigger Collaboration

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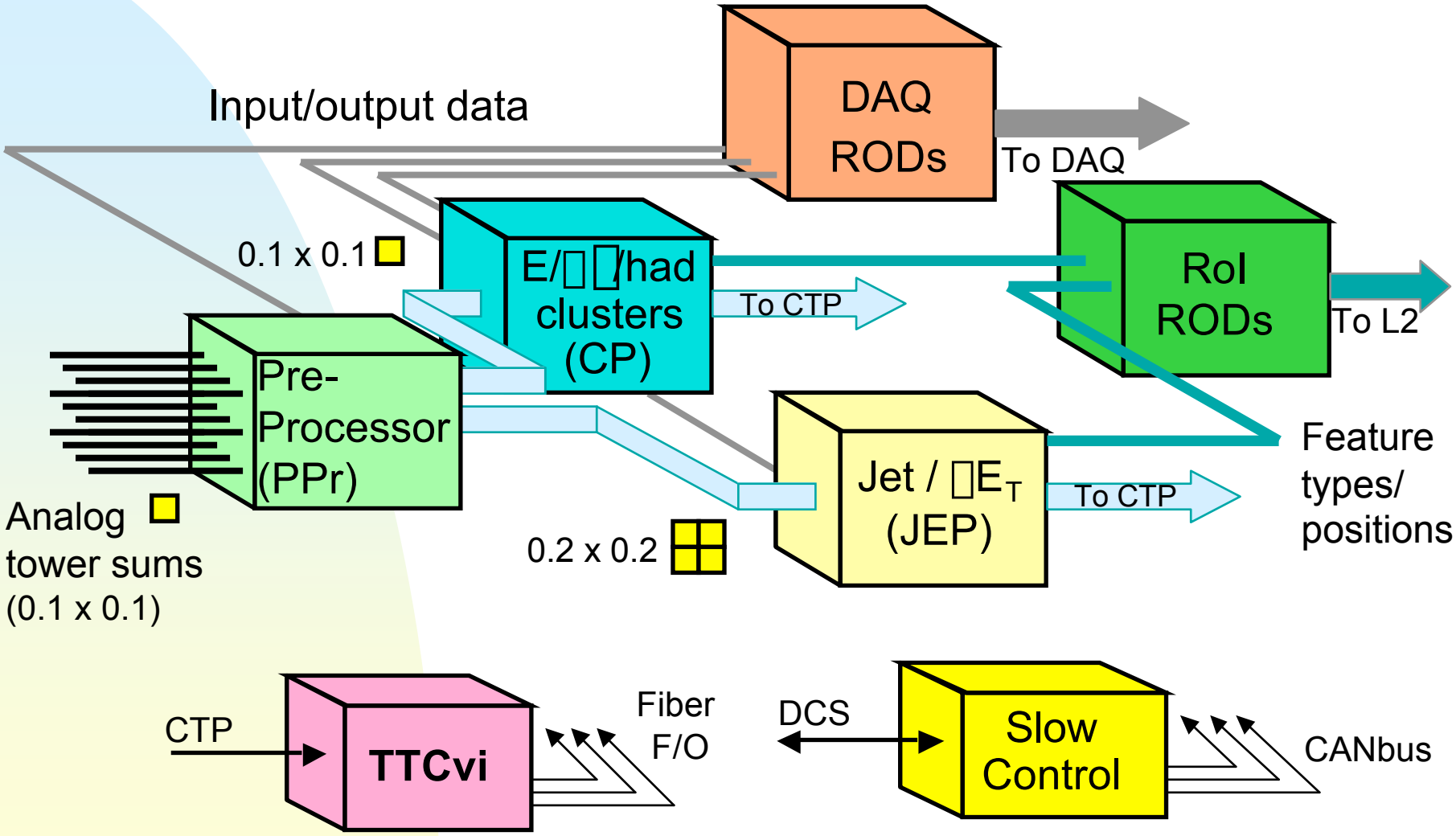
ATLAS Level-1 Calorimeter Trigger Architecture

L1 Calorimeter Functions

- Receive and digitize ~7200 analog trigger tower sums from the calorimeters
- Report to central trigger processor (CTP):
  - Multiplicities of high-energy electrons, photons and hadrons
  - Multiplicities of jets
  - Sum and missing E_T
- Report “Regions of Interest” to Level 2:
  - Positions and types of jets, e/□ and □/had clusters

L1Calo system overview

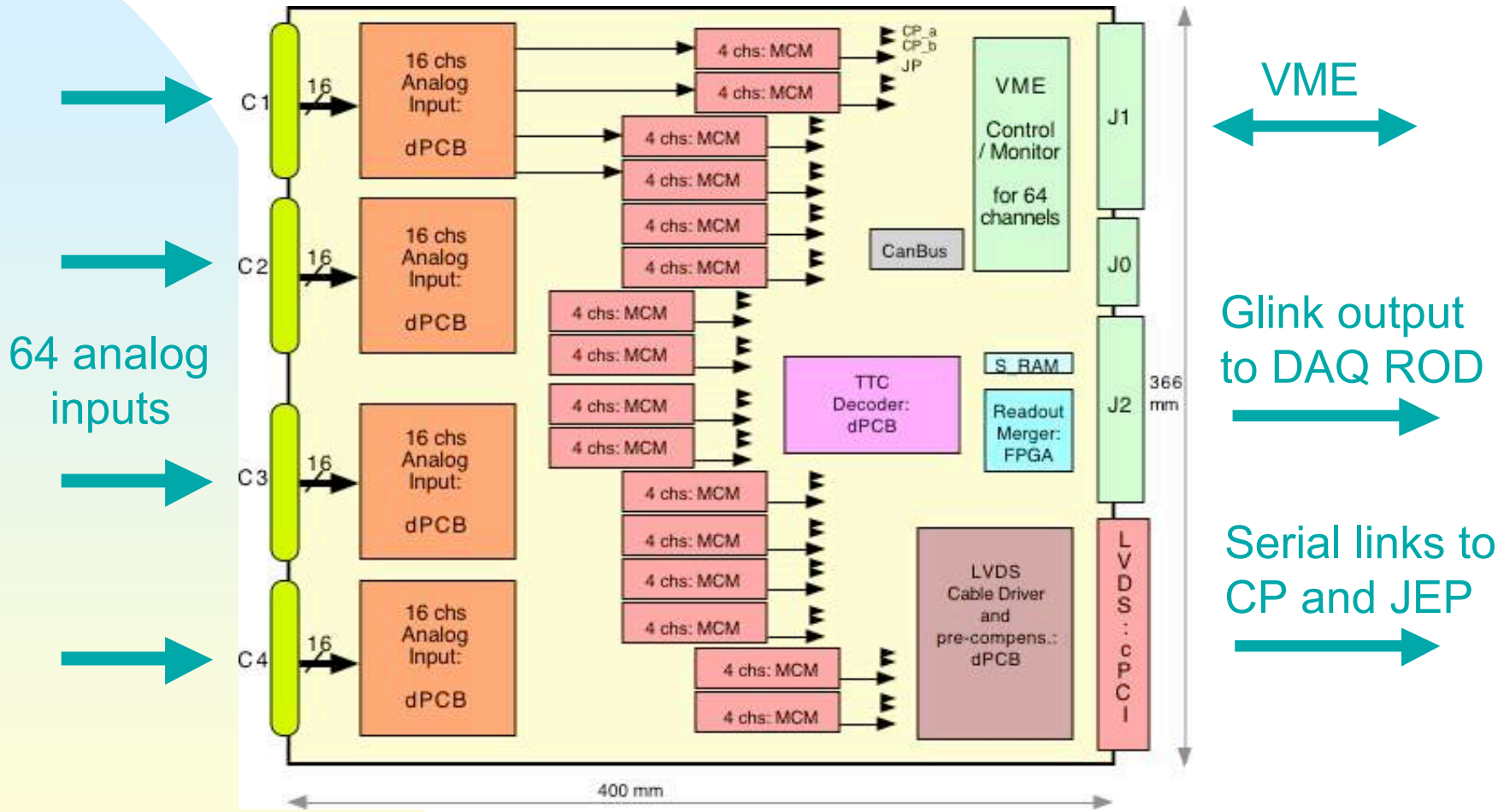


ATLAS Level-1 Calorimeter Trigger Architecture

“Evolution” of L1Calo system

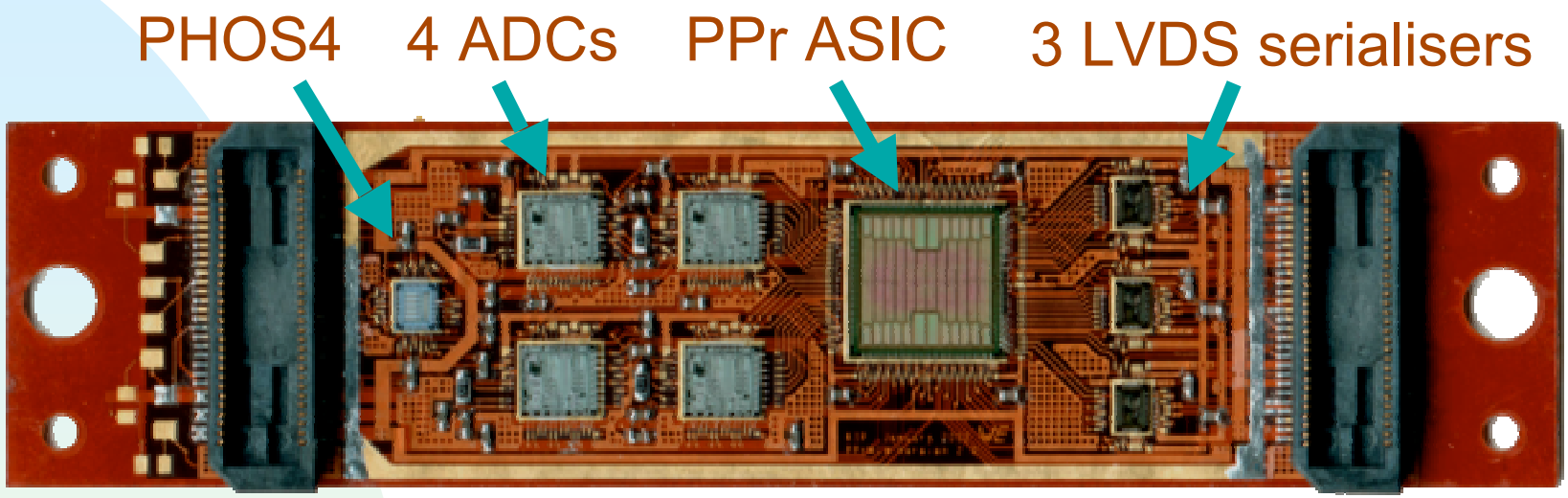
- Compact system architecture
  - Minimize number of crates, racks
  - Fewer, shorter cable links
  - Benefits in cost and latency
- Common hardware modules
  - Processor backplane, crate/system level merging, TTC and slow control interface, readout to DAQ and Level-2 (RoI)
- Robust / reliable / simple maintainance

PreProcessor Module



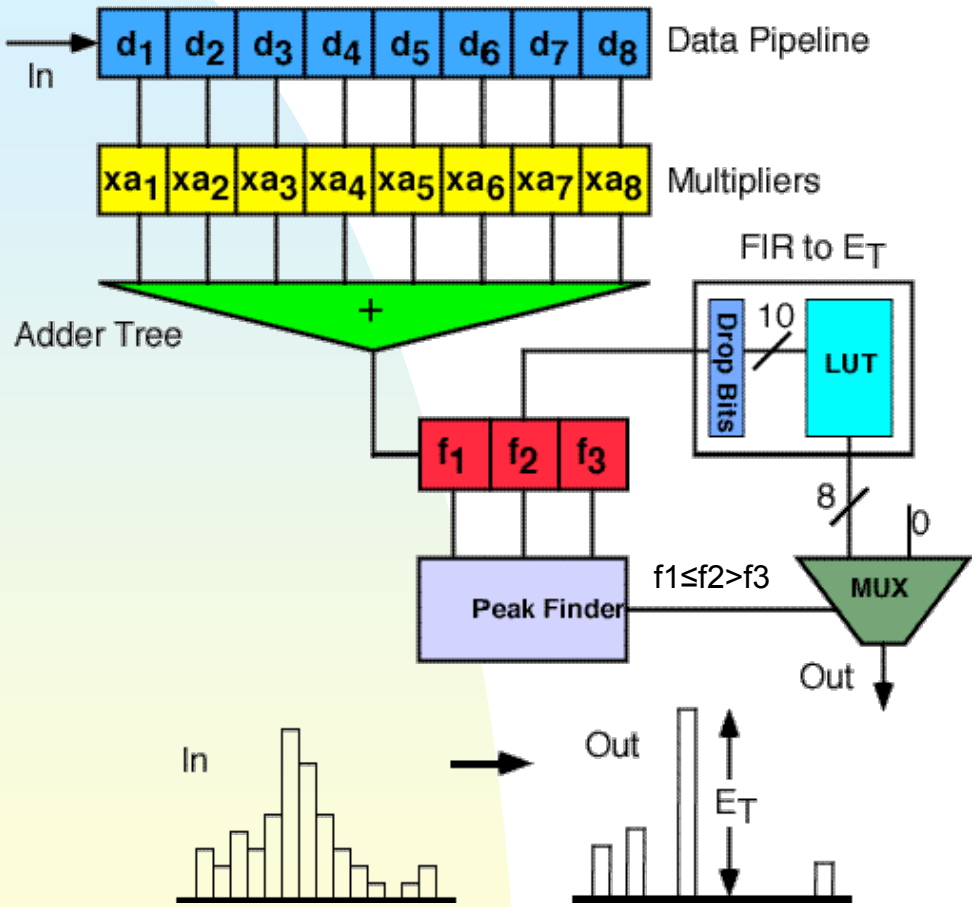
ATLAS Level-1 Calorimeter Trigger Architecture

PreProcessor MCM



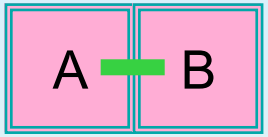
- Digitise and process 4 em or had channels
- Output via 3 LVDS serialisers (400 Mbit/s each)
  - 4 CP outputs on two serialisers using “BC-mux”
  - 1 Jet element (9b sum) on one serialiser

BCID Algorithm in PPr

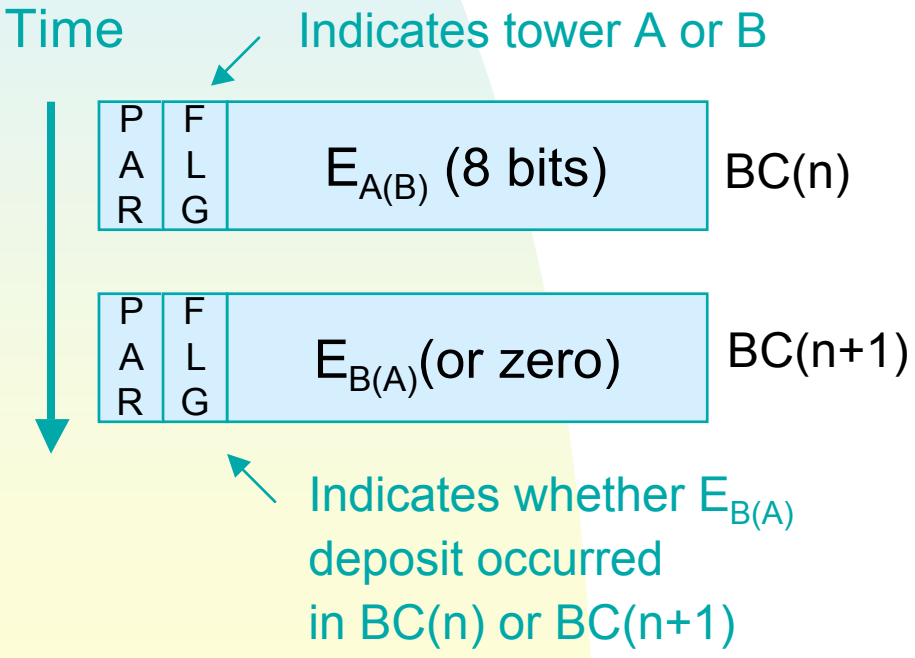


- E_T extraction uses FIR filter + lookup table
- Bunch crossing ID found from peak in FIR filter output
- Note: occupied BC always followed by a zero BC

Bunch crossing multiplexing (BC-mux)



Towers are paired. Let a tower have non-zero deposit in bunch crossing BC(n):

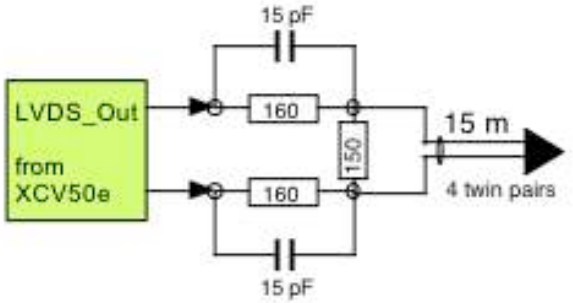


- Tower with non-zero energy reported in BC(n), FLG identifies which tower (A or B)
- Other tower reported in next BC. FLG gives BC of that tower deposit.
- If A and B both occupied, E_A reported first
- Multiple uses of FLG bit

LVDS Precompensation

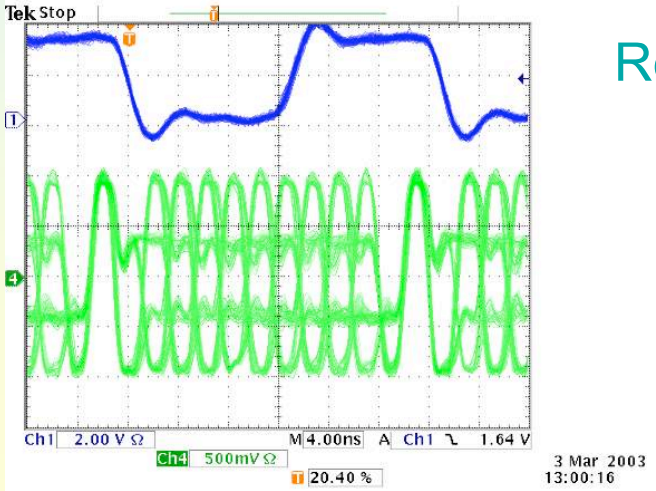
- Compensate cable distortion using passive components at transmitter
- Result: cable range extended to at least 15m (<10^{-14} bit error rate)

Precompensation circuit:

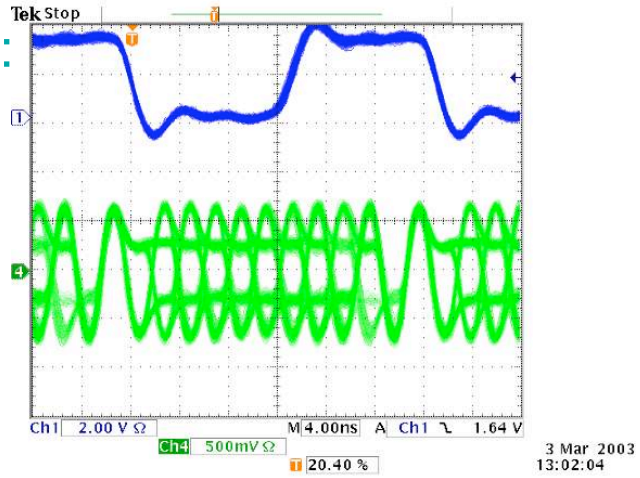


1□ 2 fanout at 400 Mbit/s
Using Xilinx Virtex FPGA

Transmitter:

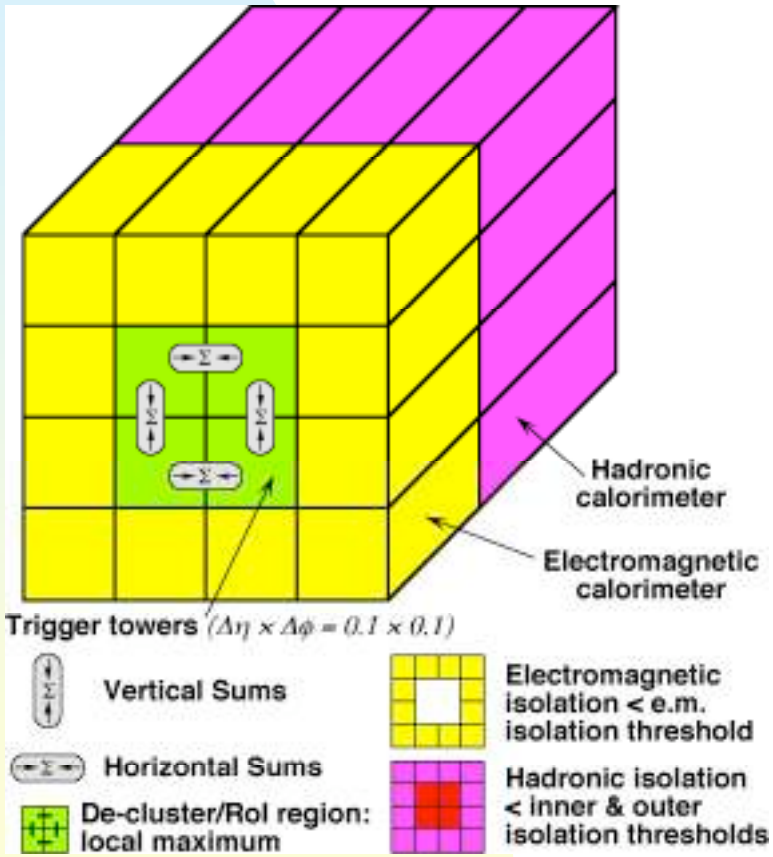


Receiver:

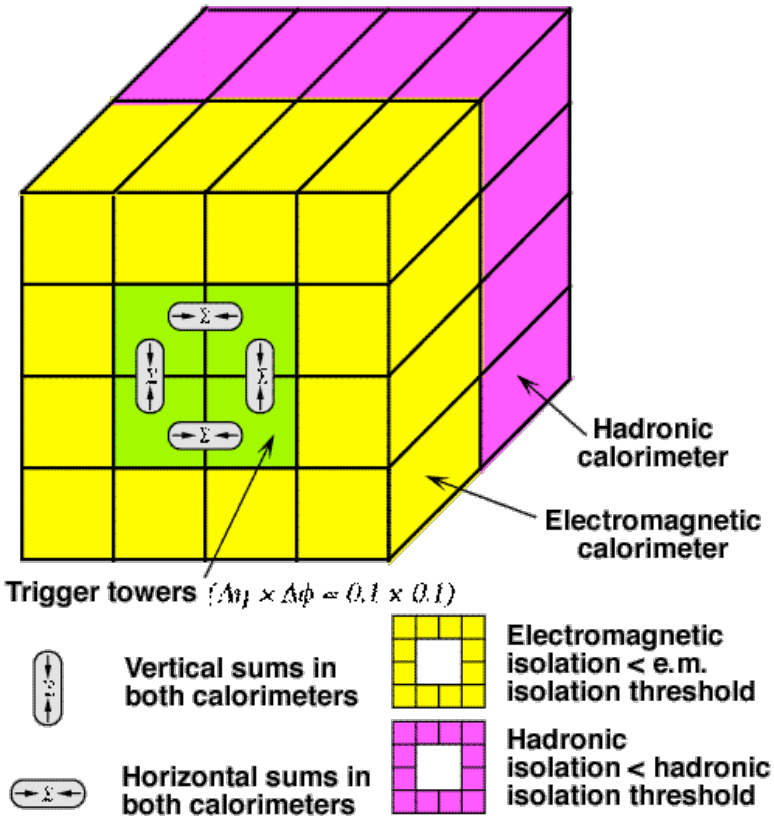


Cluster Algorithms

e/

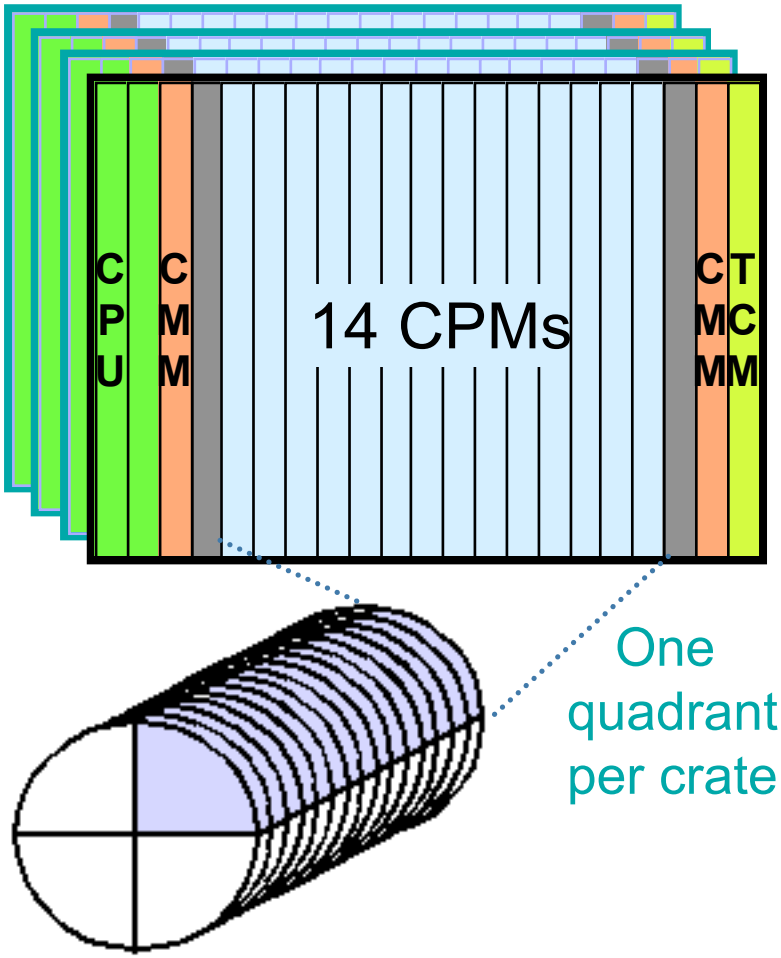


/had



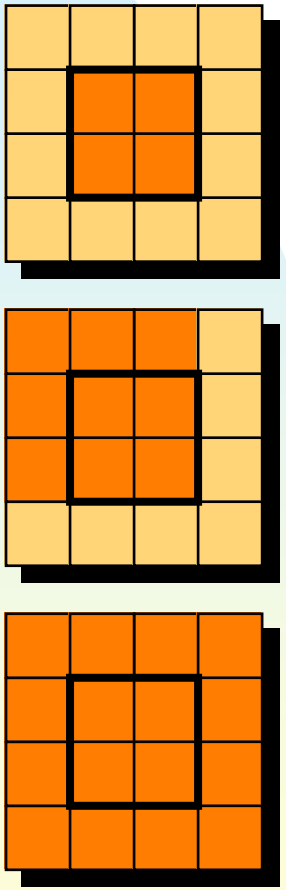
Cluster Processor Subsystem

Cluster Processor Module (CPM)



Note: quadrant layout minimizes cable fan-out from PPr

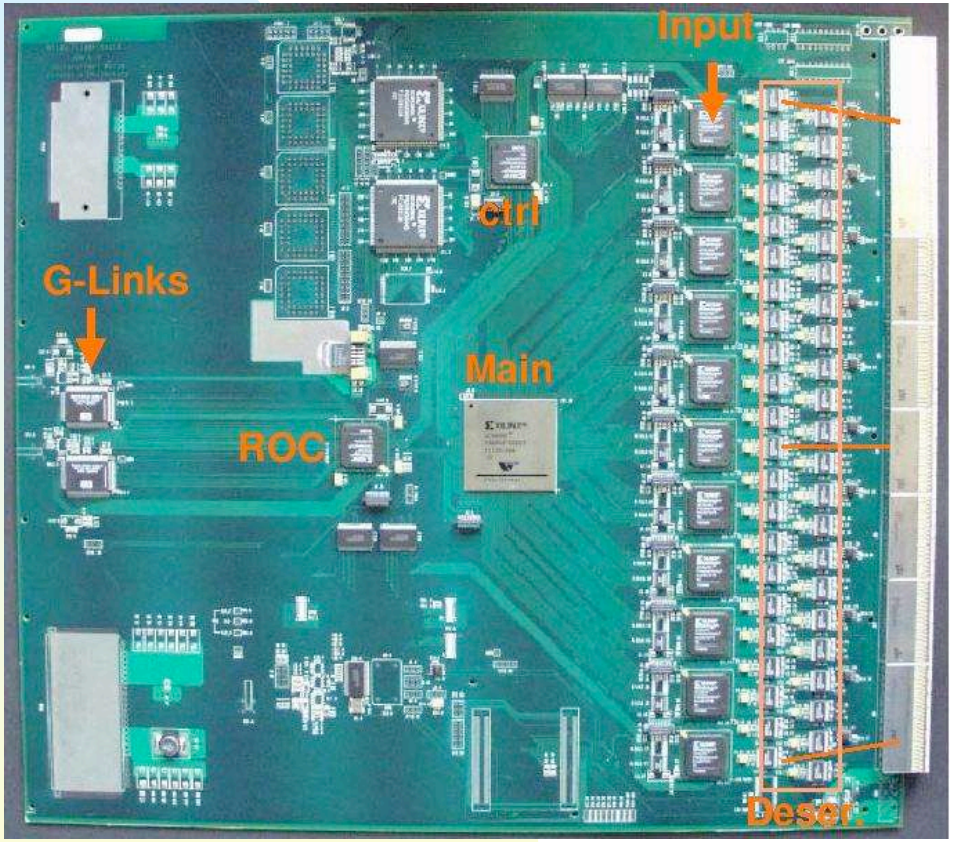
Jet Algorithms

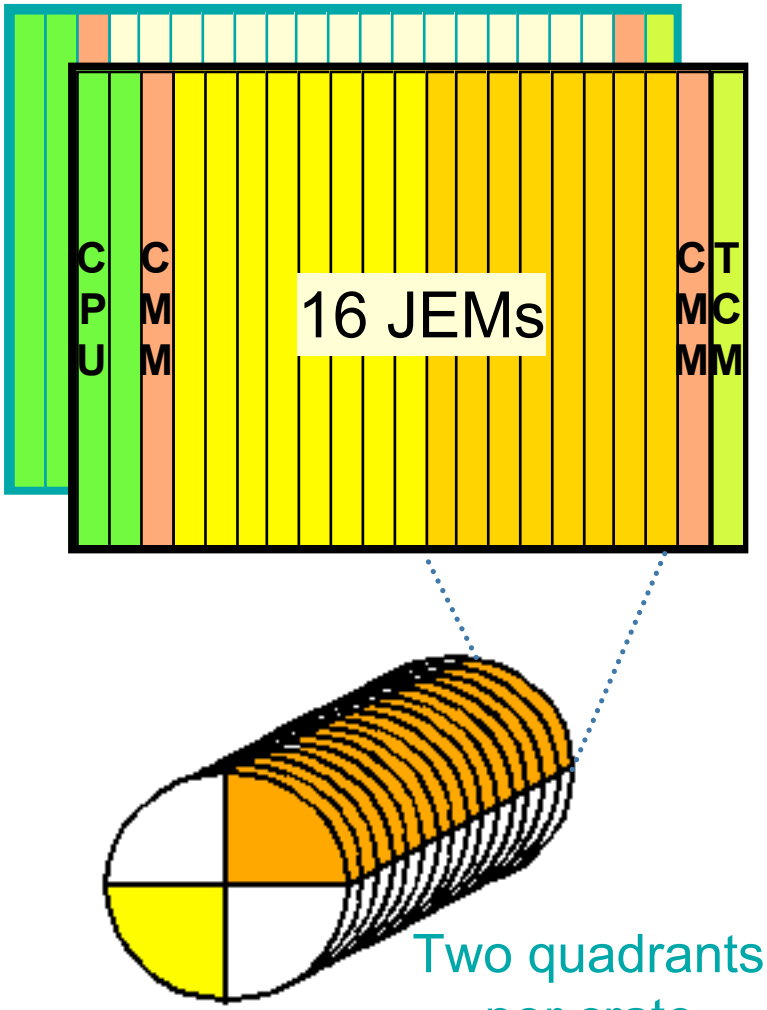


- Programmable choice of three jet cluster sizes around 0.4□0.4 local maximum
- Jet window moves by 0.2
- 8 independent, programmable jet thresholds
- Each threshold comprises an energy value and cluster size

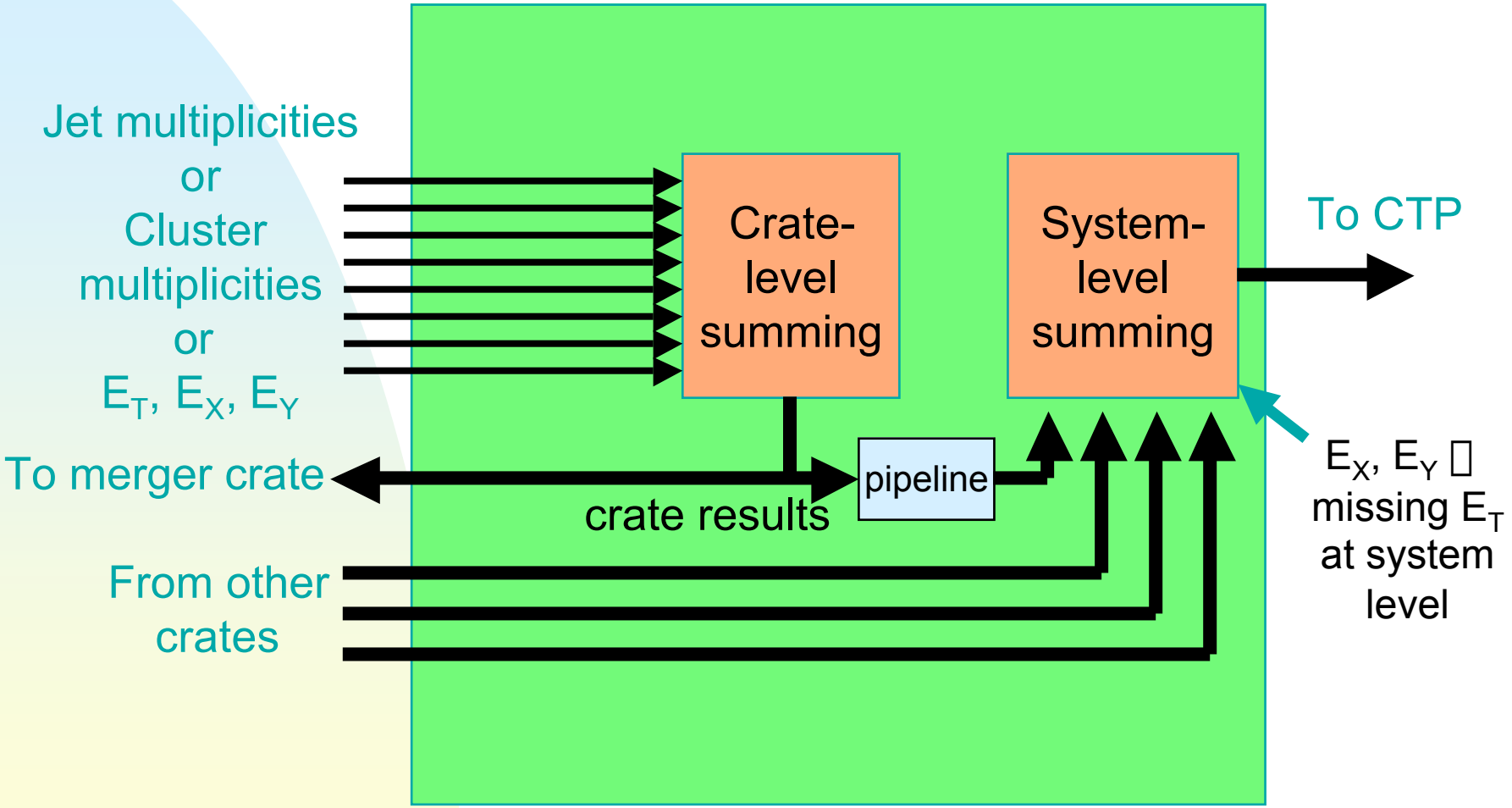
Jet/Energy-sum Subsystem

Jet/Energy Module (JEM)

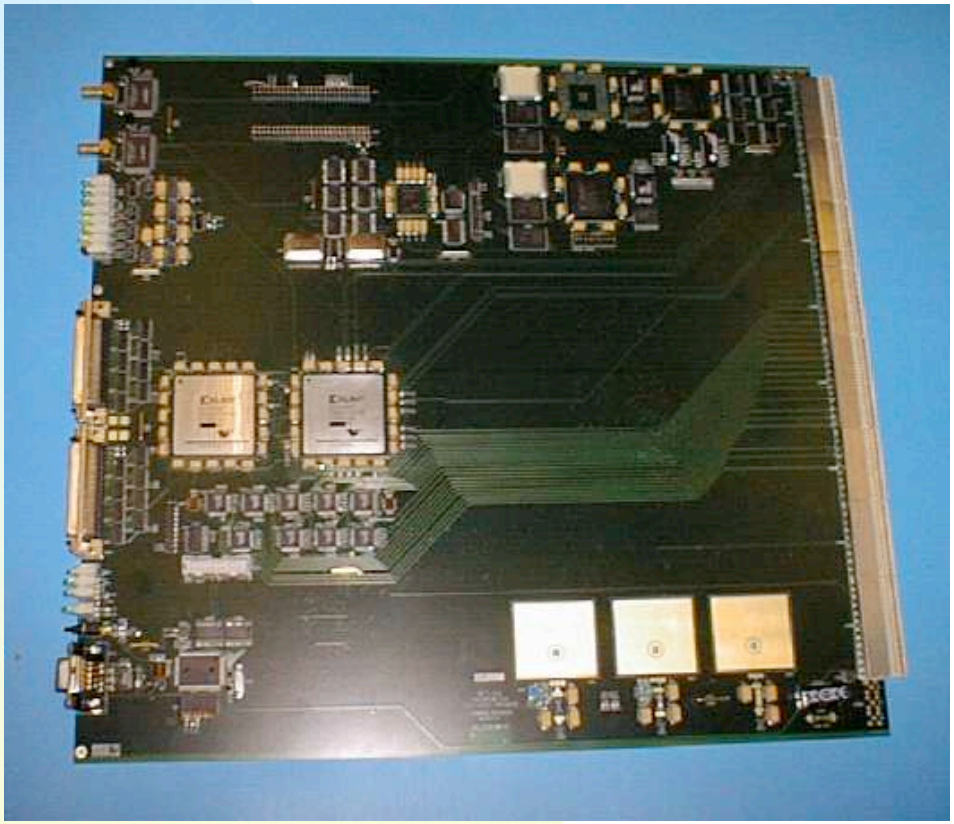




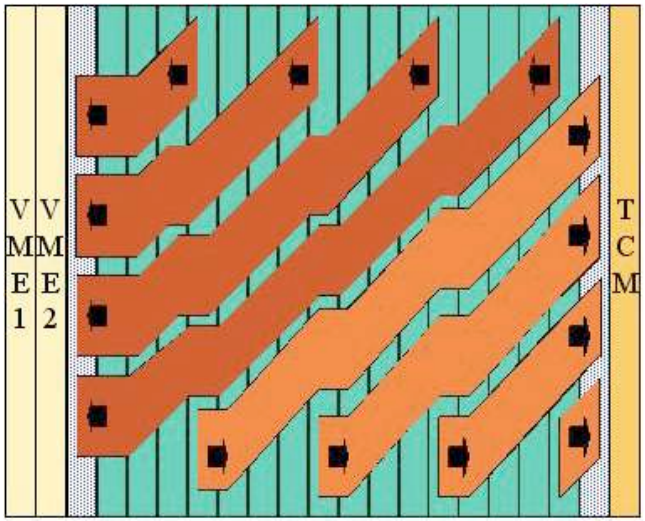
Merging processor results



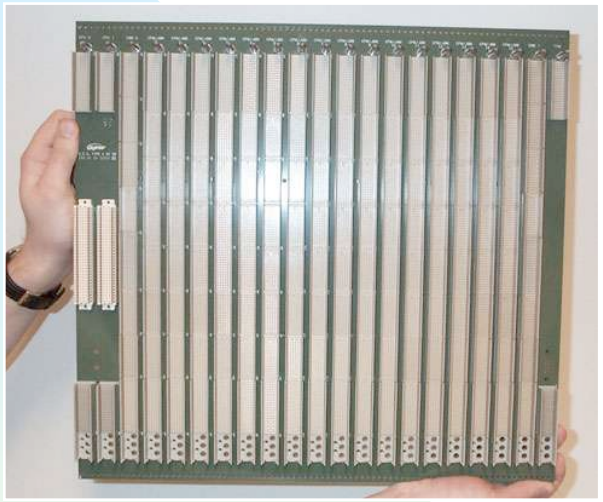
Common Merger Module



- Same module hardware design merges cluster, jet, and energy results
- Crate-level merging over backplane:



Processor Backplane

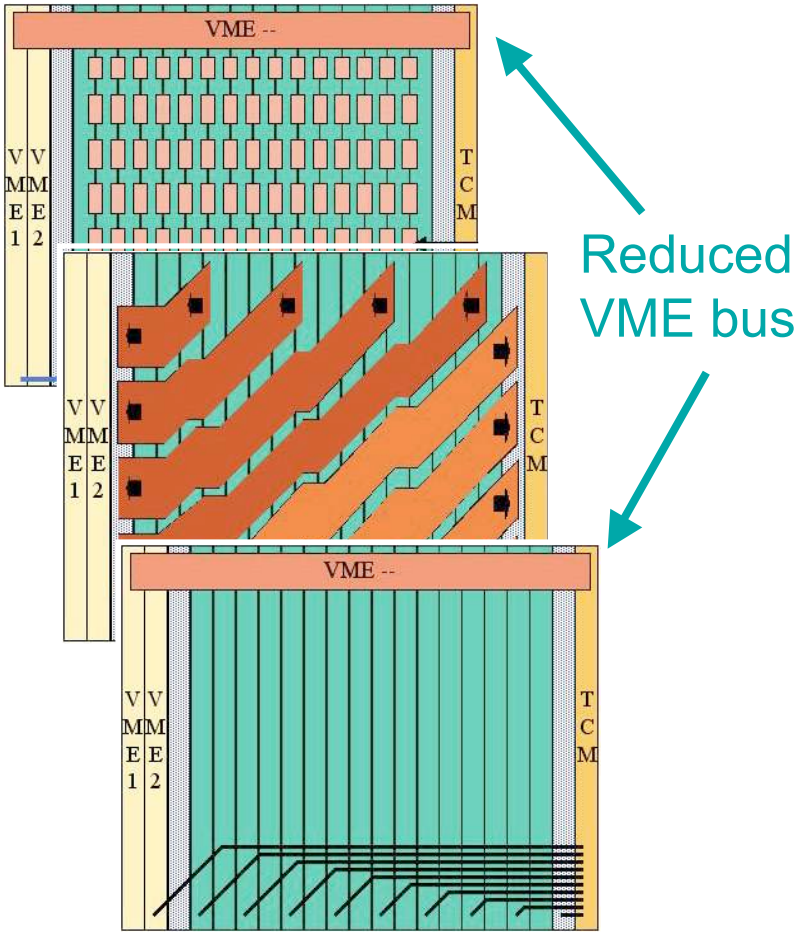


18 layers, 8 signal layers:

2 fan-in/out:

4 merger:

2 TTC fanout:

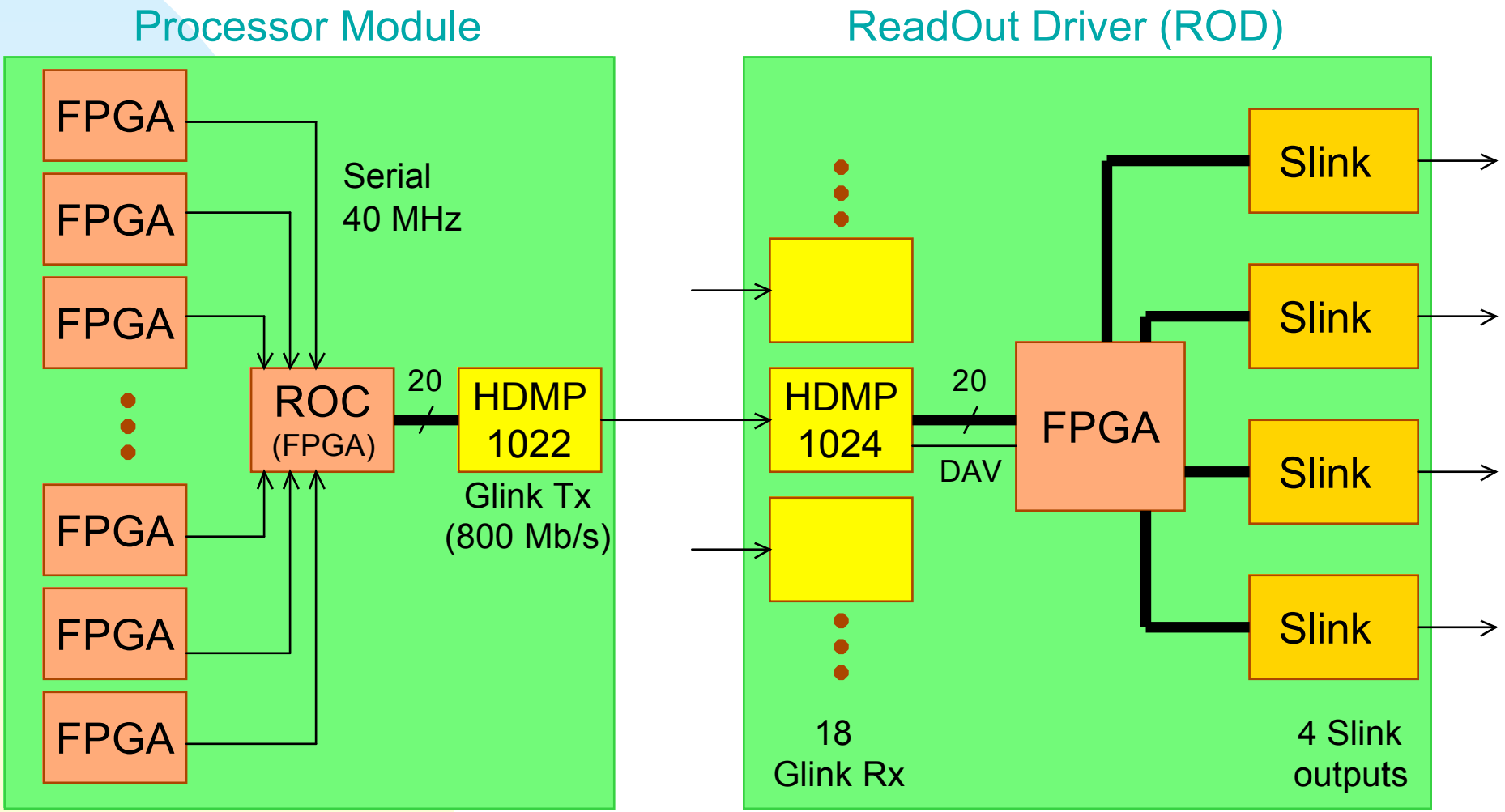


Reduced VME bus

Important backplane features

- LVDS links and merger interconnect cables connected to modules through backplane
  - Few front-panel cables
  - Less recabling over experiment lifetime
- Extended geographic addressing
  - Modules know position *and* crate number
  - Use to set unique VME, CAN and TTC addresses
  - Use to automatically load appropriate FPGA configurations on multiple-use modules

ReadOut Driver (ROD)



Prototype ROD

- Same ROD hardware for all DAQ and ROI readout
- Data compression, zero suppression, some monitoring
- 6U module
  - Final ROD will be 9U
- 4 Glinks in,1 Slink out
  - Final design 18 Glinks in, 4 Slink outputs out

Summary

- Compact system architecture
  - 8 PreProcessor, 4 CP, 2 JEP crates
  - Minimizes cost and latency
  - Number of cables to CP halved by BC-mux
- Several common hardware solutions
  - Economy in cost, design effort, spares
- Robust / reliable / simple maintainance
  - Serial link reliability enhanced
  - Few front panel cables on CP, JEP subsystems
  - Self-configuring modules with geog. addressing