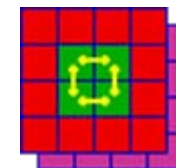




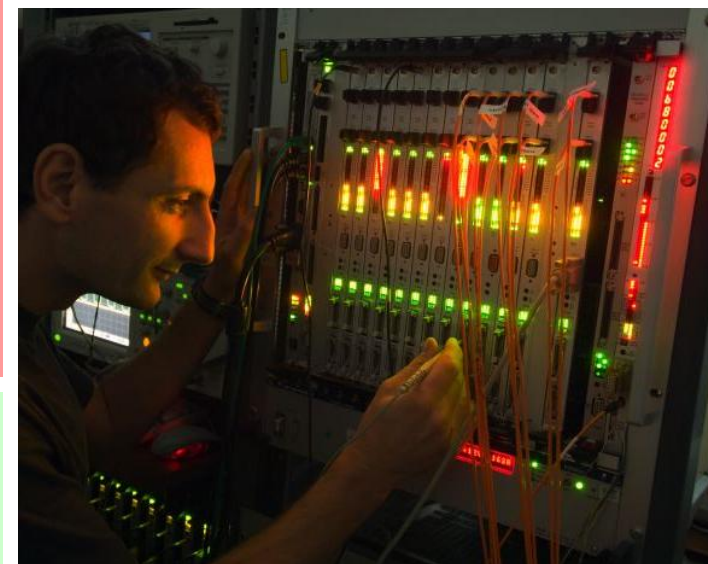
Commissioning Experience with the ATLAS Level-1 Calorimeter Trigger System



ATLAS Level-1 Calorimeter Trigger Collaboration



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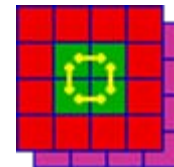
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Commissioning of ATLAS Level-1 Calorimeter Trigger, Stephen Hillier



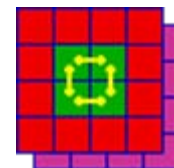
Commissioning Experience with the ATLAS Level-1 Calorimeter Trigger System



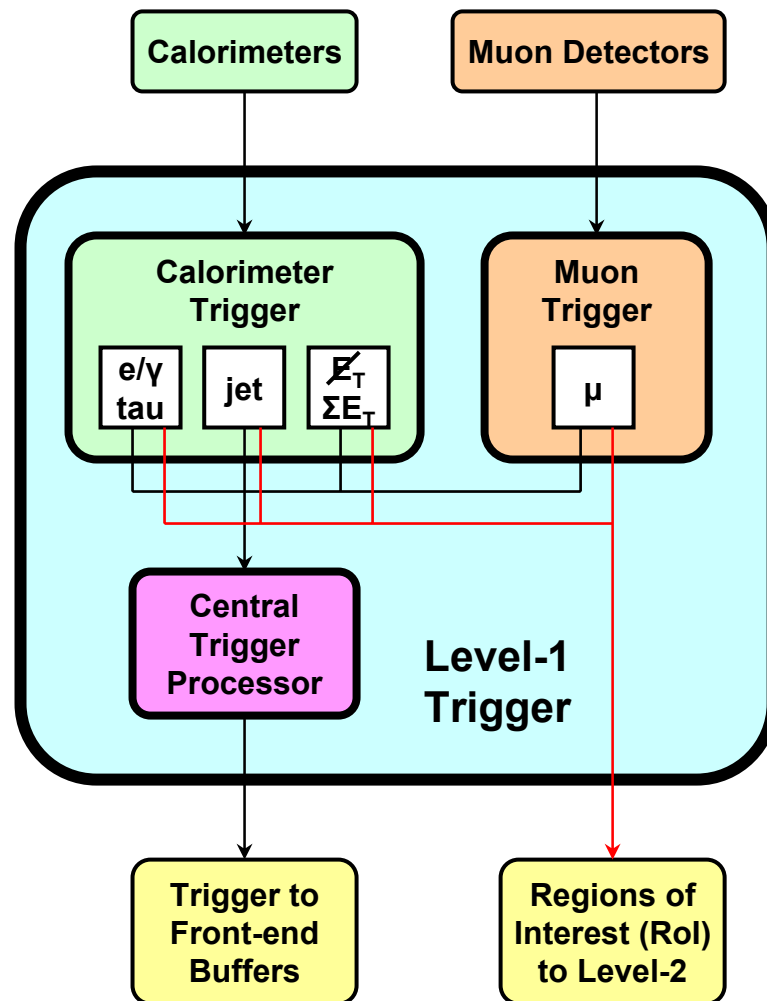
- Trigger Architecture
- Challenge of Scale
 - Rationale for architecture and size
 - Implications for Installation
 - Full scale crate tests
- Commissioning and Integration
 - Integration into ATLAS Data Acquisition
 - First signals from Calorimeters



Level-1 triggering in ATLAS

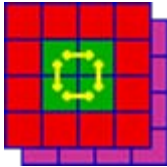


- Three-stage triggering system
 - Level-1: custom-built hardware, fixed latency - target rate 75 kHz
 - Level-2: mostly software, RoI-based selection - target rate 1000 Hz
 - Event Filter: software, full detector - target rate 200 Hz
- All data buffered at bunch-crossing rate of 40 MHz for 2.5 μ s
- Level-1 has three sub-systems:
 - Calorimeter Trigger
 - Muon Trigger
 - Central Trigger (CTP)

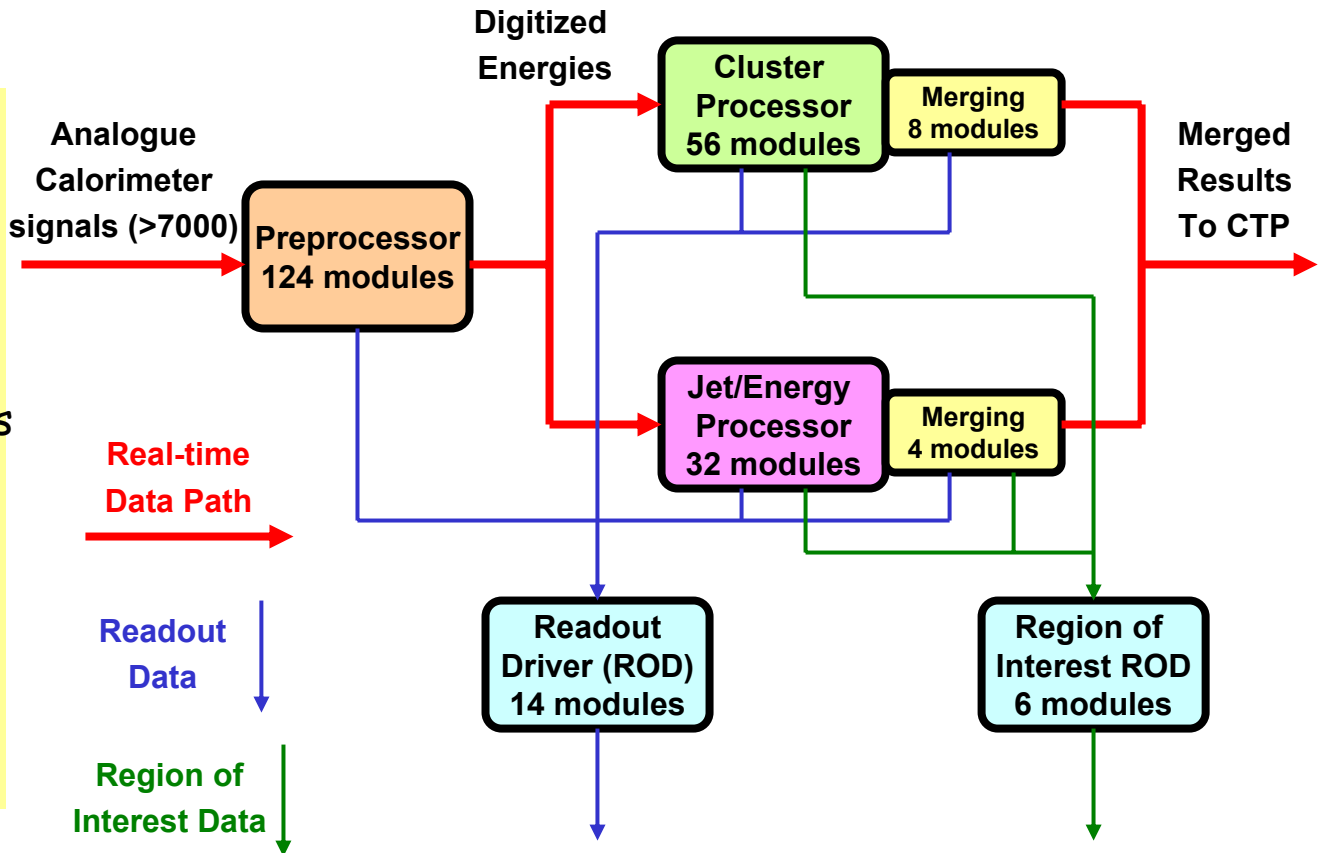




Calorimeter Trigger Architecture



- Features:**
- Real-time Path: Fixed Latency ($\sim 1\mu\text{s}$)
 - Many processing stages
 - Massive parallelism
 - Multi-purpose modules
 - Heavily FPGA based

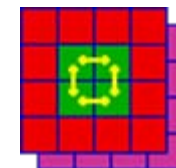


Five Main Types of Custom 9U Modules

PPM	CPM	JEM	CMM	ROD
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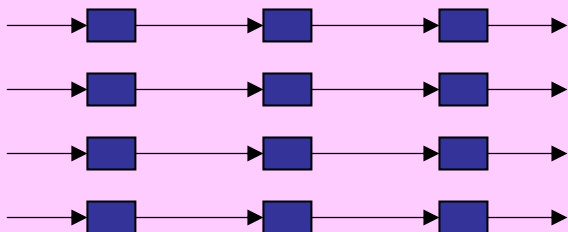


Compromise of Scale



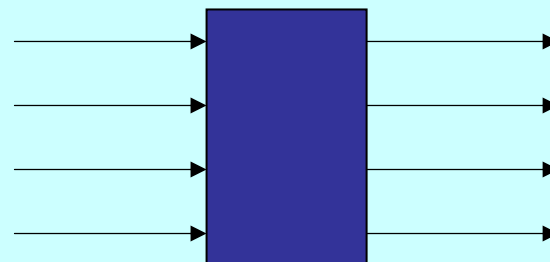
Main motivations leading to:

Extensive Parallel System



- Physical Size of Connectors
 - e.g. 496 inflexible analogue cables with large connectors
- Quantity of processing
- Power consumption

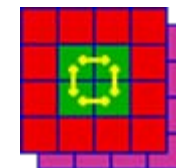
Compact Integrated System



- Latency
- Fewer data transmission stages
- Algorithm Environment
 - Sharing of information leads to extensive fanout/fanin

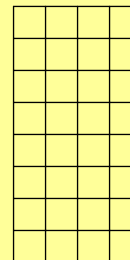


Influence of Overlapping Windows in Physics Algorithms

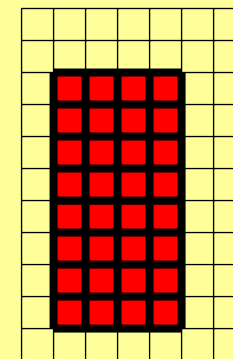
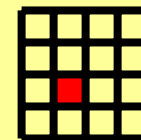


- Processor input is a matrix of tower energies
- Physics algorithms use 4x4 grid
 - 2-D pattern recognition
 - Applied throughout full input matrix
 - Windows overlap in both coordinates (eta and phi)
- To process each location, an outer 'environment' is required
- Each processor (module, crate) has a core of towers processed
- Extra 'environment' achieved by fanout
- Ratio of core:environment dependent on size
 - More parallel processing in smaller regions increases fanout requirements
 - Sub-dividing makes connectivity more difficult

Jet/Energy
Module Core



Algorithm
Environment



32 Core cells

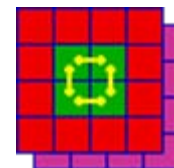
45 Environment
cells

jet/energy-sum module (4x8) 32:45

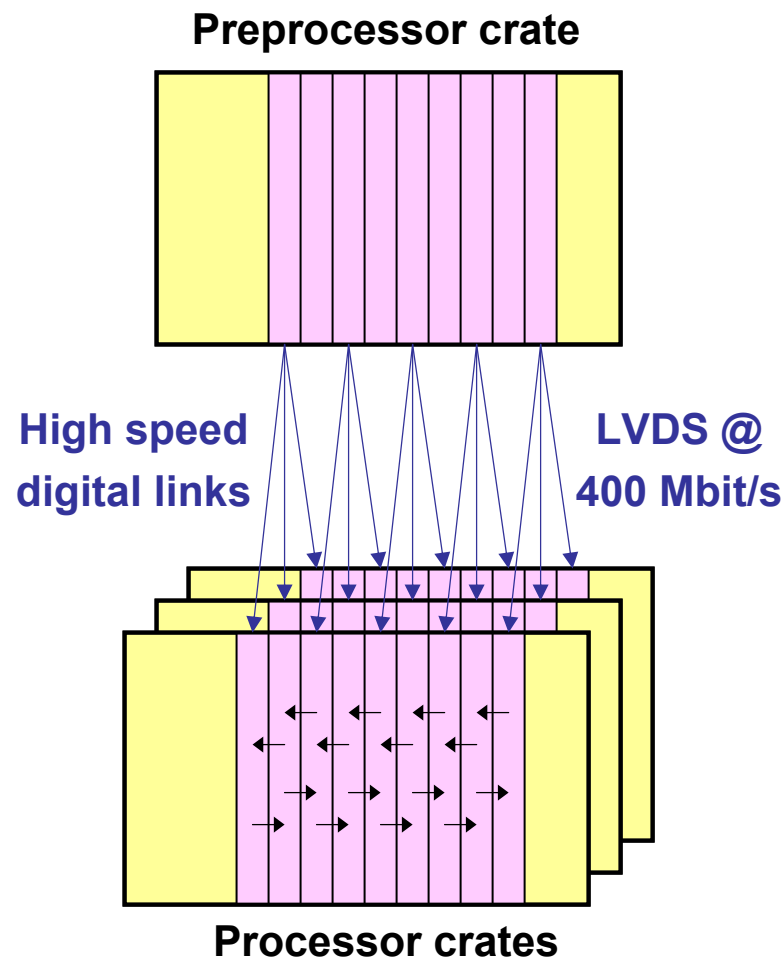
e/gamma/tau cluster module (4x16) 64:69



Solution and implications

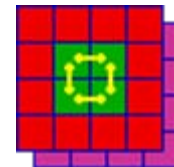


- Entirely Parallel Preprocessor
 - Size matches input cable connectors
 - Eight 9U VME crates
- High bandwidth digital cabling 'spaghetti' to:
- Parallel Processor
 - Four 9U VME crates for e/gamma/tau trigger
 - Two 9U VME crates for jet/energy-sum trigger
- Necessary fanout performed via:
 - Digital cables to processors
 - ~25% of duplication required
 - In one plane (fanout in phi)
 - Custom backplane in processor
 - ~75% of duplication required
 - In other plane (fanout in eta)





Installation Reality Check: Input Analogue Cables



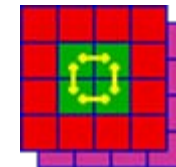
496 cables into 8 crates
Four cables just fit front of one 9U module



Commissioning of ATLAS Level-1 Calorimeter Trigger, Stephen Hillier



Installation Reality Check: Digital Cabling into Processor Crates



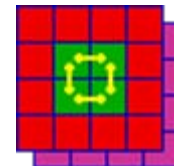
Up to 1400 individual LVDS
signals into one crate

More than 500 Gbit/s data input

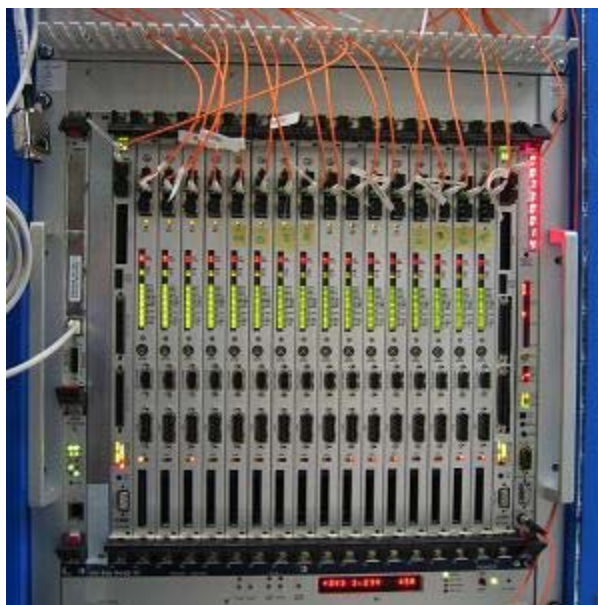




Full Scale Crate Tests



- Comprehensive tests performed with all subsystems
- Performance scaled well
- One new hardware problem:
 - Processor backplane

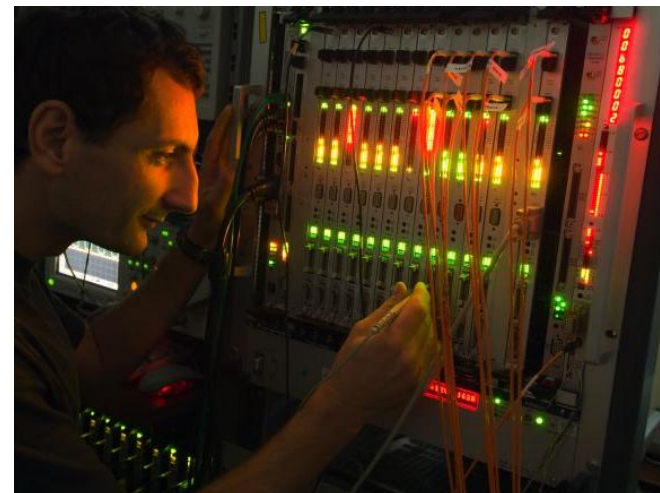


Preprocessor



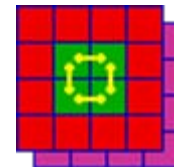
Jet/Energy Processor

Cluster Processor

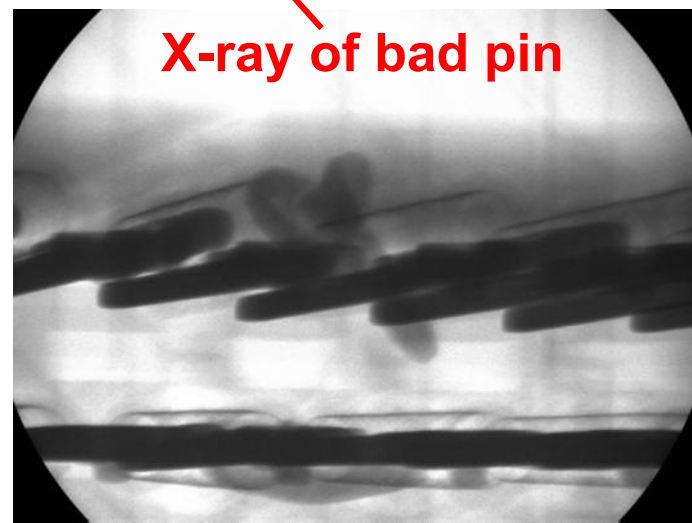
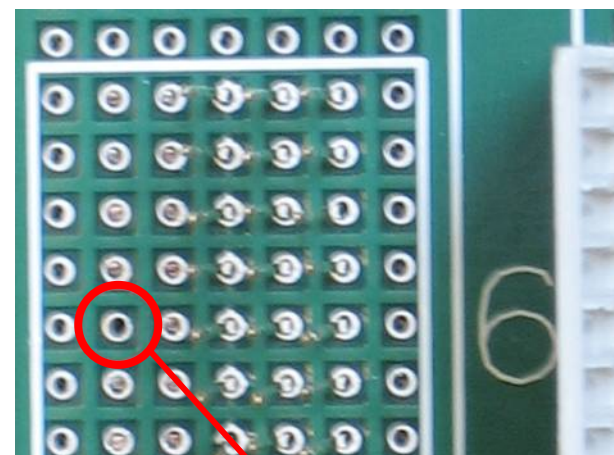




Backplane Problems and Status

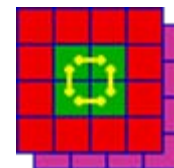


- Dense, high bandwidth backplane
 - Up to 1150 pins per slot
 - About 22,000 pins in all
- After production, pin problems at $\sim 0.01\%$ level
 - ie about 1-2 errors per backplane!
- Pins bent during insertion of connectors
- Currently in process of replacing bad connectors

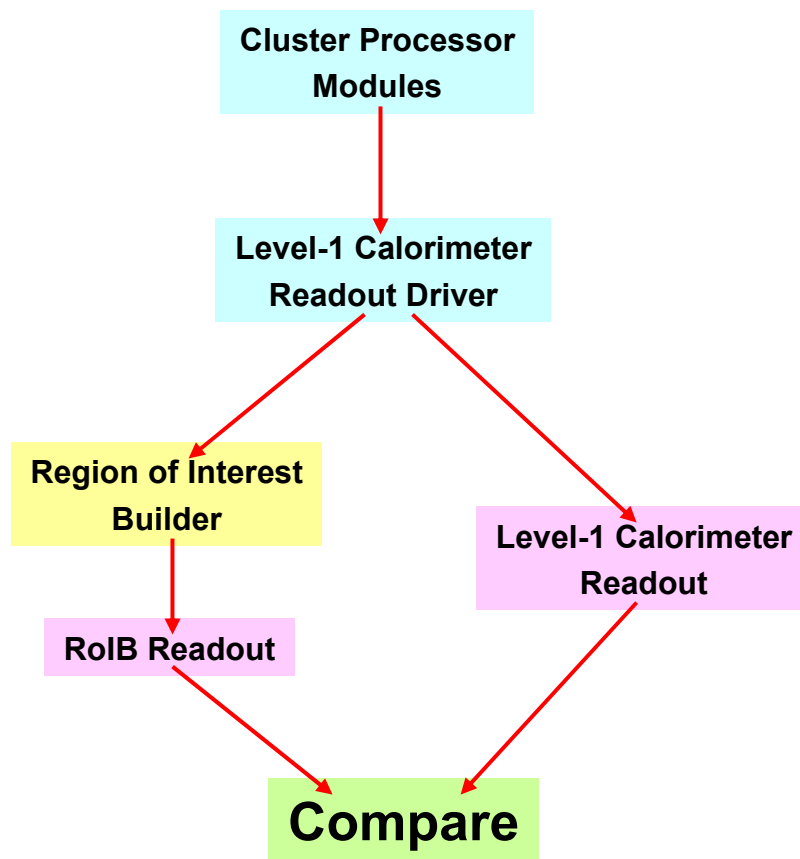




Integration into ATLAS Data Acquisition

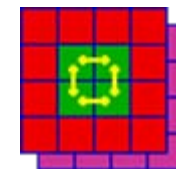


- Tests of output to all downstream hardware performed in situ
 - Simple setups for the moment
- Links to Readout System and Region of Interest Builder showed no data corruption
 - Tested at high rates
- Real-time links to Central Trigger Processor mostly fine
 - Minor problems
 - Now found and fixed





First Signals from Calorimeters



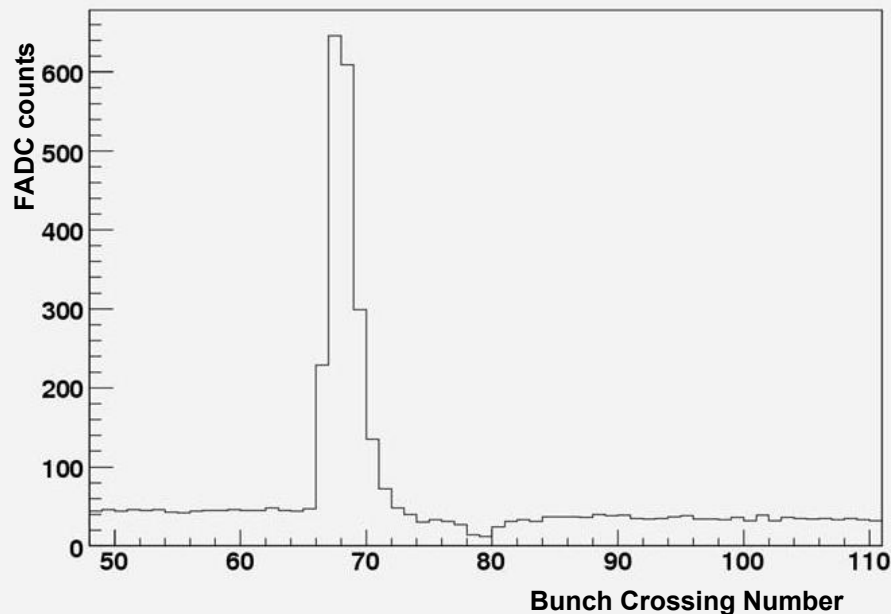
Installation at ATLAS allows:

First opportunity to see calorimeter signals since test-beam in 2004

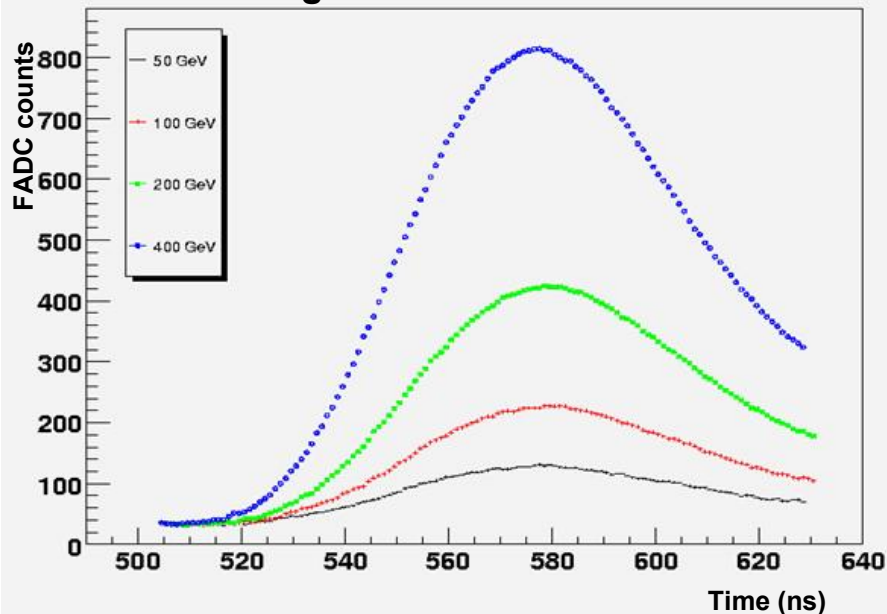
Investigation of channel connectivity, signal quality, and tower calibration

(Using calibration systems)

Input pulse as seen by Preprocessor FADC

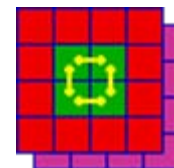


Timing and calibration scans





Future Plans



- More integrations
 - Connect up full scale subsystems
 - Further calorimeter tests
 - More channels
 - Different parts of detectors
 - Join ATLAS combined runs
 - Commissioning runs
 - Cosmic runs
- Majority of hardware installed by mid-2007
- Will require much work to fully understand system