# Test results for the Jet/Energy Processor of the ATLAS Level-1 Calorimeter Trigger

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## *Abstract*

The Jet/Energy Processor (JEP) is one of three processing units of the ATLAS Level-1 Calorimeter Trigger. It identifies and finds the location of jets, and sums total and missing transverse energy information from the trigger data. The Jet/Energy Module (JEM) is the main module of the JEP. The JEM prototype is designed to be functionally identical to the final production module for ATLAS.

Two JEM prototypes (Module-0), which use the full number of channels and have all necessary interfaces, have been built and successfully tested. Various input test vector patterns were used to check the performance of the jet and energy summation algorithms. Data communication between adjacent JEMs and all relevant modules of the JEP has been tested. We present a description of the architecture, required functionality, and jet and energy summation algorithm of the JEM. Recent test results using the JEM prototypes are presented and discussed. Based on the test experiences and technology developments, the final modules, JEM Module-1, are under design.

## I. Introduction

A highly selective, efficient and flexible first level trigger system is vital to achieve the physics goals of the ATLAS experiment. The ATLAS Level-1 Calorimeter Trigger provides information for the Level-1 trigger decision by identifying and counting clusters in the calorimeter data [1]. They are considered candidates for jets, electrons/photons or hadronic taus. The total and missing transverse energy ($\Sigma E_T$ and $E_{T,miss}$) is calculated, which is an important signature for many interesting physics processes. The algorithms are implemented in two processor systems: The Cluster Processor (CP) and the Jet/Energy Processor (JEP) [2]. These two processor systems send results for every bunch crossing to the Central Trigger Processor (CTP) which makes a Level-1 Accept (L1A) decision based on them, including additional data from the Muon Level-1 Trigger system. The latency of the Level-1 trigger is limited to 2 $\mu$sec, which requires the system to use a reduced granularity of mainly $\Delta\phi \times \Delta\eta = 0.2 \times 0.2$ for the JEP, and $\Delta\phi \times \Delta\eta = 0.1 \times 0.1$ for the CP. The system is built using custom designed, fast digital electronics. The ATLAS Level-1 Calorimeter Trigger processors use field-programmable gate arrays (FPGAs) as their main technology, which offer both the required performance and high flexibility. The JEP covers the complete ATLAS calorimetry in the range of $|\eta| < 4.9$ If the CTP accepts the event, the JEP and CP processors provide information on the location and presumed type of the clusters. These areas in the calorimeter (Regions of Interest - RoI) are examined using fine granularity and inner detector data by the Level-2 trigger.

## II. The Jet/Energy Processor

The JEP uses highly parallel data processing. The JEP must handle a large number of input signals and provide very fast logic. To minimise complexity of the inter-module fanin-fanout required for sliding-window algorithms, the JEP has four sections. Each processes calorimeter signals from one quadrant in azimuth, and uses 8 JEMs. The JEP consists of 32 JEMs, where each covers a region of the $\Delta\phi \times \Delta\eta$, illustrated in Fig. 1. In order to achieve non-ambiguous results in the cluster-finding jet algorithm, each module also needs data surrounding

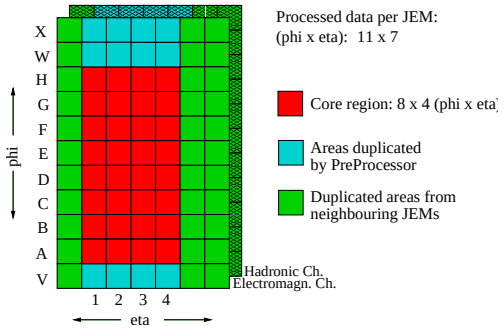


Figure 1: Channel map of a JEM: total range of input channels: $\Delta\phi \times \Delta\eta = 11 \times 7$, of which $\Delta\phi \times \Delta\eta = 8 \times 4$ are the core region.

its core region. The JEM processes event information from the PreProcessor (PPr) system and transmits the energy summation and jet algorithm results to Common Merger Modules (CMM), as well as information about accepted events via Read-Out Drivers (RODs) to the Data Acquisition (DAQ) system. TTC (Timing, Trigger and Control [8]) and DCS (Detector Control System) signals are provided by a Timing Control Module (TCM), and configuration and control are carried out via a reduced VMEbus.

## A. *Architecture of the Jet/Energy Module prototype*

The architecture of a JEM is shown in Fig. 2. The electromagnetic and hadronic components of energy depositions are received from the PPr system on 88 channels of LVDS links at 400 MB/s, which are converted into parallel words of 10-bit width at 40 MHz by *Link Deserialisers*. The first stage of data processing is handled by 11 *Input FPGAs*, which receive the data words and sum the associated electromagnetic and hadronic data up to jet elements. The FPGAs also control the link status and the deserialisers. The jet element data is then multiplexed and sent both to the next stage of processing on the same JEM, and onto the backplane as 5-bit words at 80 MB/s. The device carrying out the algorithms of energy summation and jet location and classification is the *MainProcessor FPGA*. Each JEM houses one MainProcessor FPGA, a common Xilinx device. The areas of data in $\Delta\phi \times \Delta\eta$ which are processed by the algorithms are illustrated in Fig. 1. The duplicated channels in $\eta$ and $\phi$, necessary to achieve non-ambiguous results for the jet algorithm, are provided either by duplication in the PPr system [2], or by transmisssion of jet elements from the two neighbouring JEMs inside the JEP crate through the custom Processor Backplane [2]. Further devices, common Xilinx Spartan-II and CPLD, on the JEM are needed to configure, initialise and control the algorithms. All required algorithms of the JEM are developed, simulated and implemented using the hardware description language VHDL.

One of them is the *Control-FPGA* which provides the interface of the module to a reduced VMEbus on the backplane and also handles data from the *TTCrx* chip mounted onto

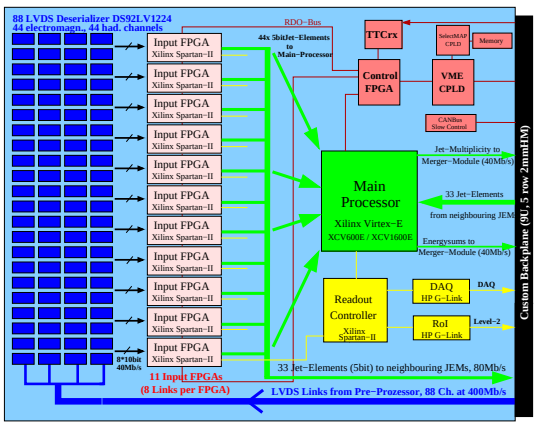


Figure 2: Schematic architecture of a JEM, prototype version 0.1/0.2. One module uses a XCV600E/XCV1600E device as MainProcessor.

the module to receive the system clock and control signals via the TTC network. The *VME-CPLD* allows for in-situ configuration of the FPGAs via VME. On receiving a L1Accept another FPGA, the *Readout Controller* (ROC), collects and sends out all input data, Sum-$E_T$, Sum-$E_x$, Sum-$E_y$ and jet multiplicities, called slice data, onto a connection to the DAQ system using an Agilent G-Link transmitter chip [6]. It also sends the Region of Interest (RoI) data provided by the jet algorithm to Level-2 in the same way.

## B. *Implementation of algorithms*

Each JEM receives electromagnetic and hadronic energies for each jet element via electrical high-speed serial links (LVDS) from the PPr system [5]. Within the InputFPGAs, a synchronisation stage is implemented at the receiving end, which is auto-calibrating on a switching pattern through the LVDS inputs. Parity checks are executed to detect transmission problems, and a mask register allows switching off selected channels. The electromagnetic and hadronic channels are added up to jet elements, multiplexed to 5-bit data at 80 MHz and sent out to the main processing stage. The main parts of both the energy and jet algorithms are implemented in the MainProcessor.

The jet algorithm processes the data at 80 MHz. Jet elements are summed over windows of 2x2, 3x3 and 4x4, allowing a programmable choice of jet window size. The 2x2 windows of the central 4x8 region are compared with their nearest neighbours to identify RoI jet candidates that are a local maximum. If so, the associated jet window is compared with 8 programmable energy thresholds. Finally, 3-bit multiplicities of jet clusters are produced corresponding to the 8 jet definitions. In parallel the energy algorithm processes the demultiplexed 10-bit wide jet elements of the core region at a rate of 40 MHz. To calculate the total transverse energies, all 32 jet elements are summed to form $E_T$ and the components $E_x$ and $E_y$ needed to from missing energy. The energy sums are compressed using a quad-linear encoding to a 25-bit odd-parity-protected data word. The results, which are the RoIs, jet multiplicities, and the energy sums, are sent via the backplane for detector-wide summation in CMMs [2]. Lookup tables are used to determine $E_{T,miss}$ from the $E_x$ and $E_y$ components.

Additional memories are implemented for the purpose of stand-alone diagnostic tests of the data path. The play-back memories which are implemented in front of the data path within the InputFPGAs can be filled with test patterns. Upon receipt of a broadcast command by the TTC, the playback memories start to insert the test data into the processing chain. The energy and jet results of the test patterns are captured in spy memories further down the chain. Both types of diagnostic memories are accessible via VME. Data from accepted events are used for subsequent data analysis and validation. Therefore the slice data are stored in pipelines on each InputFPGA and on the MainProcessor to await a Level-1 accept decision. On receiving a L1Accept signal the ROC will initiate and control the transfer of up to 5 slice packages along with the corresponding bunch crossing number to the DAQ system via

RODs, and of the transfer of the ROIs to the level-2 trigger. For stand-alone diagnostic tests of the DAQ read-out functionality, additional spy memories are implemented on the ROC-FPGA.

## III. Standalone tests of Jet/Energy Module

Systematic tests have been performed on the JEM prototypes in order to assure correct and reliable operation of the JEM within the trigger environment. As a first step, the modules are operated stand-alone with the system clock provided by the onboard crystal oscillator, not by a TTC system. The playback memories of 256 words depth within the InputFPGAs are filled with various data patterns. A playback/spy cycle is initiated via a VME signal and the results from the spy memories are read back and compared offline by the in-crate CPU with the results of a closely modelled simulation program for the energy summation. Simple test programs have been used, allowing fast throughput of data, but not interfacing the Level-1 trigger software environment.

### A. Test patterns

Two options of test patterns are available for JEM prototypes. The physics patterns, in this case the $t\bar{t} \rightarrow WW^{(*)} \rightarrow 4$ Jets channel, were produced by the event generator PYTHIA and fed into the detector and trigger simulation ATLFAST and ATL1CT [7] (Fortran Version). 2.5 million events have been produced and stored for use in tests. Data for the core regions of a JEM were written out by the trigger simulation. Since the deposition per event is very low, the kinematic cuts on the production level of PYTHIA have been set very high, in order to increase the rate of high-energy jets within the data sample for the JEM: Mass: 700-2000 GeV, transverse momentum $p_T > 500$ GeV, and more then 64 GeV of $E_T$ deposition. This set of test patterns requires all 64 channels of the core region to be filled with data, which can always be achieved using the onboard playback memories, but they are not usable if only a small set of real input LVDS channels is available.

Random patterns are also produced which cover the whole range of input data up to 9 bits (511 GeV) and are sensible for those tests with a limited number of input channels of the JEM's. In order to increase the rate of highly energetic channels, but at the same time to avoid saturation, the channels are filled using random numbers between 0 and 1 folded with a sloping exponential function ranging from 0 to 511. These random patterns have also been used with the full number of channels.

### B. Test using Playback and Spy memories only

Two JEM prototypes have been tested using the test vector patterns described above. A test was performed using the $t\bar{t}$-event library, processing the library 24 times, with a total of 60 million events. The results for the energy summation algorithm for Sum-$E_X$, Sum-$E_Y$ and Sum-$E_T$ were identical to the expected values from the offline simulation. Another test used random patterns. A total of 6 million events was processed, also showing the expected results for the energy sums.

### C. Test using 16 channels serial LVDS input data from DSS and Spy memories

The test was then extended using a Data Source/Sink module fitted with two LVDS Source daughter modules, which provide a total of 16 serial LVDS channels, being able to serve two neighbouring InputFPGAs with data as expected from the PPr system. Due to the limited number of channels, the random patterns described above have been used in this test. For this test, the data buffers in the DSS are filled repetitively with the random test vectors. The DSS is set to send a constant stream of data. A VME signal enables the spy memory inside the JEM's MainProcessor to be filled. The data is then read back from this memory, matched with the repetitive stream and compared with the expected results. This setup processed 1.8 million events and all values received for the energy sums were as expected. The test has been repeated using all four possible pairs for InputFPGAs in the core region.

### D. Loopback test of duplicated channels

In order to test the connectivity of the backplane, a loopback device has been designed, feeding the outputs of jet element data from the InputFPGAs intended to go to the neighbouring JEM back into the MainProcessor of the same JEM. The energy summation algorithm is changed to accept the duplicated channels instead of the core region. A test pattern of a binary counter from 0 to 511 GeV being filled into just one input channel is used to check the correct reception of the data, which has been found to work properly.

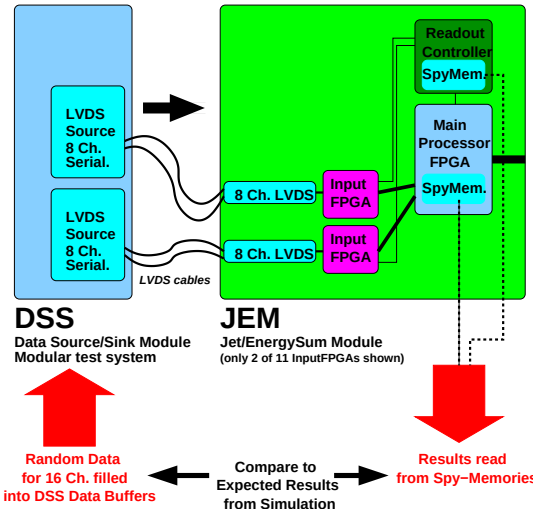


Figure 3: Standalone test of JEM with LVDS data feed at Mainz

## IV. Tests of Jet/Energy Module with LVDS data feed, within ATLAS software environment controlled by TTC

The test setup for the JEM prototype was then extended with a TTC system for system clocking and command distribution. A daughter module housing a TTCrx chip is mounted on the JEM prototype. A TTC system consisting of a TTCvi and a TTCvx module is connected to the JEM via the electrical output and to the DSS via the optical output. Whereas the tests described in the previous paragraph have been controlled by simple test scripts and programs based on the VME driver routines, all further tests have been carried out using routines in C++ within the Level-1 Calorimeter Trigger Software environment.

The Linux installation of Red Hat 7.3 of the VME Single-Board Computer includes the ATLAS `DAQ-1` software package and the CERN VME driver. The Level-1 Calorimeter Trigger Software `l1calo` is installed, which includes all necessary routines to initialise, configure and control the hardware as well as the simulation. The routines dealing with the hardware directly, the `ModuleServices`, are developed in the responsible groups as well as the simulation `ModuleSim`, which are being developed for each module, very closely modelling the functionality of the modules. The simulation is run in parallel in an identical setup as the hardware. This setup is described by database files using `XML`, which include all information about module types, crate location of modules, cables and connections. The test setup is controlled by the `RunControl`. The firmware of the InputFPGAs is supplemented with an input sychronisation stage, which ensures a reliable data transfer at the input stage of the JEM by adjusting the clock phase of the internal DLLs of the Xilinx Spartan-II FPGA [3] in order to compensate for delays between the input channels caused by cables and onboard tracks and routing. One of the four available clock phases of the DLLs is automatically selected when a special synchronisation pattern is fed to the InputFPGAs.

The tests described in the previous chapter have been repeated with this setup, using both the random and the physics test patterns. System commands for Playback/Spy cycles are broadcast using the TTC system. The results read back from the Spy-Memories of the MainProcessor have again been found to be identical to the expected values from the simulation.

The readout functionality of the module was tested in a stand-alone setup using a Spy-Memory within the ROC that captures all readout data streams from the Input and MainProcessor FPGAs. The data has been found to match the expected data packets. Further tests using the complete readout chain are described in the following paragraph.

Using the two available JEM prototypes mounted into the custom backplane within the 9U crate, a latency measurement has been done. The deskew-2 setting of the TTC is used for this scan. The latency of the JEM algorithm has been found to be 8 bunch crossings (25 ns each). A picture from the oscilloscope

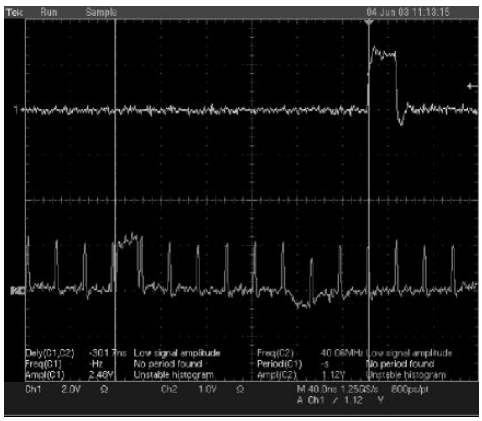

Figure 4: Latency measurement of the Real Time Data Path of the JEM prototype (energy summation only)

illustrating the latency is shown in Fig. 4.

### A. *Trigger prototype module integration: Readout of the JEM*

All interfaces of the JEM to the outside world within the experiment environment are being tested in an integration test. The setup is illustrated in Fig. 5. Input data as expected from the PreProcessor is fed into the JEM using a DSS module with 16 channels of serial LVDS source. The results of the JEM are transmitted via the custom backplane to the Common Merger Module [2]. The readout data of both the JEM and the CMM is via G-Link cables connected to a prototype Readout Driver (ROD [2]), which converts the readout data packets to S-Link and transmits them. The data sent through the S-Links is received by a DSS equiped with an S-Link sink module. Using this setup, incoming data and results at all interface stages of the system can be checked both by comparing the readout data and also by using the spy memories inside the modules. In order to assure a consistent set of data from the various stages, the readout signal (L1A) is provided by the TTC system, which is also used to provide all system clocks.

The system has also been tested for the whole number of input channels using the playback memories of the JEM's InputFPGAs. The expected S-Link output data is generated by the simulation chain. Both sources of input data - either the DSS's data buffers or the InputFPGA playback memories - are filled using the very same data patterns as the online trigger module simulation, allowing for an automated comparison of the readout streams.

## V. Development of final Jet/Energy Module for ATLAS: JEM-1

The next generation of the JEM, Module-1, planned to be the module to be used in the final ATLAS Level-1 Calorimeter trigger, is being designed taking into account the experience from the tests of the prototype modules and the development in technology. A schematic overview of this module is given in Fig. 6. LVDS deserialiser devices of the SCAN series are

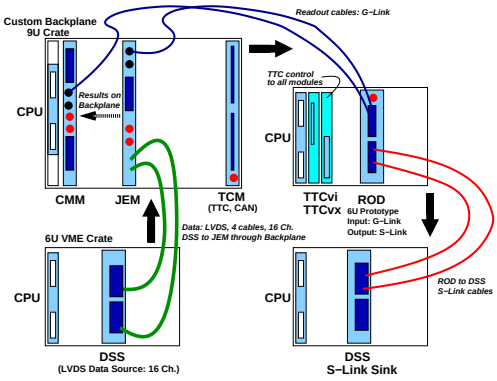


Figure 5: Readout of Jet/Energy Module with DSS as LVDS data feed, Readout Driver (ROD) and DSS for S-Link data sink

used, which will allow for JTAG/Boundary Scan testing of the onboard connections. Each of these devices deserialises 6 data channels. A new generation of FPGAs, the Virtex-II series, will be used on JEM-1. They offer higher logic densities and improved performance. Since fine-pitch BGA packages are usually fitted to smaller PCB's in the current commercial market, it has been decided to fit one InputFPGA and four LVDS deserialisers on daughter modules. A JEM-1 will be fitted with four of those daughter modules. The use of daughter modules also simplifies the rework of faulty modules significantly, as they can be easily replaced. The readout and control functions will also be on a daughter module, leaving basically only the MainProcessor mounted on the mainboard of JEM-1.

The firmware has been adapted to match the new devices and mapping. Since all interfaces to the outside world are identical, Module-1 can replace the current prototype in the module integration tests. The daughter modules and the main board are under production and will be subjected to standalone tests and module integration tests in 2004.

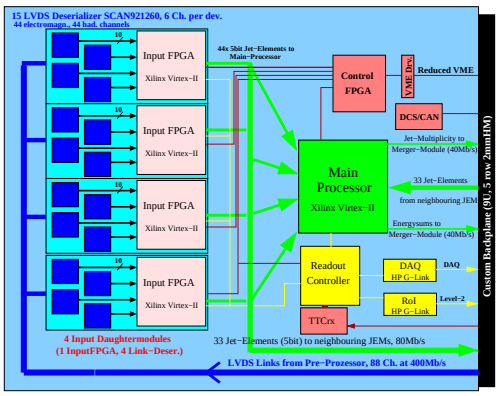


Figure 6: The final Jet/Energy Module for ATLAS: JEM-1

## VI. Conclusion

Two fully functional JEM prototypes have been designed, produced and tested in a stand-alone test set-up using test vectors for the energy sum algorithm. Test vectors were generated by the trigger simulation, which provides both input data for the JEM and the expected energy summation results.

The stand-alone test of JEM used the playback memories or a DSS whose source buffers are filled with test patterns and the spy memories. The DSS provides the JEM with a continuous data stream via the serial LVDS links. The results received from the spy memories were compared to the expected values from the trigger simulation. Several millions events have been processed using both the internal memories and the DSS data source, with all energy summation results read back from the JEM being identical to the expected values.

The data communication between the neighbouring JEMs via the custom processor backplane has been tested, which is essential for the sliding window jet algorithm.

The readout facilities at board-level and the data communication to the CMM and ROD have been tested. The two JEMs have been subjected to an integration test in a setup connecting all interfaces simulating the final Level-1 trigger setup controlled by a TTC system. This includes the control software and trigger module simulation environments. Test patterns have been provided using LVDS sources, and both the results store within in-module memories and readout data have been compared to the expected data packets from the simulation.

Based on the results of this programme and recent developments in technology and board manufacturing, the final JEM-1 is being designed. Volume production of the 32 JEMs needed for ATLAS will start in 2004.

## VII. References

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