Production Test Rig for the ATLAS Level-1 Calorimeter Trigger Digital Processors

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Abstract

The Level-1 Calorimeter Trigger is a digital pipelined system, reducing the 40 MHz bunch-crossing rate down to 75 kHz. It consists of a Preprocessor, a Cluster Processor (CP), and a Jet/Energy-sum Processor (JEP). The CP and JEP receive digitised trigger-tower data from the Preprocessor and produce electron/photon, tau, and jet trigger multiplicities, total and missing transverse energies, and Region-of-Interest (RoI) information. Data are read out to the data acquisition (DAQ) system to monitor the trigger by using readout driver modules (ROD). A dedicated backplane has been designed to cope with the demanding requirements of the CP and JEP sub-systems. A number of pre-production boards were manufactured in order to fully populate a crate and test the robustness of the design on a large scale. Dedicated test modules to emulate digitised calorimeter signals have been used. All modules, cables and backplanes on test are final versions for use at the LHC. This test rig represents up to one third of the Level-1 digital processor system. Real-time data between modules were processed and time-slice readout data was transferred to the ROD at a trigger rate up to 100 kHz. Intensive testing consisted of checking the readout data by comparing to hardware simulations of the trigger. Domains of validity of the boards were also measured and dedicated stressful data patterns were used to check the reliability of the system. Test results have been successful and the Level-1 calorimeter trigger system is proceeding to full production.

I. THE ATLAS LEVEL-1 TRIGGER SYSTEM

The ATLAS trigger chain is a three-level system designed to reduce the raw rate of 1 GHz of proton-proton interactions and 40 MHz beam-beam bunch crossing to 200 Hz [1]. The first level, or Level-1, selects interesting events at a rate of 75 kHz within a total latency of 2 μs. It provides Region-of-Interests (RoIs) to the Level-2 to build a decision at a rate of 2 kHz. The third level makes further selection and stores data at the final rate of up to 200 Hz.

The ATLAS Level-1 trigger works on a reduced-granularity data from the calorimeter and muon systems. The calorimeter trigger is based on trigger-towers, covering calorimeter cells of 0.1 x 0.1 in η x ϕ. Potentially interesting events are selected by identifying electron/photon candidates, jets, single-hadron/tau candidates, missing transverse energy, and total transverse energy. Muon candidates are selected with a separate trigger. Information from both of these systems are combined and sent to the Central Trigger Processor where the decision to accept or reject the event is made.

The algorithm of event selection of the ATLAS Level-1 calorimeter trigger system is implemented in hardware, with the use of FPGAs to allow flexibility. All board designs have been tested thoroughly, but before launching the full production, a first set of boards were built in order to test the robustness of the design in a heavily populated environment. An adequate number of pre-production boards were manufactured to fully populate a crate, corresponding to ¼ of the final Level-1 Calorimeter Trigger system. Peripheral modules were built to source data for such a subsystem. The development of such a test rig is a vital tool to check the quality of the boards as they will come from the manufacturer.

This paper will firstly describe the architecture of the ATLAS Level-1 calorimeter trigger system. A detailed description of the production crate test rigs will follow, and test results of the boards in such an environment will be presented.

II. THE ATLAS LEVEL-1 CALORIMETER TRIGGER ARCHITECTURE

The ATLAS Level-1 Calorimeter Trigger system consists of three subsystems, namely the Preprocessor (PP), electron/photon and tau/hadron Cluster Processor (CP), and Jet/Energy-sum Processor (JEP) (Figure 1) [2]. The CP and JEP will receive digitized calorimeter trigger-tower data from the Preprocessor, and send trigger multiplicity information to

the Central Trigger Processor (CTP) via Common Merger Modules (CMM). A full description of the Preprocessor can be found elsewhere in these proceedings. It consists of 124 Preprocessor Modules (PPM), which provide the input data for the CP and JEP systems. Using Readout Driver modules (ROD), the CP and JEP will provide RoIs also for Level-2 (Event Filter), and intermediate and final results to the data acquisition (DAQ) system for monitoring and diagnostic purposes. This paper refers to the two latter subsystems, CP and JEP, as described in more detail in the following section.

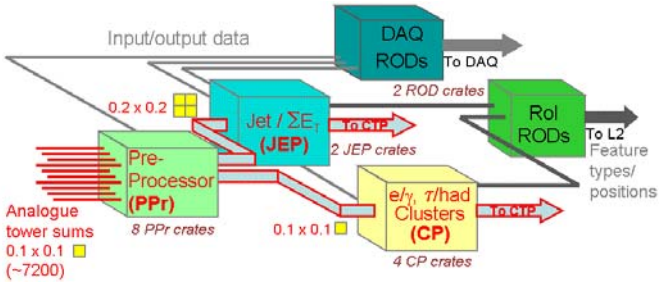

Figure 1 The Level-1 Calorimeter Trigger

III. The Cluster and Jet/Energy Processor

The CP and JEP system work at 40 MHz in real time, and provide readout information on receipt of a Level-1 Accept signal.

A. Real Time Data

The CP system consists of 56 Cluster Processor Modules (CPM) shared between 4 crates. It identifies and counts electron/photon and tau/hadron candidates. The Jet/Energy Sum processor consists of 32 Jet/Energy Modules (JEM) shared between 2 crates. It counts jet candidates and form missing and total transverse energy sums. All final sums of cluster/jet candidates and total and missing energy are merged through 12 CMMs, with a layout of 2 CMMs for each processor crate.

Both systems received their input data from the Preprocessor using LVDS 400 Mbit/s serial 4-links chipset in order to reduce the I/O requirements on cables and pins. The total number of LVDS cables needed is 1888, each 12 m long. In addition to the incoming data, large volumes of data are exchanged between neighbouring modules to accommodate the cluster and jet-finding sliding-window algorithms. A common custom backplane has been designed containing over 15000 pins, through which digital signals are propagated with speeds of up to 400 Mbit/s differential and 160 Mbit/s single-ended. Details of such a challenging backplane, design and production, are available elsewhere in these proceedings.

In total, the CP and JEP process in real time around 550 GBytes/s of data, to reduce them down to ~0.05 GBytes/s sent on to the CTP to build the Level-1 decision.

B. Readout path

On receipt of a Level-1 decision, the CP and JEP send out DAQ and RoI data to 20 Readout Driver modules (ROD). Each ROD can process data from up to 18 input boards using optical links. The design is such that one ROD should read out one processor crate. A maximum data rate of 800 Mbit/s per link is achieved using the Agilent G-link protocol [3]. Data is reformatted into standard ATLAS event fragments, and transmitted on optical links using the ATLAS S-link protocol.

IV. The Production Crate Test Rig

Although boards and backplane have their layout completed and were ready to go to full production [4], their design was initially approved on a scale of a few pre-production boards. The ATLAS Level-1 Calorimeter Trigger is mainly composed of custom made components, down to the backplane, and it was decided to test the robustness of the different designs in a fully-populated crate environment. A set of additional boards were produced corresponding to a ¼ of the final CP and JEP system.

To avoid the need for a large number of Preprocessor Modules, emulator boards have been designed to deliver the equivalent LVDS calorimeter data needed. These so-called LVDS Source Modules (LSM) have a topology such that each individual board matches a digital board of the CP or JEP system. The final ATLAS LVDS cables were used to connect the LSMs to the modules under test. A total number of 300 cables have to be routed from the LSMs to the backplane. A picture of the setup in the laboratory is shown in figure 2. Table 1 lists the different hardware components used to build such a test system. The crate was equipped with a CPU mounted on an adaptor board to match the custom backplane crate, and a custom board, the Timing and Control Module (TCM), to broadcast the clock to each individual module. The TCM also provides an external CANbus to interface with the DCS system of ATLAS.

Components	Number
LSMs	16
CPMs	14
JEMs	7
TTCrx	30
OPTICAL CABLES	18
LVDS CABLES	308

Table 1 List of Components for the production crate test rig

Since the beginning, all tests of prototypes and pre-production modules used the ATLAS online software. It was easily expandable to such a large scale by just adding the new components in the database files. A simulation program down to the bit level was successfully run to validate the data processed by the hardware.

Figure 2 308 LVDS cables installed at the back of the crate.

V. TEST RESULTS

A. *Cluster Processor Modules*

A total number of 14 CPMs were tested in the crate (figure 3). Stress patterns of alternating words were send to check the stability of the LVDS. Parity correct data were processed, and no parity errors were observed on input or across the backplane after 5 hours of running.

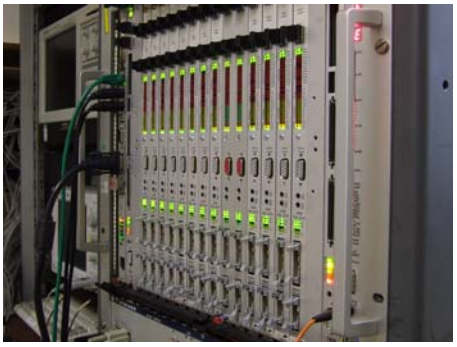

Figure 3 A crate with 14 CPMs

Figure 4 shows the parity-error-free timing window measured on one board, for 8 of the most demanding FPGA chips processing single-ended 160 Mbit/s signals. A window of around 2 ns has been measured, similar to what was measured with just a few boards in the crate.

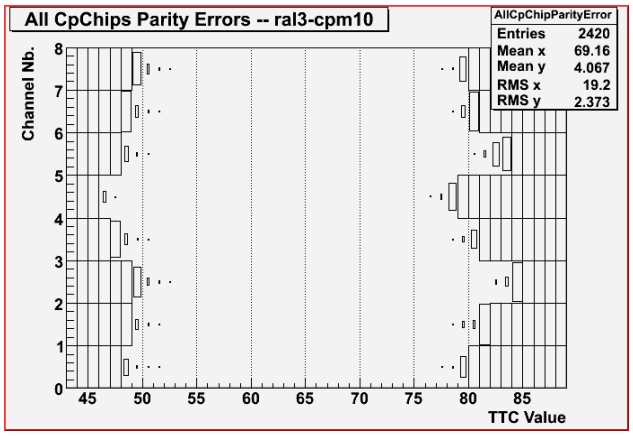

Figure 4 Parity error free timing window for 8 FPGA chips on the CPMs. Empty cells represent timing values with no errors.

A power consumption of 1 kW per crate has been measured, but this value is data patterns dependent. Dedicated test patterns with a programmable ATLAS occupancy rate have been sent into the system to explore its limits. Figure 5 shows that for a 10 % ATLAS occupancy rate, the total current drawn in the crate is around 200 A at 5V. Higher occupancy has also been used and the total current stays well below the maximum current supply of 300 A. During a run, individual sensors from the on-board FPGAs have been read out, with temperatures around 45 ^{o}C for the biggest parts. The values of their currents were within specification.

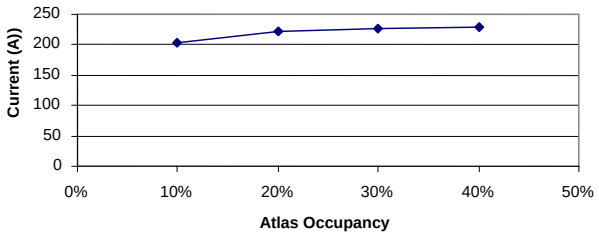

Figure 5 Current consumption as a function of the ATLAS occupancy rate

B. *Jet Energy Module*

Seven Jet Energy processor boards have been used to populate a crate, completed with a set of 8 CPMs. A full crate of JEMS would have already been half of the final JEP system, so such a mixed configuration was a good compromise to test the JEM design within a noisy environment.

Similar tests as with the CPM were performed, and the stability of the LVDS links was checked over several hours of run. Unlike the CPMs, JEM data are not parity protected, and dedicated firmware was produced to test the stability of the data across the backplane. After a 5-hour run, no data errors were detected across the backplane.

C. *Common Merger Module*

The crate was equipped with two common merger modules. Hit information, energies and jet counts are send through the backplane, and gathered by the CMMs before being sent to the CTP. Data are parity protected, and no parity errors were detected after a 5-hour run on backplane inputs. A timing investigation of the data was performed using 14 CPMs as a source of data, and a parity error free window of 10 ns was recorded as shown in figure 6.

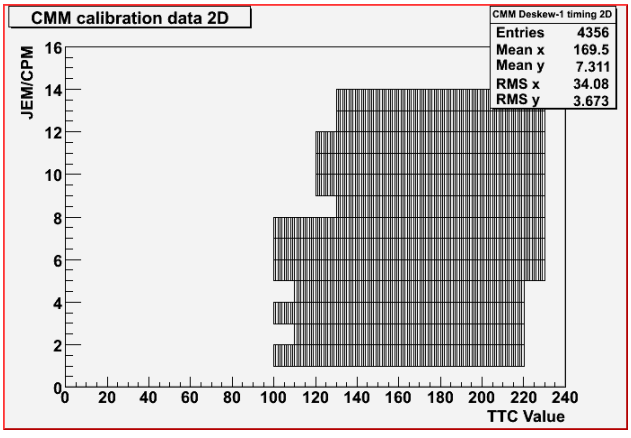

Figure 6 TTC scan of 14 CPMs on the CMM input

D. *Readout Driver*

The availability of several optical G-link transmitters from the boards in the crate was a good test bench for exercising the multitude of inputs of the ROD. A total of 16 G-links (due to a hardware problem, the 2 bottom links were not available) were therefore connected to the ROD, and no parity errors or

link failures were observed after a 1-hour run with a Level-1 Accept rate around 80 kHz. Event fragments from 5 CPMs were also compared to simulation, and a total of 200K events were successfully processed

E. DCS

The external CANbus was connected to a DCS standard Kvaser card [5]. The ATLAS Level-1 Calorimeter Trigger does not use the ELMB [6] but it still has to provide the slow control information using the CANOpen protocol [7]. Firmware was successfully written and tested, and values of voltages, currents and temperatures of 13 boards were correctly read out using the CANOpen format. Preliminary S/W using the PVSS environment was running, and figure 7 shows an example of the temperature map along the crate. Each column represents one board, and each square represent the colour-code temperature of the 8 biggest FPGA chips per CPM. One board was not loaded with the microcontroller F/W, and its equivalent dark column corresponds to no data available. In addition, alarm controls were also implemented and tested by decreasing the thresholds of warning (such as current level). It was checked that the crate was switched off accordingly. Such a feature is vital when testing a board for a long run without requiring the presence of an operator nearby.

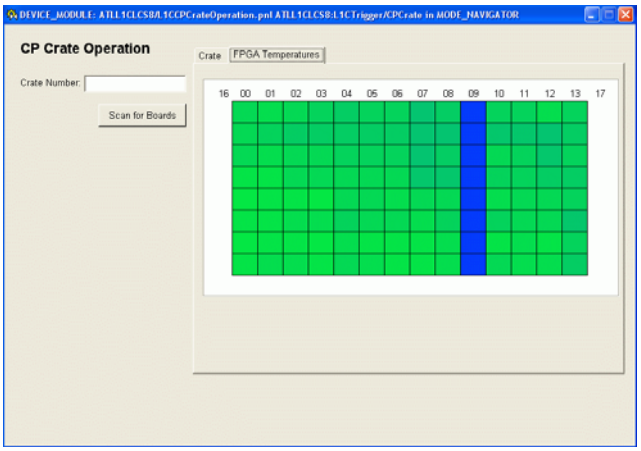

Figure 7 An example of the temperature profile across the crate for 14 CPMs

VI. CONCLUSION

The crate test has been successful in validating the final design of the digital modules of the ATLAS Level-1 Calorimeter Trigger Processor. Problems met and not reported in this note, were corrected in the comfort of the laboratory rather than in the ATLAS pit. Power consumption of the crate has shown that the system is not running on the edge, and currents and temperature measurements show that the components are well inside their specifications.

Boards are now in full production, and will be installed progressively at CERN as they complete manufacture and test.

VII. REFERENCES

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[6] http://elmb.web.cern.ch

[7] Can in Automation (CiA) international users' and manufacturers' group, http://www.can-cia.org