The ATLAS Level-1 Calorimeter Trigger is designed to identify high-p_T jets, electrons/photons and hadrons and measure total and missing transverse energy in proton-proton collisions at the Large Hadron Collider (LHC). Two subsystems – the Jet/Energy-sum Processor (JEP) and the Cluster Processor (CP) – process data from every crossing, and report feature multiplicities and energy sums to the ATLAS Central Trigger Processor (CTP) where the Level-1 Accept (L1A) decision is made. Locations and types of identified features are held in readout pipelines to be sent to the Level-2 Trigger as so-called regions-of-interest (RoIs). Real-time data to the CTP are sent synchronously at 40 MHz over copper cable, while asynchronous readout to the Level-2 Trigger and the data acquisition system (DAQ) is done over gigabit optical links.

The JEP and CP subsystems use FPGAs for algorithm processing, data distribution, readout and control. While developed at separate institutions, they share a great deal of common infrastructure, including a custom, high-density backplane, common modules for VME configuration and monitoring, timing and detector control, and data merging and readout hardware that use FPGAs with different firmware configurations for different tasks. This approach saved substantial development effort and provided a uniform model for software development.

The algorithm-processing modules in the JEP and CP subsystems, however, have significantly different designs, and used different approaches to use multiple, large BGA devices on 9U many-layer printed circuit boards, with different implications for manufacture, assembly, and upgrades.

We present an in-depth description of the two subsystems as manufactured and installed. We compare and contrast the JEP and CP systems, and discuss experiences during production, installation and commissioning. We also briefly present results of recent tests that suggest an interesting upgrade path for higher luminosity running at LHC.