ATLAS Level-1 Calorimeter Trigger
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VME-- Specification

Version 1.2

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Summary

The calorimeter trigger processor requires a large number of signals passing over a purpose-built backplane between processing modules. Insufficient backplane pins and connector height are available for standard VME connectors or event for the full number of pins. This note specifies the reduced VME ("VME--") as used for the backplane and modules concerned, and documents the assigned VME-- addresses for modules.

1 Introduction

The level-1 calorimeter trigger uses a common 9U crate and backplane for the Jet/Energy Processor (JEP) and Cluster Processor (CP) trigger subsystems. The purpose-built backplane includes a section containing the VME-- bus described in this document, as well as high speed point-to-point links between the trigger-processing modules. Each processing crate contains a single board computer (SBC) in slot 1, a Clock Alignment Module (CAM)in slot 2, and Common Merger Modules (CMMs) in slots 3 and 20. In the JEP, 16 Jet/Energy Modules (JEMs) occupy slots 4 to 19, while in the CP slots 3 and 19 are empty and 14 Cluster Processing Modules (CPMs) use slots 5 to 18. In all crates, a Timing Control Module (TCM) is placed in slot 21. This module has the important ancillary function of providing a VME-- bus monitor with LEDs. The CAM can be removed without compromising the digital processing chain if additional space is needed in the crate.

A very large number of signals passed over the backplane between the processor modules, and even using the densest available connector scheme, not enough pins are available for full VME. VME-- needs 49 pins compared with 192 for 3-row VME and 320 for 5-row VME.

The VME-- bus is presented on a 5-row 2mm connector. A 9U module with a 6U aperture adapts slot 1 for use by a commercial SBC. The signal levels and backplane track impedance are identical to those used with full specification VME. The bus is terminated immediately behind the SBC (on the adapter card), so that tracks on the adapter cad effectively form part of the bus.

In this document, the term VME-- is used to refer to the reduced-specification bus, and the term "VME" refers to the standard VME64 bus. VME-- signal specifications are identical to those with the full function and specifications defined by the VMEbus standard [1] except where stated.

The following sections of this document list the restrictions to be observed when using the VME-- bus, the signal pins present and absent in the backplane, and the assigned Crate VME addresses.

2 VME-- Restrictions

2.1 Cycle Types

The crate computer must use A24 D16 cycles to address modules. D8 , D32 and D64 are not supported, nor are A16, A32, A40 or A64. Block Transfers are not supported, although conventional DMA may be used with A24 D16 cycles. The VME Address Modifier (AM) codes are not available, and modules must respond as if AM0-AM5=39 and IACK*=1 were asserted (standard non-privileged A24 data access). Without the AM codes, a module will respond to the address phase of any VME cycle whose low 24 address bits match the module address range. The crate computer must ensure the slaves are addressed appropriately by issuing only A24 D16 AM=39 VME cycles.

2.2 Crate Mastership

A single crate master position is provided in the crate at slot 1. Other modules cannot become bus masters, and there is no provision for handling interrupts or bus mastership requests generated by slave modules.

2.3 Bus Errors

The BERR signal is not present on the crate backplane. This implies that slave modules cannot assert bus error. However, the bus watchdog timer within the SBC VME interface will detect a bus timeout and generate a bus error if a VME cycle fails to complete within the time required. This should be reported through system software as an error.

By convention, trigger processing modules always respond to VME operations within their address range, and error conditions are indicated by error bits in a status register. Software should check for error conditions at appropriate times.

2.4 Geographical Addressing

A24 addressing restricts the address space available to modules. Sixteen JEMs (or 14 CPMs) with identical address windows must have addressing windows no greater than 512Kbytes wide to leave addresses free for other modules.

An extended Geographical addressing scheme determines VME (and also TTC and CAN) addresses throughout the calorimeter trigger system. This relies on the use of non-overlapping VME address allocation ranges for different module types. Each module uses the backplane to determine which address window it should use within the allocated range for its module type. The backplane distinguishes the 16 JEMs (or 14 CPMs) and the two CMMs from one another, using four geographical addressing pins in the JEM/CPM slots and one in each CMM slot.

Modules in the same slot number but different crates must have different TTC and CAN addresses. Three additional geographical addressing pins define the crate numbers, and these are present at every module position.

Address allocation for the different modules are included in section 4.

2.5 Termination and Grounding

The standard 6U VME computer used in slot 1 is housed on an adapter board with the dual functions of providing support within the 9U crate and of connecting the VME and VME-- signals. The adapter board provides termination both for the unused signals and for the VME-- backplane.

Several ground pins are available to modules, and separate VME-- ground pins are not provided.

3 VME- Pin Details

The following signals are defined in the VITA VMEbus handbook, fourth edition [1].

3.1 VME signals present at trigger modules

The following signals are present at all modules. A total of 49 signal pins are required.

Signal mnemonic	Name	Use in LVL1 Processor crates	Pins
A01-A23	Address bus	Needed for A24 addressing	23
DS*	Data strobes	Use single data strobe - see 3.1.1	1
D00-D15	Data bus	Needed for D16 Cycles	16
DTACK*	Data acknowledge	Needed for data transfer	1
WRITE*	Write	Needed for data transfer	1
SYSRESET*	System reset	Separate from CPU reset - see 3.1.2	1
GA0-5	Geographical Address	Needed for geographical address	6

3.1.1 Data and address strobes

In standard VME, data strobes DS0* and DS1* are used to qualify data and also (with A01, A02 and LWORD*) to determine the number of bytes and byte routing within a data transfer (see [1], page 70). However, the data size for VME-- is always D16, so DS0* and DS1* operate identically, and only one of the two is needed. VME rules also allow a slave module to qualify both address and data with the data strobes. AS* may therefore also be omitted, and only a single strobe, named DS*, is provided on the trigger backplane. DS* is obtained by ORing the DS0* and DS1* signals from the SBC on the SBC adapter module.

3.1.2 SYSRESET

The VME64 SYSRST line provides a mechanism to force all modules in a crate to a known state. Asserting SYSRST at the crate SBC may cause it to reboot, and rebooting an SBC may cause it to assert SYSRST. As the crate CPU is expected to be less stable than the trigger processor modules, the SBC Adapter Link Card separates the SBC and crate SYSRST lines.

The adapter link card provides three configurable reset mechanisms:

- A reset push button. A switch connects this to the backplane SYSRST line, the SBC SYSRST line, or a separate RESET input to the SBC (specific to the Concurrent CPU). Any mix of these connections is possible.
- A Processor reset Lemo socket, which can be configured to reset the SBC via its SYSRST or RESET inputs.
- A Backplane Reset Lemo socket, which asserts backplane SYSRST.

3.2 VME Signals Absent from trigger modules

3.2.1 Data Transfer Signals

None of the following signals are used in A24 D16 cycles:

Signal mnemonic	Name	Use in LVL1 Processor crates
A24-A31	Address bus	Not used for A16 or A24.
AM0-AM5	Address modifiers	Not used. See Notes.
LWORD*	Longword	Not used for D16 cycles
D16-D31	Data bus	Not used for D16 Cycles
AS*	Address strobe	Use Data strobes - see 3.1.1
BERR*	Bus error	Only at CPU slot - see 2.3

3.2.2 Arbitration Signals

These signals are terminated on the SBC adapter board and not bussed.

Signal mnemonic	Name	Use in LVL1 Processor crates
BR0*-BR3*	Bus request	Only at SBC Connector
BG0IN*-BG3IN	Bus grant In	Only at SBC Connector
BG0OUT*-BG3OUT*	Bus grant out	Only at SBC Connector
BBSY*	Bus busy	Only at SBC Connector
BCLR*	Bus clear	Only at SBC Connector

3.2.3 Priority Interrupt Signals

Signal mnemonic	Name	Use in LVL1 Processor crates
IRQ1*-IRQ7*	Interrupt request	Only at SBC Connector
IACK*	Interrupt acknowledge	Only at SBC Connector. See notes
IACKIN*-IACKOUT*	Interrupt daisy-chain	Only at SBC Connector

All these signals are terminated on the SBC adapter board and not bussed. IACK* is connected to IACKIN* at the SBC slot on the adapter, as required by the VME standard. This allows a slot-1 processor to raise and service its own interrupt.

3.2.4 Utility and Serial bus signals

Signal mnemonic	Name	Use in LVL1 Processor crates
SYSCLK*	System clock	Only at SBC Connector
SYSFAIL	System fail	Only at SBC Connector
ACFAIL*	Power fail	Only at SBC Connector
SERCLK	Serial clock	Only at SBC Connector
SERDAT*	Serial data	Only at SBC Connector

All these signals are terminated on the SBC adapter board and not bussed.

4 VME addresses

Modules are numbered to match their geographical address in each crate. The 16 JEMS are numbered 0-15, the 14 CPMs are numbered 1-14, and the 2 CMMs are numbered 0 and 1.

Module addresses start at clean address boundaries. Equally numbered JEMs and CPMs start at the same VME-- address. As they can never occupy the same physical slot even if they are put in the same crate, this will not lead to an address conflict.

The addressing scheme divides the 24 bit (16 Megabyte) VME-- address space into two, and allocates the upper half (0x00800000 - 00FFFFFE) to JEMs and CMMs. This gives each JEM or CMM the maximum possible address space in our system of 80000x bytes (512K bytes). The CMMs are placed just below this (they need only 40000x bytes but are allocated 80000x bytes for simplicity) at 700000x and 780000x, and the TCM at 680000x.

Addresses from 0 to 5FFFFEx are not used (address 0 is vulnerable to attack by undefined address bugs in the software), but are available for any module in the reserved slot 2 in the processor crates. As an example, the Concurrent SBC mapping to VME has sufficient flexibility to map shared areas of memory into this region to allow two single-board computers to communicate.

The VME-- base address ranges are assigned as in the following table:

Crate Slot Number	Module		VME-- address
1	Single-Board Computer		
2	*CAM (or Spare)*		0x00600000-67FFFE
3	CMM 0		0x00700000-77FFFE
4	JEM 0	*Unused*	0x00800000-87FFFE
5	JEM 1	CPM 1	0x00880000-8FFFFE
6	JEM 2	CPM 2	0x00900000-97FFFE
7	JEM 3	CPM 3	0x00980000-9FFFFE
8	JEM 4	CPM 4	0x00A00000-A7FFFE
9	JEM 5	CPM 5	0x00A80000-AFFFFE
10	JEM 6	CPM 6	0x00B00000-B7FFFE
11	JEM 7	CPM 7	0x00B80000-BFFFFE
12	JEM 8	CPM 8	0x00C00000-C7FFFE
13	JEM 9	CPM 9	0x00C80000-CFFFFE
14	JEM 10	CPM 10	0x00D00000-D7FFFE
15	JEM 11	CPM 11	0x00D80000-DFFFFE
16	JEM 12	CPM 12	0x00E00000-E7FFFE
17	JEM 13	CPM 13	0x00E80000-EFFFFE
18	JEM 14	CPM 14	0x00F00000-F7FFFE
19	JEM 15	*Unused*	0x00F80000-FFFFFE
20	CMM 1		0x00780000-7FFFFE
21	TCM		0x00680000-6FFFFE

5 References

[1] Wade D. Peterson, The VMEbus Handbook, pub VMEbus International Trade Association.

6 Update History

6.1 Version 1.0

Initial version

6.2 Version 1.1

Added Clock Alignment Module.

6.3 Version 1.2

Minor Typing corrections