A novel simulation and verification approach in an ASIC design process

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Summary:

Summary of a contribution to the 2000 IEEE Nuclear Science Symposium: A novel simulation and verification approach in an ASIC design process

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Abstract

For the Pre-Processor System of the ATLAS Level-1 Calorimeter Trigger we have built a fast signal-processing and readout ASIC (PPrAsic). The novel ASIC design environment incorporates algorithm development with digital hardware synthesis and verification. The purely digital ASIC was designed in Veriog HDL (hardware description language) and embedded in a system wide analog and digital simulation of implemented algorithms. We present here results of our design experience and first performance tests of the Pre-Processor ASIC.

I. Introduction

The ATLAS experiment at CERN requires a highly selective trigger system with optimal efficiency. The event selection at ATLAS will be achieved by a three level trigger system. The first level trigger (Level-1) is a fast pipelined system for the selection of rare physics processes. It achieves a rate reduction from the 40 MHz LHC bunch crossing rate down to the Level-1 accept rate of 75 kHz (100 kHz upgrade). This is done by searching for trigger objects within a total Level-1 trigger latency of 2.0 μs. The number of presumed analog calorimeter signals (trigger towers) which are used as input to the Level-1 trigger is about 7200.

Regarding the timing constraints and the large number of analog signals, the Level-1 trigger needs a hard-wired front-end to perform fast signal processing on all analog input signals in parallel. This system, which is referred to as Pre-Processor system, provides the input data for the Level-1 trigger algorithms and it performs the readout of data on which the Level-1 trigger has based its decision.

II. Summary

A. The Pre-Processor ASIC

The Pre-Processor ASIC performs signal processing on data from four trigger towers signals. It is completely described in the Hardware Description Language Verilog and it will be manufactured in a 0.6 μm CMOS process offered by Austria Micro Systems (AMS). The following tasks need to be performed by the PPrAsic:

- **Synchronization:** The digitized data needs to be synchronized to the same bunch-crossing, because of different time-of-flight for particles from the interaction point to the calorimeter and the different cable lengths from the calorimeter to the trigger cavern.
- **Bunch-crossing identification (BCID):** This circuit consists of two algorithms to identify the transverse energy deposition represented by a trigger tower signal, and the corresponding bunch-crossing in time. One algorithm is applied to non-saturated signals and one is applied to saturated signals.
- **Energy calibration:** A lookup table is used to fine-calibrate the digitized data to the deposited transverse energy E_T. It maps 10-bit data after BCID to 8-bit.
- **Formation of jet elements:** The Pre-Processor pre-sums four trigger towers to coarser cells (jet elements)
- **Bunch-crossing multiplexing:** This transmission scheme (BC-mux) doubles the effective bandwidth of the output data.
- **Readout:** The data on which the Level-1 Trigger has based its decision are read out for verification.

B. The design environment

The requirements of the ATLAS trigger system, like optimal efficiency and fast processing, makes it necessary to develop application specific algorithms implemented in integrated circuits. Further more, the system complexity requires compact electronics with a high level of integration. In order to handle this complexity, a flexible design environment was developed for the Pre-Processor ASIC. The environment makes use of a CVS[1] repository, which allows many designers to contribute to the hardware description code simultaneously.

The purpose is to provide a platform for a system wide simulation of implemented algorithms and their surrounding electronics. Such a simulation can be used to develop algorithms, to demonstrate their efficiency, and to generate input and expected output test vectors. Test vectors are required for simulation of the hardware description (NC-Verilog) during the design process, and once the ASIC is back from its foundry, test vectors can quickly be adjusted to what is expected in real operation.

The design environment is shown in Figure 1. It consists of three types of simulators: an analog circuit simulator (Pspice [1]) for analog input pulse generation, a heterogeneous simulator for analog and digital algorithm simulation (Ptolemy [2]), and a simulator for the hardware description (NC-Verilog [3]). The communication between simulators are coordinated by Perl scripts, which provide the configuration, set-up, and

[1] CVS: Concurrent Versions System

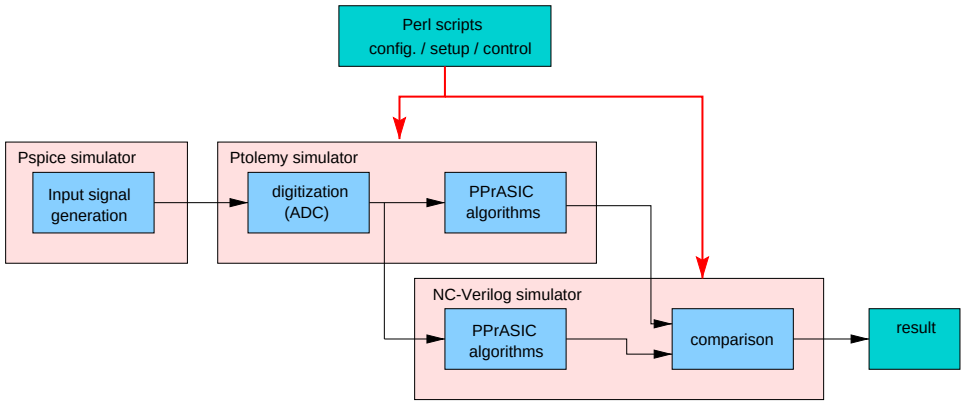

Figure 1: Design environment used for algorithm development, hardware description, and verification of the Pre-Processor ASIC.

test vector data to each simulator. The final simulation results are compared by dedicated Verilog modules.

C. *Results and design experience*

In an ASIC design process verification is usually be done by looking at waveform displays. The designer has to check his code thoroughly by comparison of output vectors with what was originally intended for the algorithms. Here, the Verilog code can be check in addition with the development tool (Ptolemy) directly. This allows to perform a more detailed verification and it has helped to speed up the verification process of the large and complex PPrAsic design.

A 4-channel PPrAsic consists of 34.000 standard cells, 66 kbit RAM, and it has a size of 65.6 mm^2. The design flow of the PPrAsic is illustrated in Figure 2.

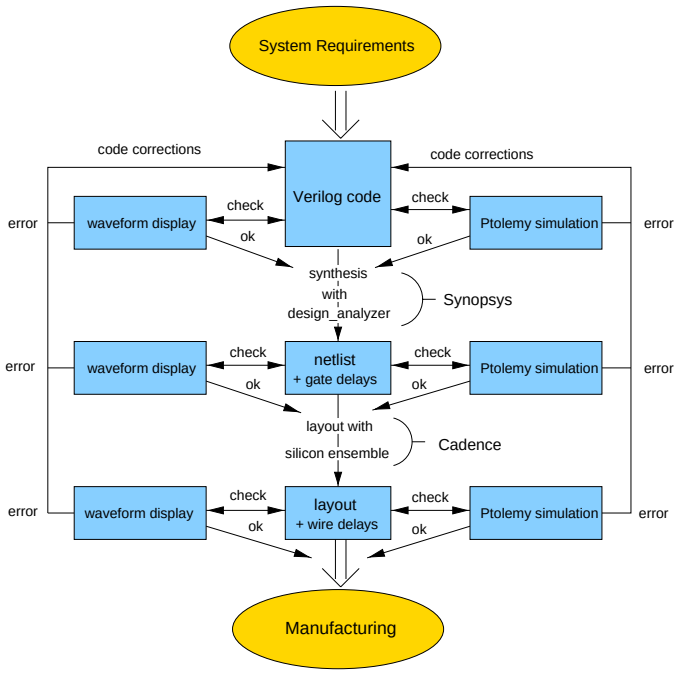

Figure 2: Design flow of the PPrAsic. The verification process is illustrated on each level of the design process, where different timing information are present.

We present here the performance of the PPrAsic, where the described novel design environment has contributed to the ASIC design from the beginning up to the final chip tests.

III. References

[1] Pspice V9 “Mixed A/D circuit simulator,” *Orcad* http://www.orcad.de

[2] Ptolemy 0.7.1 “Heterogeneous Modeling And Design,” *University of California at Berkeley* http://ptolemy.eecs.berkeley.edu

[3] NC-Verilog *Cadence Design Systems Inc.* http://www.cadence.com