Prototype Cluster Processor Module for the ATLAS Level-1 Calorimeter Trigger

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Abstract

The Level-1 Calorimeter Trigger consists of a Preprocessor, a Cluster Processor (CP), and a Jet/Energy-sum Processor (JEP). The CP and JEP receive digitised trigger-tower data from the Preprocessor and produce trigger multiplicity and region-of-interest (RoI) information. The CP Modules (CPM) are designed to find isolated electron/photon and hadron/tau clusters in overlapping windows of trigger towers. Each pipelined CPM processes a total of 280 trigger towers of 8-bit length at a clock speed of 40 MHz. This huge I/O rate is achieved by serialising and multiplexing the input data. Large FPGA devices have been used to retrieve data and perform the cluster-finding algorithm. A full-specification prototype module has been built and tested, and first results will be presented.

Summary

The ATLAS Level-1 Calorimeter Trigger system consists of three subsystems, namely the Preprocessor, electron/photon and tau/hadron Cluster Processor (CP), and Jet/Energy-sum Processor (JEP). The CP and JEP will receive digitised calorimeter trigger-tower data from the Preprocessor, and will provide trigger multiplicity information to the Central Trigger Processor via Common Merger Modules (CMM). Using Readout Driver (ROD) modules, the CP and JEP will also provide region-of-interest (RoI) information for the Level-2 trigger, and intermediate results to the data acquisition (DAQ) system for monitoring and diagnostic purposes.

The CP system has to process 6400 trigger towers. A Cluster Processor Module (CPM) has been designed to process 280 trigger towers. To receive 8-bit parallel data from all of those trigger towers would require 2240 connections. This would be clearly impractical, so the scheme is to transport the data in high speed serial format. In addition, a multiplexing scheme has been implemented to further increase the number of trigger towers per link. This is possible due to the nature of the Bunch Crossing IDentification (BCID) algorithm, which leaves adjacent time-slices empty.

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LVDS deserialisers receive the 400 Mbits/s input streams. In order to process overlapping 4x4 trigger-tower windows, massive fanout of data is required, both on each CPM and to its immediate neighbours. Twenty FPGAs per CPM convert the parallel input data to a 160 Mbit/s single-ended serial format for use on the CPM, and via a custom-built backplane to its neighbours. Eighty-four trigger towers, of both e.m. and hadronic data, must be handled to implement electron/photon and tau/hadron cluster-finding algorithms in a single chip that processes eight overlapping trigger-tower windows. Virtex-E FPGA technology has been chosen to implement the code in this so-called CP chip. The algorithms could be upgraded or rewritten in the future to add trigger capabilities. Each CP chip flags which e.m./tau thresholds, among 16, have been passed by an isolated cluster. Regions of Interest are available as output for the Level-2 trigger. Eight CP chips are necessary to fully process all the trigger towers of one module. Firmware has been written and tested successfully, showing comfortable latency.

Two streams of data are output from the CPM :

- Realtime data: an additional FPGA calculates the multiplicity of each threshold passed by the eight CP chips and results are sent through the backplane to two CMMs, which between them sum the total multiplicity of each of the 16 cluster thresholds over the 14 CPMs in each crate.
- Time Slice Data: from two additional FPGA devices, DAQ and RoI data type are formatted and sent to the ROD modules via G-link.

A full-specification prototype CP module has been implemented on a 9U board and one of them has been manufactured successfully early this year. Intensive tests have been performed with the custom-built backplane. Although tests have been performed with data loaded inside internal memory of some chips, Data Source Sink Modules (DSS) were used to transmit and recover sampled data. Supplementary daughter cards have been designed to populate the DSS to match speed and signal type delivered/received to/from the CPM. A C++ package has been developed in order to simulate data expected inside the board and through the system test. This software tool enables us to verify and debug data during testing.

Similar tests are being done in parallel with other boards of the trigger system. The goal is to realise a full test bench holding 1/14 of the Level-1 Calorimeter Trigger by the end of this year.