Prelude: LHCC referees

- Have only just seen the report of the LHCC referees on their Comprehensive Review in July.
- There were no comments at all about the calorimeter trigger!

ATLAS System Status Overview (ASSO)

- **Run by ATLAS Technical Coordination (TC)**
  - Not a *technical* review
  - First one was for TileCal; this one covered all of T/DAQ (!)
- **Presentations very short, but TC contact (Bill Cleland) worked with speakers in advance**
  - Bill suggested outline of the talks, which were:
    Preprocessor – Paul Hanke; **CP and JEP – Tony Gillman**
  - Some material shown to Bill but not included in talks
- **Does not pass judgement — output is an action list, intended to help the system**
  - We were asked to suggest actions that would be useful to us

Bill Cleland's outline

1. Short description of the deliverable or activity
2. How locally the work is organized to accomplish this
3. Description of the necessary infrastructure
   (labs, tools, manpower, …)
4. Input interfaces: definition, needs, and problems
5. Output interfaces: definition, needs, and problems
6. Internal milestones or schedule (end R&D, start production, 10%, 50%, …)
7. Quality Assurance activities and organisation
8. Results or performance issues

Additional questions

1 List the names of the contacts you have with the systems with which you interface. Are the interactions adequate for your work? If not, can you suggest improvements?

2 Are the specifications and requirements for the hardware for which you are responsible adequately defined?

3 Are there areas within your responsibility where you see significant technical or schedule risk? If so, please list them and state the nature of the problem.

4 Are you aware of any problem not alluded to above concerning the LVL1 system or its interfaces with other ATLAS systems which should be brought to the attention of TC?

Items flagged at video pre-meeting

- **The following items were mentioned, but do not appear again in the ASSO comments and actions:**
  - PRR timing and organisation for PPr ASIC, MCM (and PPM)
    - Do them all together, after the slice tests
  - Quality assurance for manufacturing phase — define
  - Documents to EDMS, including pre-review specifications and reports on reviews
    - Activate EDMS life-cycle facilities

Relevant comments on level-1 (1)

- **Central Trigger**
  - Extract from general remarks:
    - There is no single physicist who is concerned with the timing of the experiment.
  - Extract from critical items:
    - Level-1 requires the definition of the ROD crate DAQ, including recommendation of processor hardware and histogramming tools.
- **Calorimeter trigger**
  - Preprocessor general remarks:
    - KIP possesses a complete set of tools for design and testing of ASICs and MCMs. A new rework station to permit the handling of BGA packages has been purchased.
    - There is a clear shortage of manpower in software development, which is critical for the slice test.
    - Technical responsibility for the electronics between the TileCal on-detector electronics and the Preprocessor modules is not defined, although the system is covered financially.

Relevant comments on level-1 (2)

- Preprocessor interface concern:
  - The interface between the PPr and the TileCal electronics (Leitner) should be reconfirmed, given the other duties of the TileCal PL.
- Preprocessor critical items:
  - Preprocessor ASIC functional testing.
  - Programming for slice test is on the critical path. This could be ameliorated by DIG providing the level-1 team with standard tools (Online, Dataflow, ROD-crate DAQ, Database, etc.) and by providing support for the use of these tools.
- Cluster Processor and Jet/Energy Processor general remarks:
  - The resources for PCB design at the collaborating institutions appears adequate.
  - As mentioned above, the software effort, particularly for the slice tests, needs strengthening.
  - Retention of electronics manpower is another problem. It is currently OK, but when the economy recovers there may be a new problem in this area.

Relevant comments on level-1 (3)

- CP and JEP remarks (continued)
  - Technical problems of working with BGAs on large boards need to be understood.
- CP and JEP interface concerns:
  - Calorimeter level-1 and LARG calibration system. No contact people identified.
  - Calorimeter level-1 and TileCal calibration system. No contact people identified.
- CP and JEP critical item:
  - Backplane for processors (schedule and performance verification).

Higher-level triggers

- Extract on software for level-1 trigger:
  - The present level-1 software organisation is very closely tied to the PBS, with software deliverables tied directly to hardware items. As many of the hardware tasks are successfully entering the production phase, it is critical to organise an overall level-1 software effort in order to complete the complex codes which will be needed to commission, monitor, and diagnose problems, in the complete level-1 trigger system.

Actions from ASSO (1)

- **Level-1 to identify software manpower resources for the slice test.**
- **DIG to identify a contact person or persons to provide backup support for slice test.**
- **Level-1 and LARG to document connections between LARG receivers and Level-1 Preprocessor.**
  (By December 2001?)
  Should really cover from LARG cells to Preprocessor!
- **LARG to name the institution which will provide the LARG receiver hardware and to name (or reconfirm) the contact person for this system.**
  (By April 2002)

Actions from ASSO (2)

- **Level-1 and TileCal to document the connections between trigger signal outputs on TileCal and Preprocessor inputs.**
  (By April 2002)
- **Level-1 to specify the institution which will provide the TileCal receiver hardware, and Level-1 and TileCal to provide the names of contact people.**
  (By July 2002)
- **LARG and Level-1 to identify contacts concerning use of LARG calibration system for Level-1 trigger.**
- **TileCal and Level-1 to identify contacts concerning use of TileCal calibration system for Level-1 trigger.**