



**Kirchhoff-Institut
für Physik**

ATLAS Level-1 Calorimeter Trigger

Joint Meeting @ RAL, Nov.2001



*Universität
Heidelberg*

Pre-Processor (System Issues)

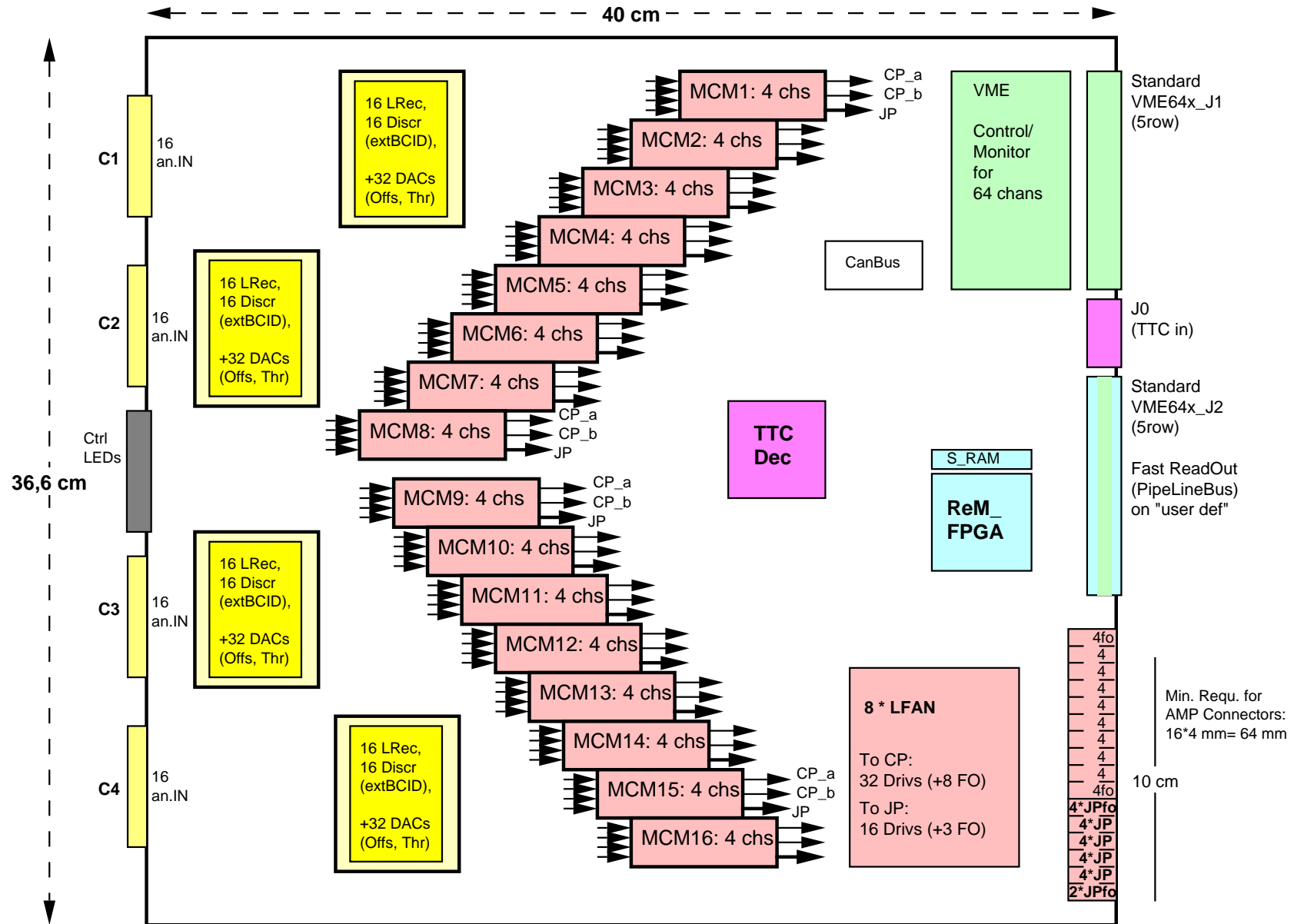
- The PPModule status
- The AnIn daughterboard, TCM adapter
- LVDS tests, LVDS backplate
- Material and Misc.

The PPModule

- Schematics still "growing" (KS, PS)
 - Commercial parts in libs (SubD37, cPCIs, VMEs)
 - AnIn, MCM, TTCrx_dPCB "footprint" in libs
 - LVDS daughterboard to be defined (see "LFan" later)

 - VME connected
 - work now on connectivity from front-panel through ... to cPCI
 - keep ReM_FPGA on 1.27mm pitch BGA(560 pins) for PCB manuf.
- Analog input signals (see H.Stenzel's talk for data)
- K.Penno works now on Video (see KP's talk)

Pre-Processor Module



Paul HANKE, KIP Heidelberg

The AnIn daughterboard (PCB: 75*75 mm**2)

- PCB with "decision for CMC connectors" included, out for manufacture (*"last" version before JK's retirement*)
 - 6 layers
 - more pins for better "Xtalk" shielding
 - PowerSupply-Input: +5V dig. separate from +5V analog
 - Comparator with "hysteresis"

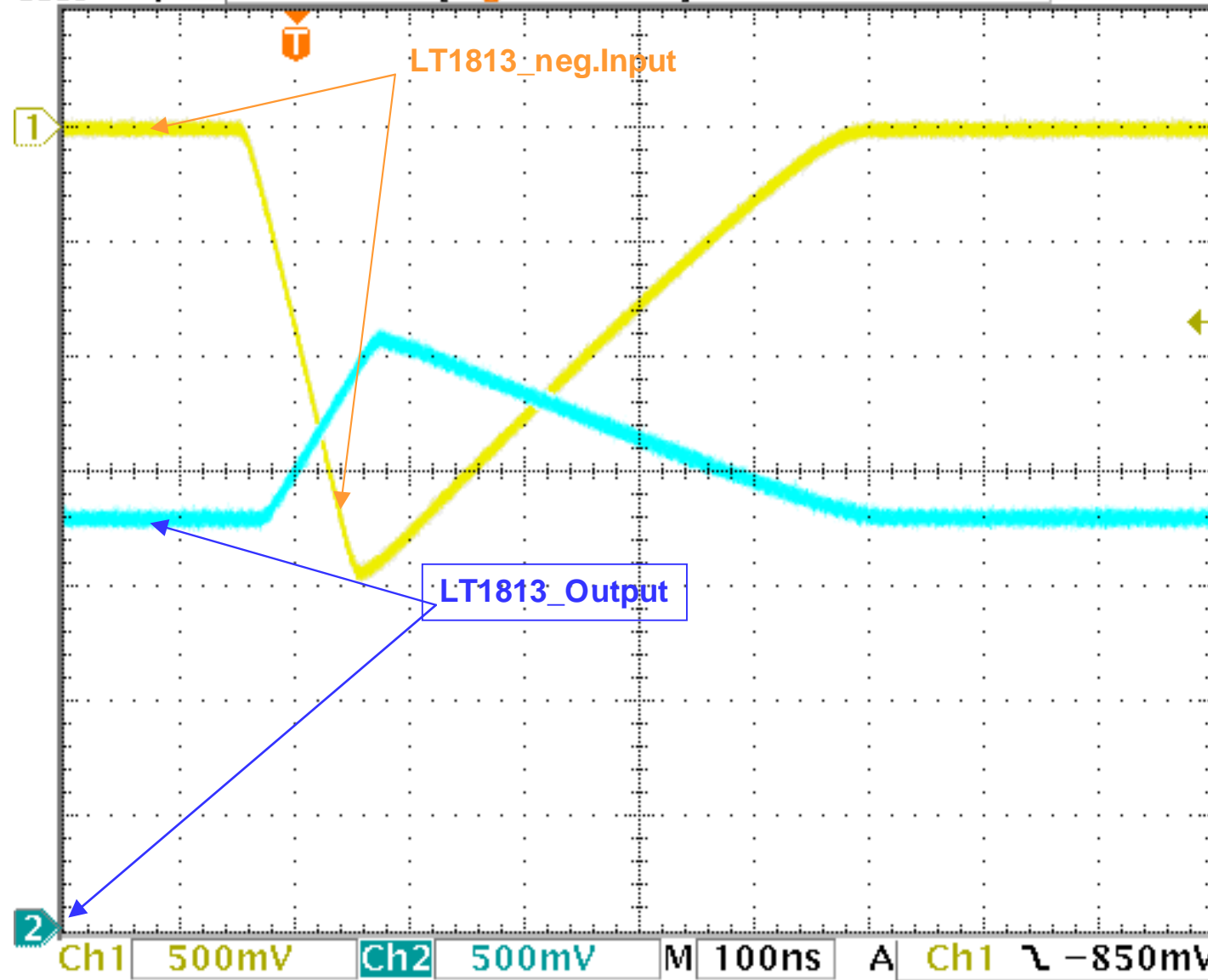
- insert feed-back "capacitor"-pads /channel to FADC;
test with MCM (see WH)

- LT1813 Oscillation-tests: to be done by us !?! (bench-test)
--->>> see first results (following 4):: NO Oscillation, "Clean" Saturation

The TCM-adapter for PPr

- schematics started (EU), ca. 50% done, for layouting the "physical" motherboard would be useful (connector placing etc.)

Tek Stop



Ch1 Fall
77.64ns

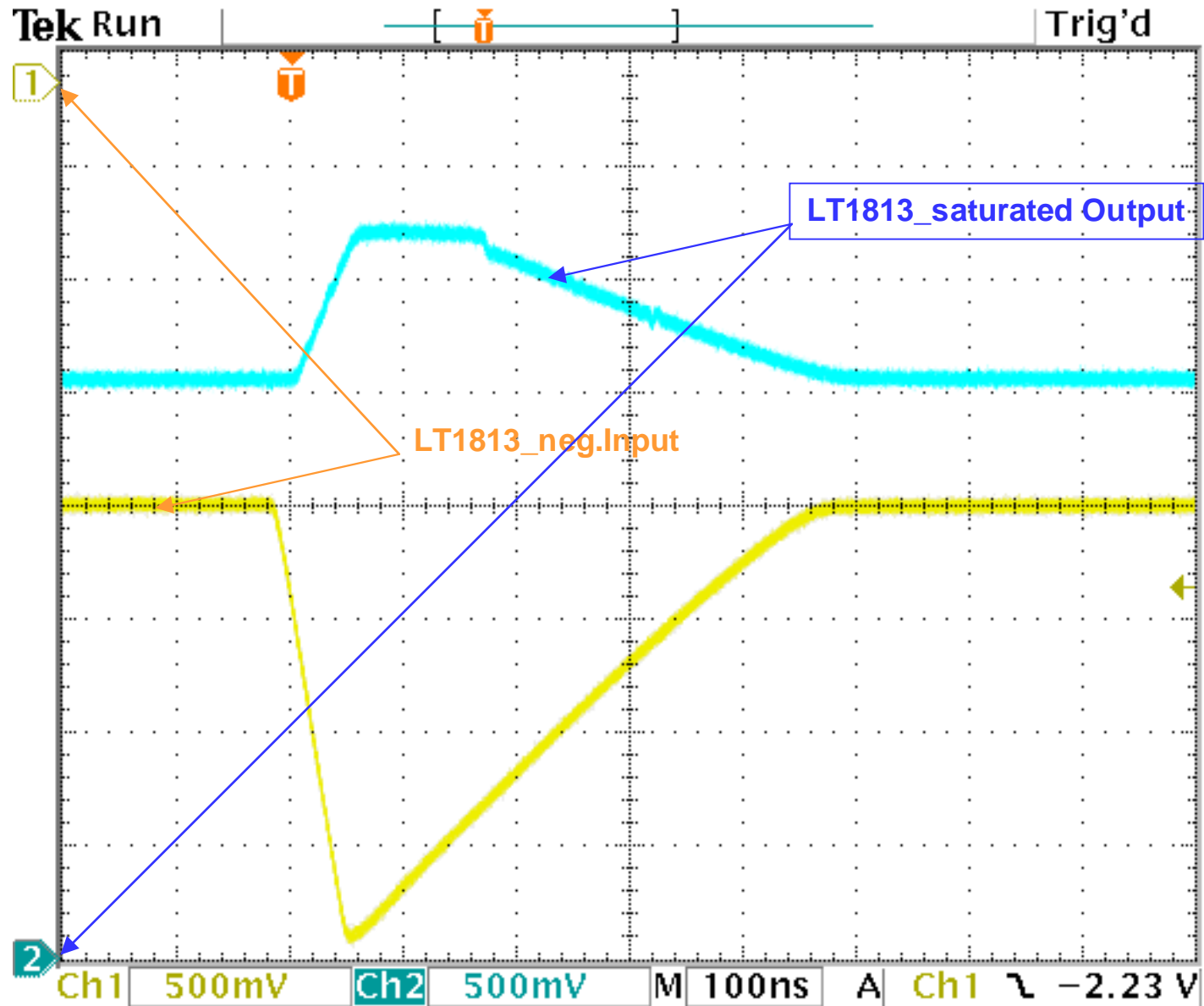
Ch2 Rise
78.99ns

Ch1 Pk-Pk
2.01 V

Ch2 Pk-Pk
868mV

20.20 %

26 Oct 2001
15:34:23



Ch1 Fall
51.00ns

Ch2 Rise
47.53ns

Ch1 Pk-Pk
1.99 V

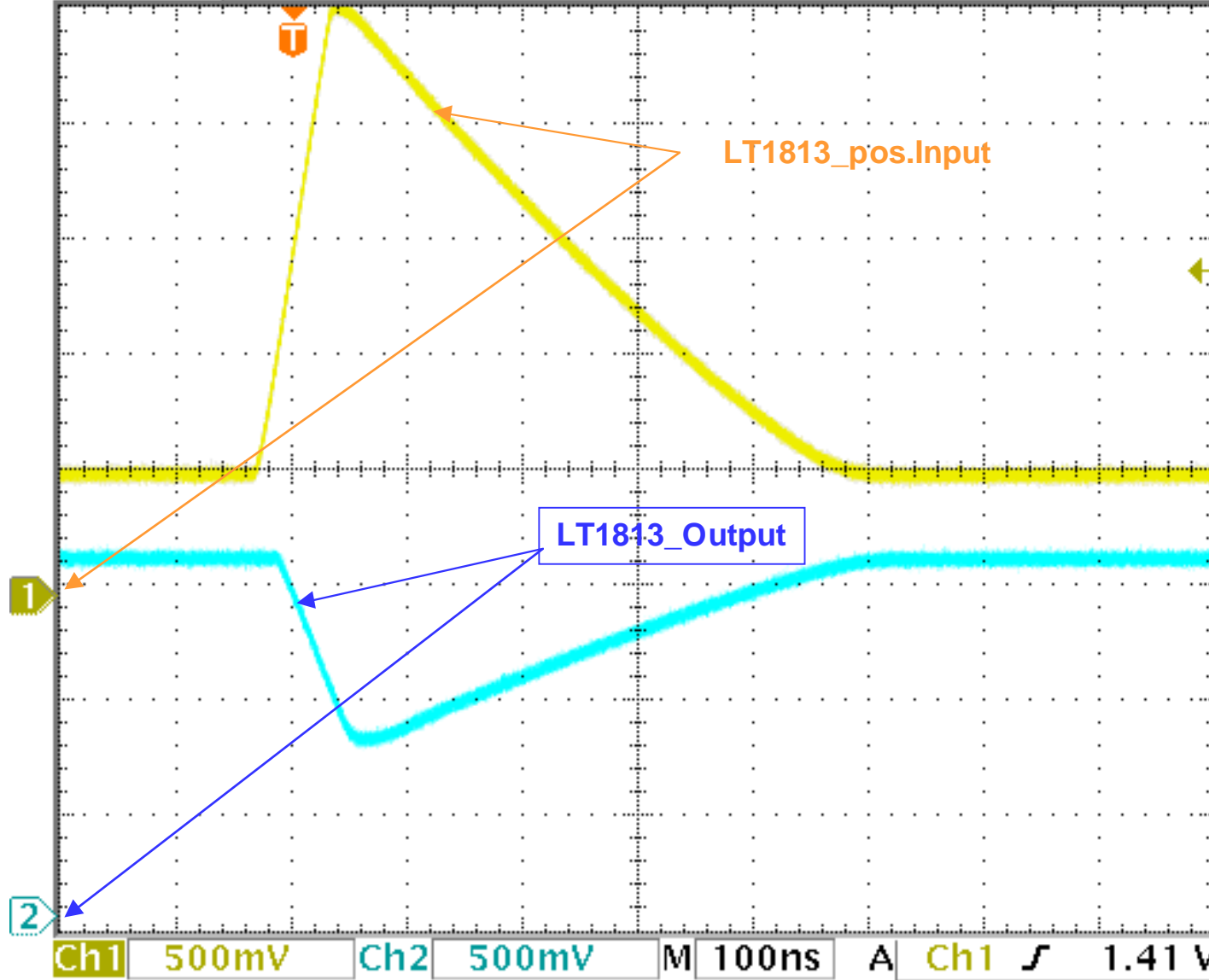
Ch2 Pk-Pk
742mV

20.20 %

26 Oct 2001
15:42:02

Tek Run

Trig'd



Ch1 Fall
345.4ns

Ch2 Rise
348.5ns

Ch1 Pk-Pk
2.09 V

Ch2 Pk-Pk
882mV

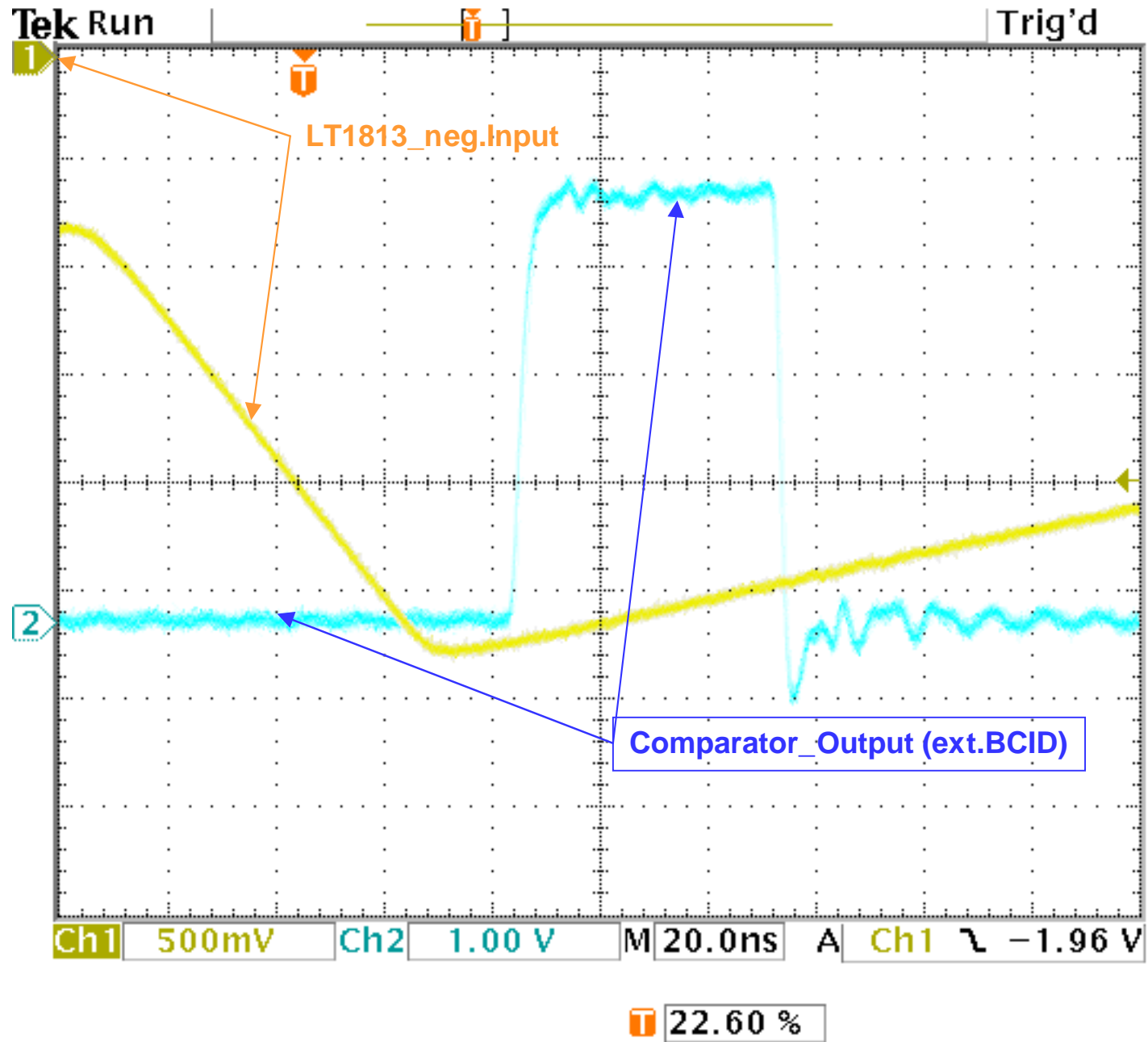
1

2

Ch1 500mV Ch2 500mV M 100ns A Ch1 1.41 V

20.20 %

26 Oct 2001
15:44:51



26 Oct 2001
16:17:58

LVDS tests, LVDS backplate

- **LVDS test PCB** (CMC board for mod.TestVME):

Layout nearly ready for manufacture,

late -> highest priority ->

- test 1021 @ "40 MHz+epsilon" (LHC clock @ 40.8 MHz)
- test XCV50E as "LFan substitute"

- **LVDS serializer implementation** (meanwhile clarified)

- 60 MHz (1023) is "footprint" compatible with 40 Mhz (1021)
i.e. present MCM layout is OK !
- "dies" are available acc. to distributor !

- **LVDS crate-backplate**

- commercial solution from ELMA-Trenew:
8 PPM--slots (3U) for LVDS throughput (B22, B25) with cable-shrouds
for AMP-cables

Material and Misc.

- Purchases for the full PPr project (orders placed):
 - front-panel connectors (SubD37)
 - VME connectors for PPM boards (J1, J2 , J0-cPCI)
 - cPCI connectors on PPM for LVDS output (B22, B25)
 - "Mezzanine" connectors for AnIn, LVDS "LFan"
 - >> ELMA-Trenew: 24 (*8slots)

••• "Forget-me-not"s

- Cabling and Tile-Receivers ? (W.Cleland @HD, Nov.26/27)
- ASSO
- Schedules (PRRs ?)
- Concept-HDL ? Transport of former designs ?
- ROD as on mod.TestVME (real ROD as "part of PPM" later)
- FTP to upload talks for next meets